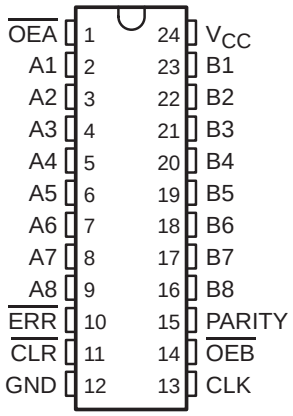
# SN54ABT833, SN74ABT833
# 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

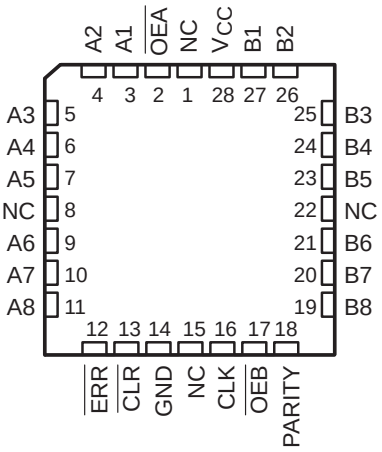
SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Parity Error Flag With Parity Generator/Checker**
- **Register for Storage of the Parity Error Flag**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

**SN54ABT833 . . . JT PACKAGE**
**SN74ABT833 . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**SN54ABT833 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The ’ABT833 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$ and $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated. The ’ABT833 provide true data at their outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the $\overline{ERR}$ flag. $\overline{ERR}$ is clocked into the register on the rising edge of the clock (CLK) input. The error flag register is cleared with a low pulse on the clear ($\overline{CLR}$) input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

## description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

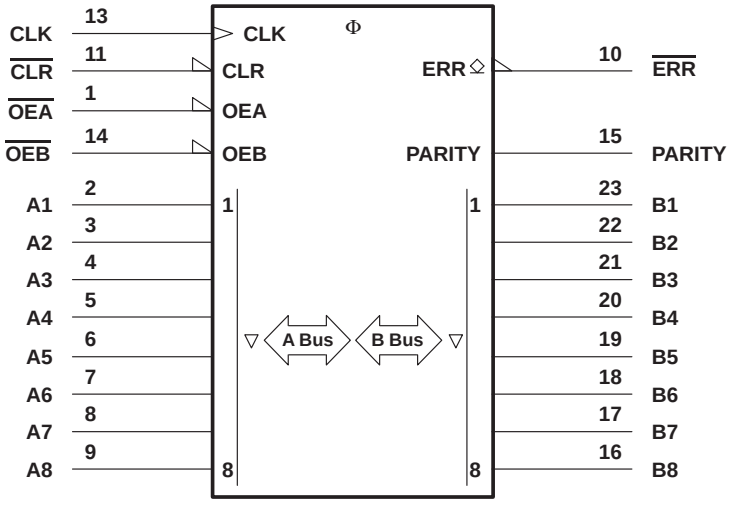
The SN54ABT833 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT833 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | OUTPUT AND I/O | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{OEB}$ | $\overline{OEA}$ | $\overline{CLR}$ | CLK | Ai Σ OF H's | Bi† Σ OF H's | A | B | PARITY | $\overline{ERR}$‡ | |
| L | H | X | X | Odd<br>Even | NA | NA | A | L<br>H | NA | A data to B bus and generate parity |
| H | L | H | ↑ | NA | Odd<br>Even | B | NA | NA | H<br>L | B data to A bus and check parity |
| X | X | L | X | X | X | X | NA | NA | H | Check error-flag register |
| H | H | H<br>L<br>H<br>H | No↑<br>No↑<br>↑<br>↑ | X<br>X<br>Odd<br>Even | X | Z | Z | Z | NC<br>H<br>H<br>L | Isolation§ |
| L | L | X | X | Odd<br>Even | NA | NA | A | H<br>L | NA | A data to B bus and generate inverted parity |

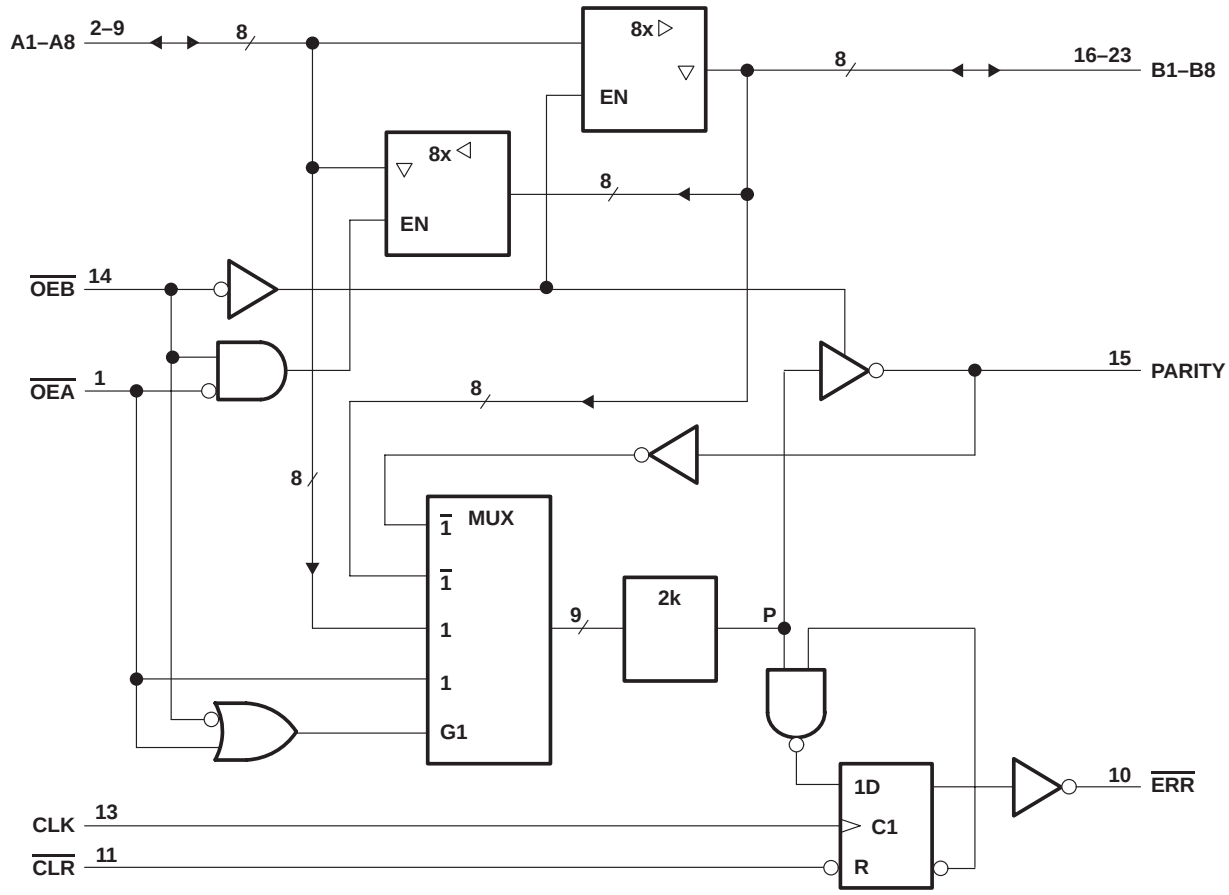
NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$ (when clocked) shows inverted parity of the A bus.

## logic symbol¶




¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)



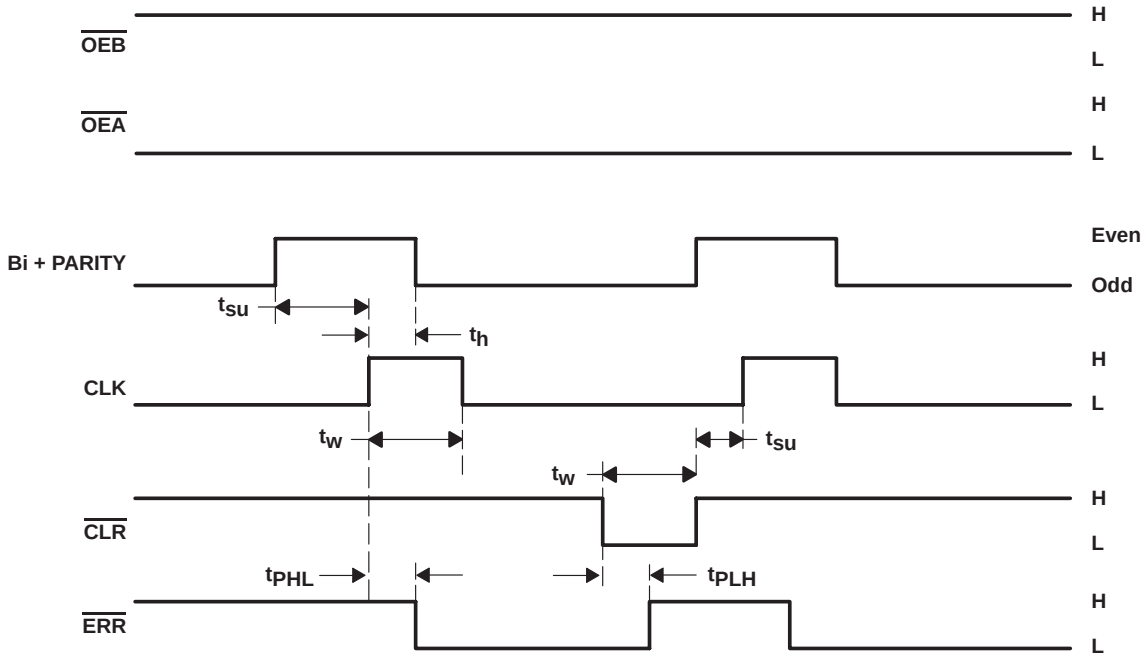

Pin numbers shown are for the DW, JT, and NT packages.

**ERROR-FLAG FUNCTION TABLE**

| INPUTS | | INTERNAL TO DEVICE | OUTPUT PRE-STATE | OUTPUT $\overline{ERR}$ | FUNCTION |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | POINT P | $\overline{ERR}_{n-1}$† | | |
| H | ↑ | H | H | H | Sample |
| H | ↑ | X | L | L | |
| H | ↑ | L | X | L | |
| L | X | X | X | H | Clear |

† The state of $\overline{ERR}$ before any changes at $\overline{CLR}$, CLK, or point P

### error-flag waveforms




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT833 . . . . . 96 mA
SN74ABT833 . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package . . . . . 81°C/W
NT package . . . . . 67°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54ABT833 | | SN74ABT833 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_{OH}$ | High-level output voltage | $\overline{ERR}$ | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | Except $\overline{ERR}$ | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 5 | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |



NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT833 | | SN74ABT833 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | All outputs except $\overline{ERR}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 24 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_{OH}$ | $\overline{ERR}$ | $V_{CC}$ = 4.5 V, | $V_{OH}$ = 5.5 V | | | 20 | | 20 | | 20 | µA |
| $I_I$ | Control inputs | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{IL}$ | A or B ports | $V_{CC}$ = 0, | $V_I$ = GND | | | –50 | | –50 | | –50 | µA |
| $I_{OZH}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | –50 | | –50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –100 | –200¶ | –50 | –200¶ | –50 | –200¶ | mA |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 1 | 250 | | 250 | | 250 | µA |
| | | | Outputs low | | 24 | 38¶ | | 38¶ | | 38¶ | mA |
| | | | Outputs disabled | | 0.5 | 250 | | 250 | | 250 | µA |
| $\Delta I_{CC}$# | Data inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | Outputs enabled | | | 1.5 | | 1.5 | | 1.5 | mA |
| | | | Outputs disabled | | | 50 | | 50 | | 50 | µA |
| | Control inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 4.5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10.5 | | | | | | pF |



* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ These limits may vary among suppliers.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

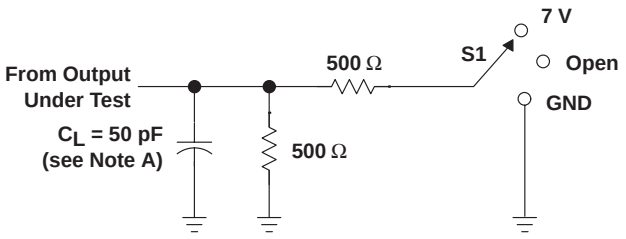
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54ABT833 | | SN74ABT833 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | 3 | | 3 | | 3 | | ns |
| | | $\overline{CLR}$ low | 3 | | 3 | | 3 | | |
| $t_{su}$ | Setup time before CLK↑ | B or PARITY high | 9.8 | | 9.8 | | 9.8 | | ns |
| | | B or PARITY low | 8.1 | | 8.1 | | 8.1 | | |
| | | $\overline{CLR}$ | 2 | | 2 | | 2 | | |
| $t_h$ | Hold time after CLK↑ | B or PARITY | 0 | | 0 | | 0 | | ns |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT833 | | SN74ABT833 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.2 | 2.8 | 4.8 | 1.2 | 5.4 | 1.2 | 5.3 | ns |
| $t_{PHL}$ | | | 1 | 3 | 4.8‡ | 1 | 5.4 | 1 | 5.3‡ | |
| $t_{PLH}$ | A | PARITY | 2.1 | 5.5 | 9.5 | 2.1 | 11.3 | 2.1 | 11.2 | ns |
| $t_{PHL}$ | | | 2.5 | 5.3 | 9.7 | 2.5 | 11.1 | 2.5 | 11 | |
| $t_{PZH}$ | $\overline{OE}$ | PARITY | 2.6 | 6.2 | 8.5 | 2.6 | 10.6 | 2.6 | 10.5 | ns |
| $t_{PZL}$ | | | 2.6‡ | 5.8 | 8.6 | 2.6‡ | 10.1 | 2.6‡ | 10 | |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{ERR}$ | 1 | 3.2 | 4.8‡ | 1 | 5.3 | 1 | 5.2 | ns |
| $t_{PHL}$ | CLK | | 1.2‡ | 2.8 | 5.7 | 1.2‡ | 6.3 | 1.2‡ | 6.2 | |
| $t_{PZH}$ | $\overline{OE}$ | A, B, or PARITY | 1 | 3.7 | 5.8‡ | 1 | 6.6 | 1 | 6.5‡ | ns |
| $t_{PZL}$ | | | 1.3‡ | 3.8 | 5.8 | 1.3‡ | 6.6 | 1.3‡ | 6.5‡ | |
| $t_{PHZ}$ | $\overline{OE}$ | A, B, or PARITY | 1.9‡ | 4.4 | 7.3 | 1.9‡ | 8 | 1.9‡ | 7.9 | ns |
| $t_{PLZ}$ | | | 2.2‡ | 4.4 | 7.7 | 2.2‡ | 8.2 | 2.2‡ | 8.1 | |

† All typical values are at $V_{CC}$ = 5 V.
‡ These limits may vary among suppliers.

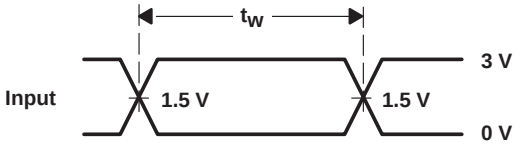
## PARAMETER MEASUREMENT INFORMATION



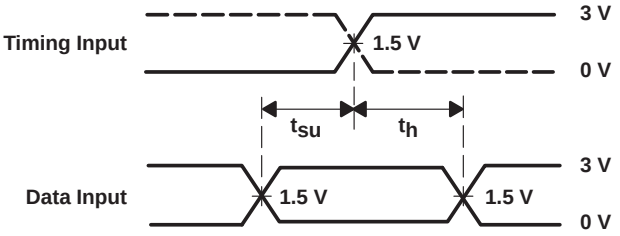

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

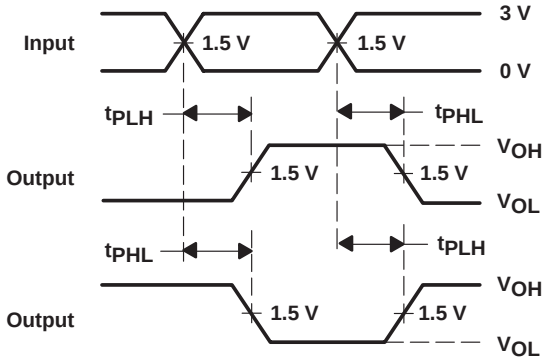
| $\overline{ERR}$ | S1 |
|---|---|
| $t_{PHL}$ | 7 V |
| $t_{PLH}$ | 7 V |



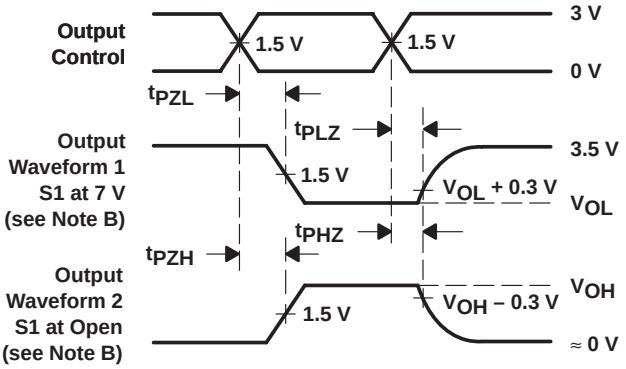

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.