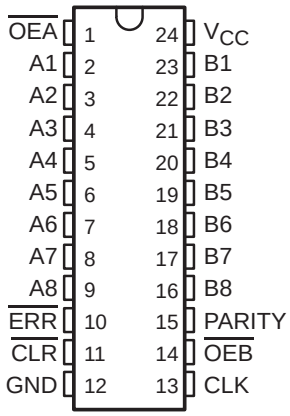
SN74ALS29833
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SDAS119D – FEBRUARY 1987 – REVISED JANUARY 1995

- **Functionally Similar to AMD's AM29833**
- **High-Speed Bus Transceiver With Parity Generator/Checker**
- **Parity-Error Flag With Open-Collector Outputs**
- **Register for Storing the Parity-Error Flag**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74ALS29833 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$, $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector $\overline{ERR}$ flag. $\overline{ERR}$ is clocked into the register on the rising edge of the clock (CLK) input. The error-flag register is cleared with a low pulse on the clear ($\overline{CLR}$) input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

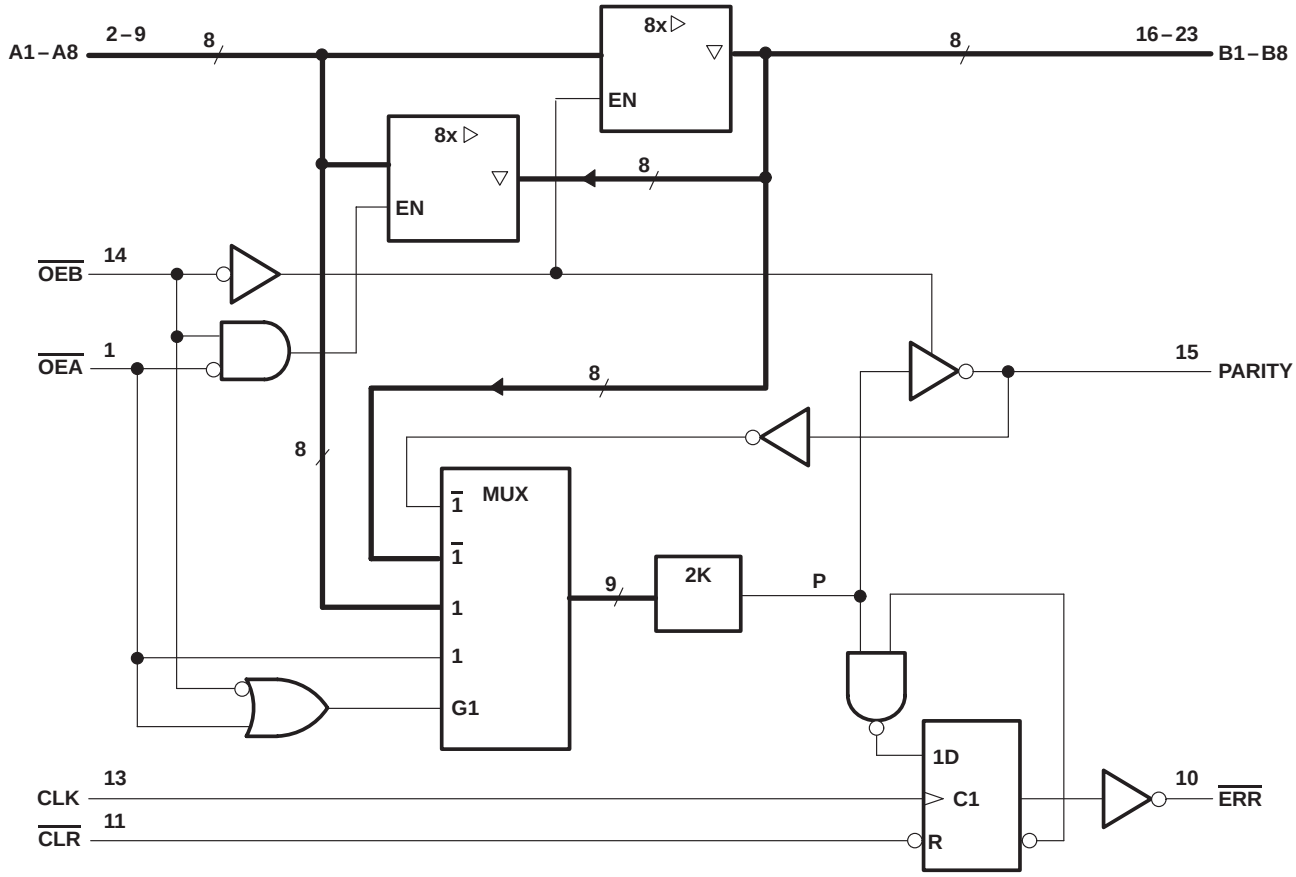
The SN74ALS29833 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

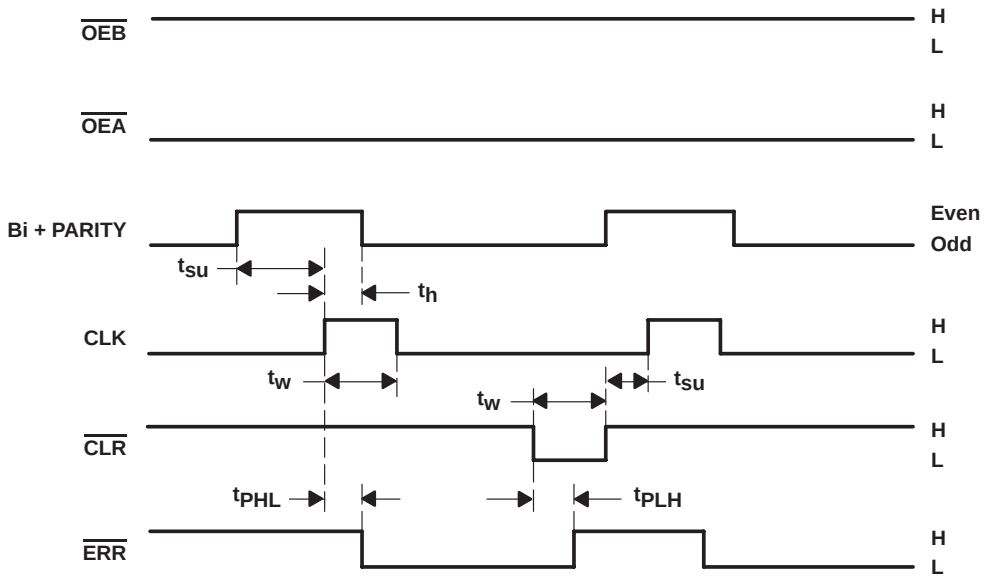
INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai $\sum$ of Hs	Bi† $\sum$ of Ls	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Clear error-flag register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation§
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$, when clocked, shows inverted parity of the A bus.

logic diagram (positive logic)



error-flag waveforms



ERROR-FLAG FUNCTIONS

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT P	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† $\overline{ERR}_{n-1}$ represents the state of $\overline{ERR}$ before any changes at $\overline{CLR}$, CLK, or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled I/O port . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$			5.5	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration	CLK high	10		ns
		CLK low	10		
		$\overline{CLR}$ low	10		
t_{su}	Setup time before CLK↑	Bi and PARITY	17		ns
		$\overline{CLR}$ inactive	15		
t_h	Hold time, Bi and PARITY after CLK↑		0		ns
T_A	Operating free-air temperature		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	All I/Os except $\overline{ERR}$	V_{CC} = 4.75 V	I_{OH} = –15 mA	2.4			V
			I_{OH} = –24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.75 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}‡	Data	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.2	mA
	Control					–0.75	
I_O§		V_{CC} = 5.25 V,	V_O = 0	–75		–250	mA
I_{CC}		V_{CC} = 5.25 V			70	100	mA

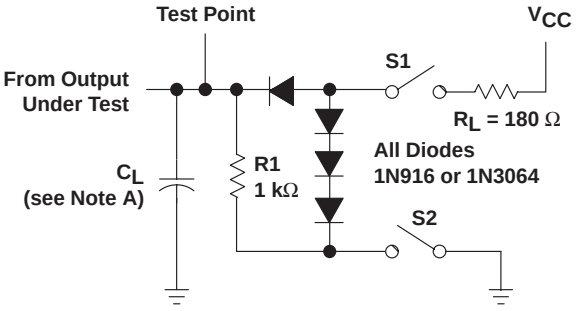
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4.75 V to 5.25 V, T_A = MIN to MAX¶		UNIT
				MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 50 pF		8	ns
t_{PHL}					8	
t_{PLH}	A or B	B or A	C_L = 300 pF		15	ns
t_{PHL}					15	
t_{PLH}	A	PARITY	C_L = 50 pF		15	ns
t_{PHL}					19	
t_{PLH}	A	PARITY	C_L = 300 pF		22	ns
t_{PHL}					24	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 50 pF		17	ns
t_{PZL}					17	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 300 pF		23	ns
t_{PZL}					23	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 5 pF		9	ns
t_{PLZ}					9	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 50 pF		15	ns
t_{PLZ}					8	
t_{PHL}	CLK	$\overline{ERR}$	C_L = 50 pF		13	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	C_L = 50 pF		13	ns
t_{PLH}	$\overline{OEA}$	PARITY	C_L = 50 pF		17	ns
t_{PHL}					19	
t_{PLH}	$\overline{OEA}$	PARITY	C_L = 300 pF		22	ns
t_{PHL}					25	

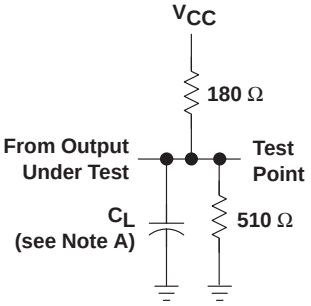
¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION



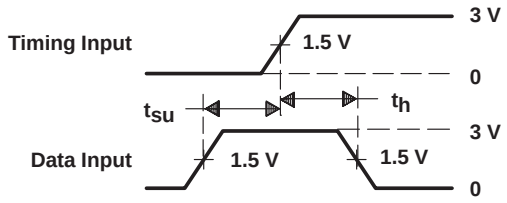
SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

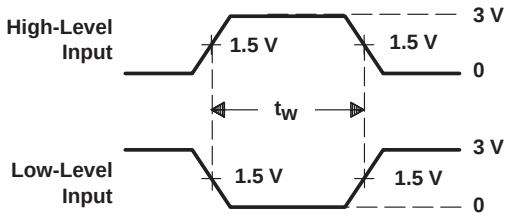


LOAD CIRCUIT 1
ALL OUTPUTS EXCEPT FOR ERROR FLAG

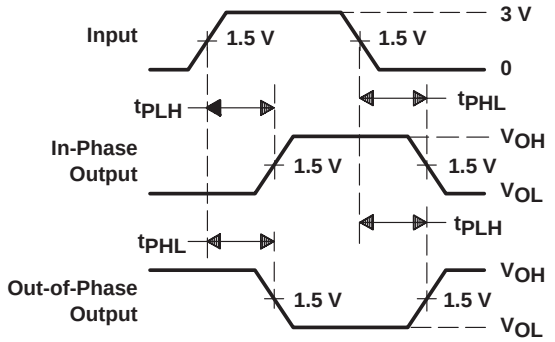
LOAD CIRCUIT 2
ERROR-FLAG OUTPUT



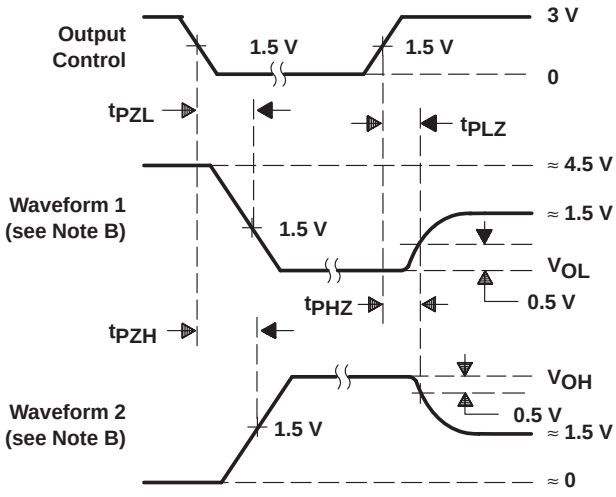
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuits and Voltage Waveforms

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