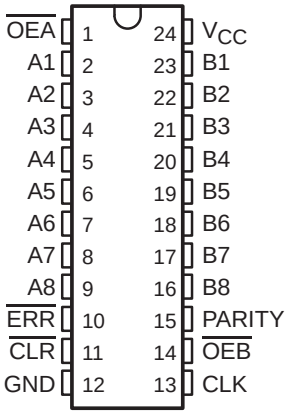
SN74BCT29834
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SCBS256 – SEPTEMBER 1987 – REVISED NOVEMBER 1993

- **BiCMOS Process With TTL Inputs and Outputs**
- **BiCMOS Design Reduces Standby Current**
- **Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Functionally Equivalent to SN74ALS29834 and AMD Am29834**
- **High-Speed Bus Transceiver With Parity Generator/Checker**
- **Parity-Error Flag With Open-Collector Output**
- **Available Register For Storage of the Parity-Error Flag**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74BCT29834 is an 8-bit to 9-bit parity transceiver designed for asynchronous communication between data buses. When data is transmitted from the A to B bus, a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the parity-error ($\overline{ERR}$) output will indicate whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$, $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector parity-error flag ($\overline{ERR}$). $\overline{ERR}$ is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the clear ($\overline{CLR}$) input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition which gives the designer more system diagnostic capability. The SN74BCT29834 provides inverting logic.

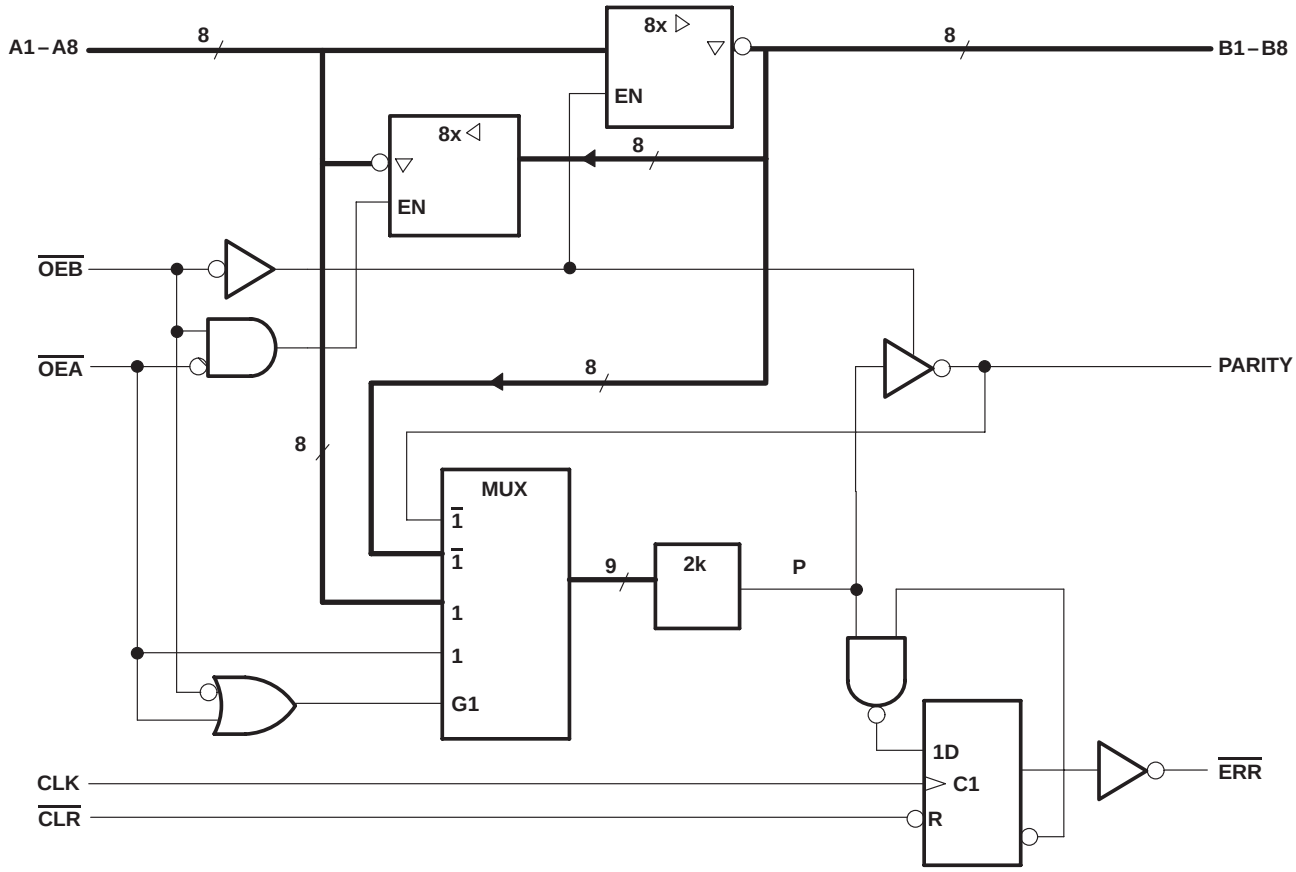
The SN74BCT29834 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai ∑ of H's	Bi† ∑ of L's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ data to B bus and generate parity
H	L	H	↑	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Clear error-flag register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume the $\overline{ERR}$ output was previously high.
§ In this mode, the $\overline{ERR}$ output, when enabled, shows inverted parity of the A bus.

functional logic diagram (positive logic)



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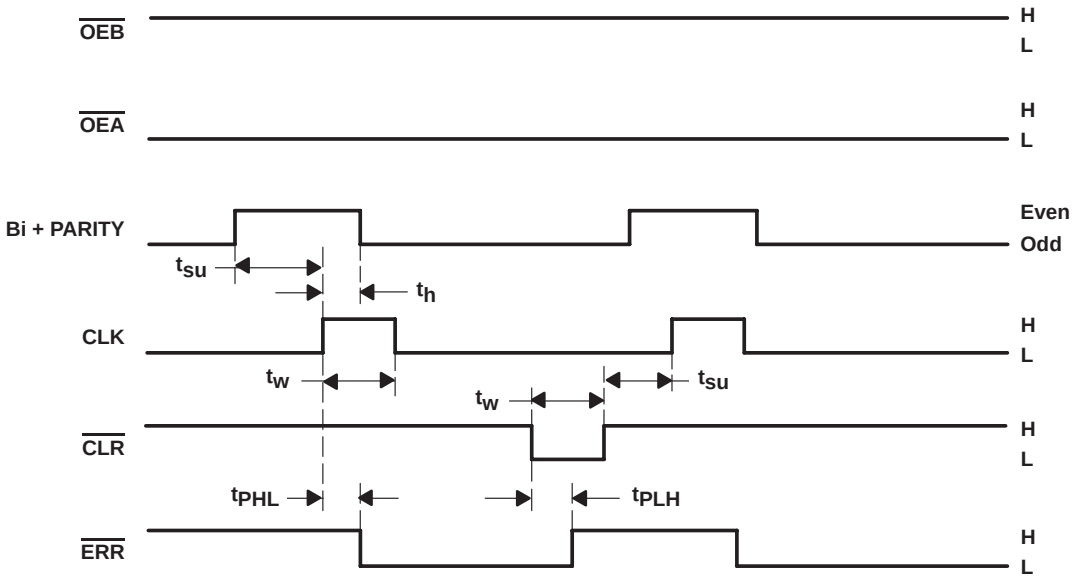
error-flag waveforms



ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT P	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† $\overline{ERR}_{n-1}$ represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled I/O port . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$			2.4	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	All inputs/outputs except $\overline{ERR}$	V_{CC} = 4.5 V	I_{OH} = –15 mA	2.4			V
			I_{OH} = –24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.5 V,	V_{OH} = 2.4 V			20	µA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}‡	Data	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2	mA
	Control					–0.75	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	–75		–250	mA
I_{CCL}		V_{CC} = 5.5 V,	Outputs open		55	80	mA
I_{CCZ}		V_{CC} = 5.5 V,	Outputs open		30	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters include off-state output current for I/O ports only.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	CLK high	10		ns
		CLK low	10		
		$\overline{CLR}$ low	10		
t_{su}	Setup time before CLK↑	Bi and PARITY	12		ns
		$\overline{CLR}$ inactive	12		
t_h	Hold time after CLK↑	Bi and PARITY	0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	8	ns
t_{PHL}			1.5	4	6	1.5	7	
t_{PLH}	A	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	8	10	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	11	15	2	19	ns
t_{PZL}			2	15	19	2	21	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	8	11	2	15	ns
t_{PLZ}			2	13	17	2	21	
t_{PLH}	CLK	$\overline{ERR}$	1.5	7	10	1.5	12	ns
	$\overline{CLR}$		1.5	13	17	1.5	18	
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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