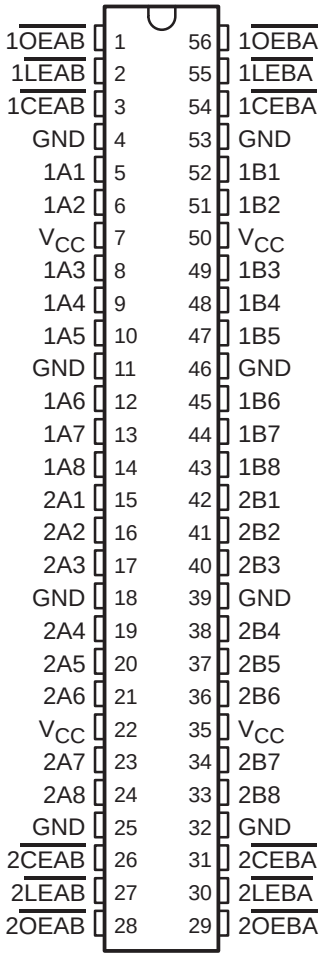
- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16543 . . . WD PACKAGE
74ACT16543 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The ’ACT16543 are 16-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. The ’ACT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) and $\overline{OEAB}$ inputs must be low to enter data from A or to output data to B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition at $\overline{LEAB}$ puts the A latches in the storage mode. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The 74ACT16543 is packaged in TI’s shrink small-outline package, which provides twice the functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16543 is characterized for operation from –40°C to 85°C.

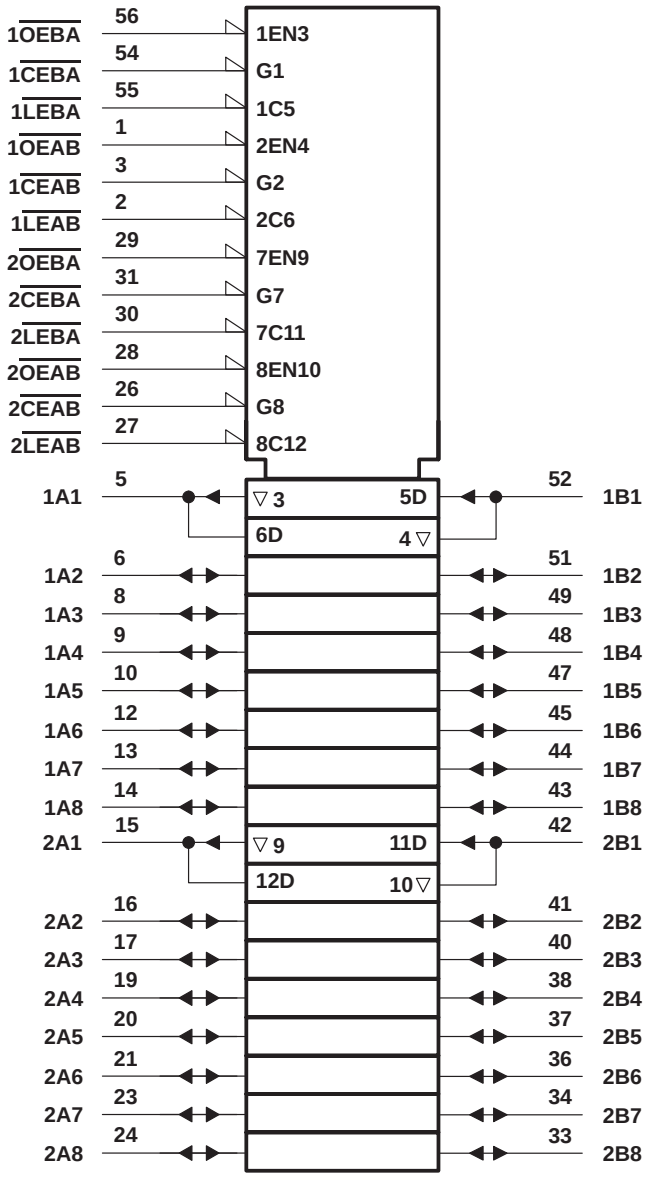
FUNCTION TABLE
(each octal register)

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1–B8
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$		
H	X	X	Storing	Z
X	H	X	Storing	
X	X	H		Z
L	L	L	Transparent	Current A data
L	H	L	Storing	Previous A data‡

† A-to-B data flow is shown: B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

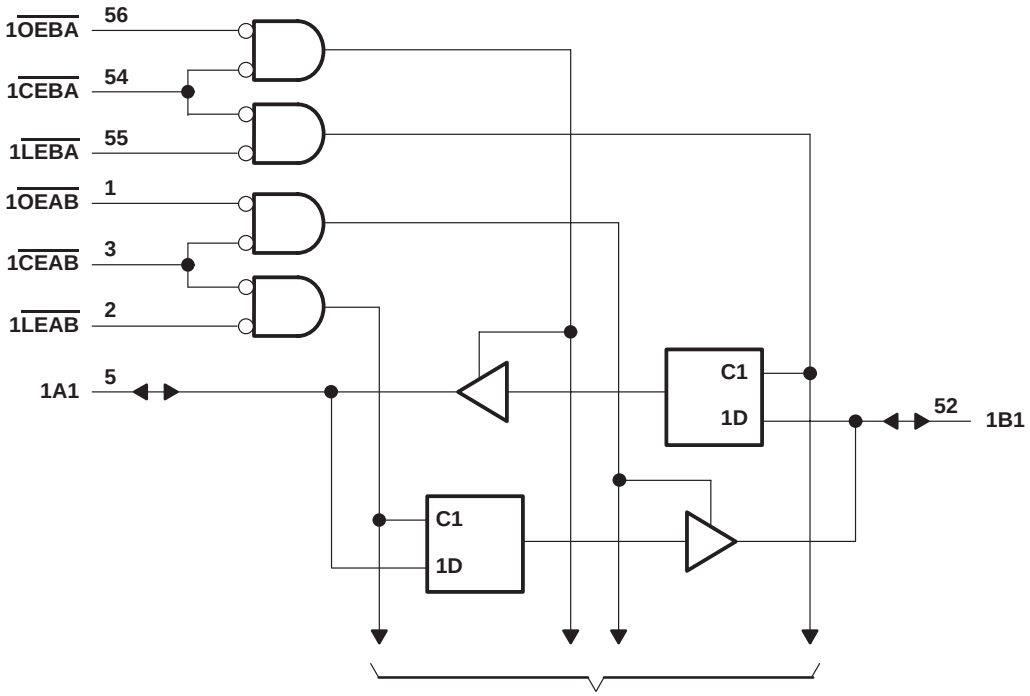
‡ Data present before low-to-high transition of $\overline{\text{LEAB}}$ occurring while $\overline{\text{CEAB}}$ is low

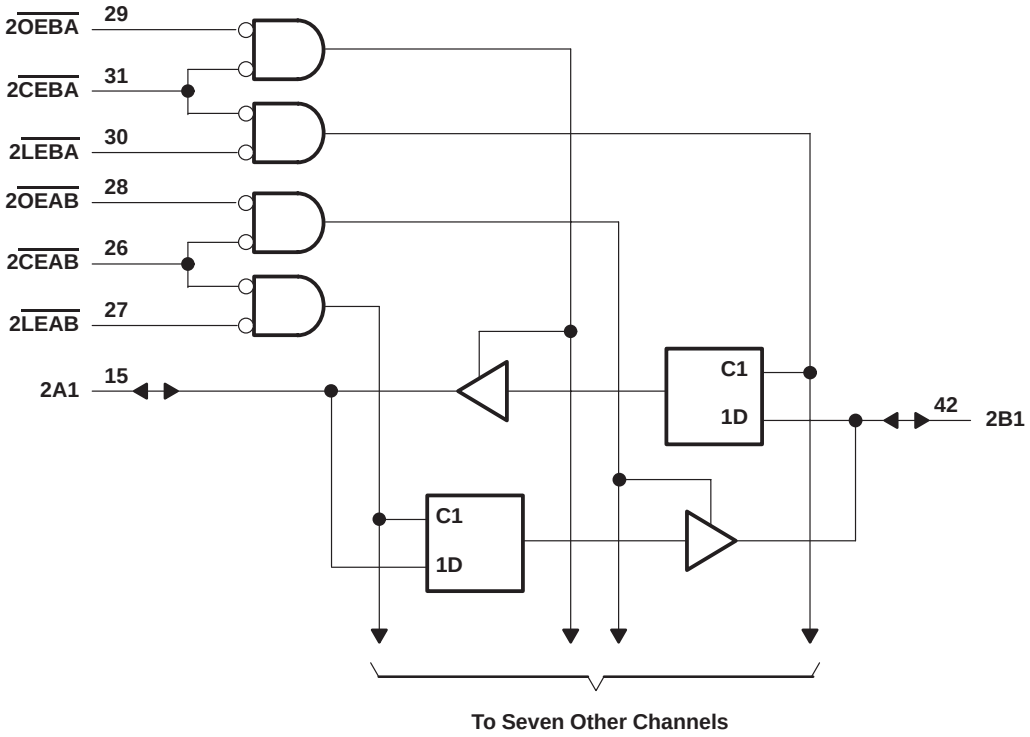
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC}+0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16543			74ACT16543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 4)	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTES: 3. Unused pins (inputs and I/O) must be held high or low to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16543		74ACT16543		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = –24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54ACT16543		74ACT16543		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	7.5		7.5		7.5		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$↑	2.5		2.5		2.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$↑	4		4		4		ns

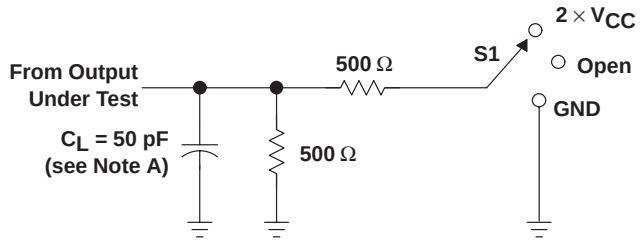
switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16543		74ACT16543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3.5	6.9	9.5	3.5	10.5	3.5	10.5	ns
t_{PHL}			3.1	7.3	10.7	3.1	11.6	3.1	11.6	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3.9	8.6	12.3	3.9	13.8	3.9	13.8	ns
t_{PHL}			3.9	8.7	12.2	3.9	13.5	3.9	13.5	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.6	7.1	10.3	2.6	11.4	2.6	11.4	ns
t_{PZL}			3.5	8.3	11.9	3.5	13.2	3.5	13.2	
t_{PHZ}	OEBA or OEAB	A or B	4.1	8.2	10.5	4.1	11.1	4.1	11.1	ns
t_{PLZ}			5	7.3	9.3	5	9.6	5	9.6	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.1	7.3	10.7	3.1	11.7	3.1	11.7	ns
t_{PZL}			3.9	8.5	12.2	3.9	13.5	3.9	13.5	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.6	8.5	11	4.6	11.6	4.6	11.6	ns
t_{PLZ}			5.2	7.4	9.7	5.2	10.5	5.2	10.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

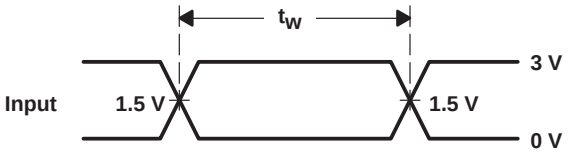
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

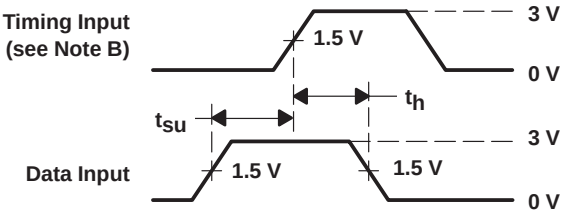


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

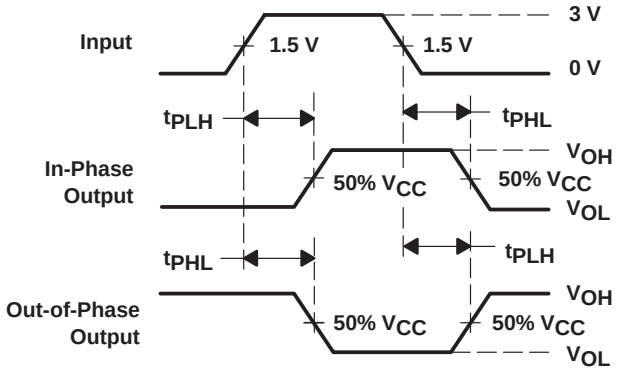
LOAD CIRCUIT



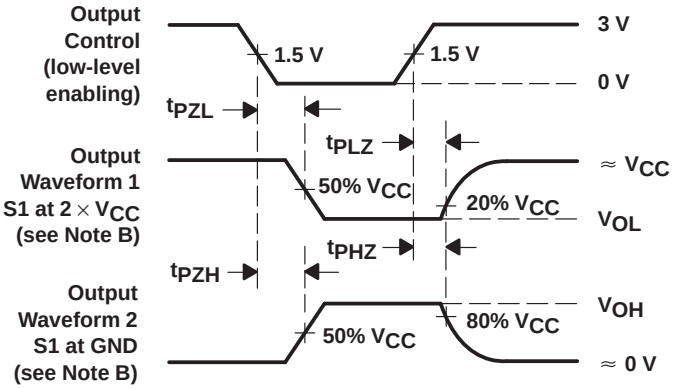
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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