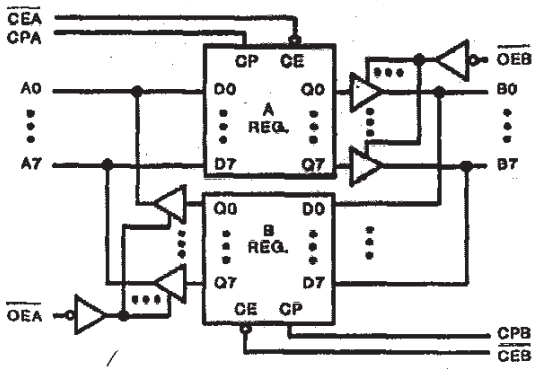
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS295

The CD54FCT2952A was not acquired from Harris Semiconductor.

CD54/74FCT2952A

Octal Register-Transceivers, 3-State

CD54/74FCT2952A - Non-Inverting



FCT2952A FUNCTIONAL DIAGRAM

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 5.6ns @ VCC = 5V, TA = 25°C, CL = 50pF*

The CD54/74FCT2952A octal register-transceiver uses a small-geometry BICMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices contain two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Each register has separate clock, clock enable, and 3-state output enable signals associated with it.

The CD54/74FCT2952A is supplied in the 24-lead small-outline plastic packages (M suffix). This package type is operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

Family Features:

- *SCR-latchup-resistant BICMOS process and circuit design*
- *FCTXXXXA - Speed of bipolar FAST*/AS/S*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BICMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54FCT2952A is also available in chip form (H suffix). This unpackaged device is operable over the -55°C to +125°C temperature range.

REGISTER FUNCTION TABLE (APPLIES TO A OR B REGISTER)

INPUTS			INTERNAL	
D	CP	$\overline{CE}$	Q	FUNCTION
X	X	H	NC	Hold Data
L	↓	L	L	Load Data
H	↓	L	H	

OUTPUT CONTROL

	INTERNAL	OUTPUTS	
$\overline{OE}$	Q	FCT2952A	FUNCTION
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

File Number 2400.1

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

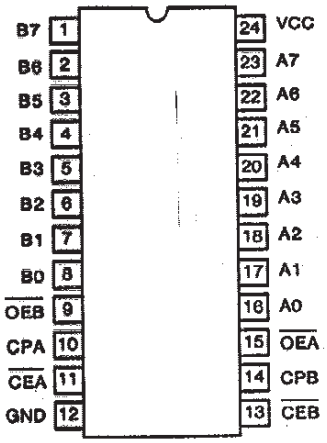
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

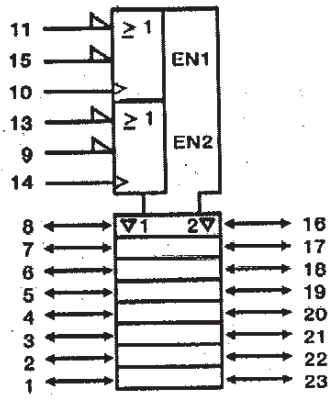
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT2952A TYPE



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, −55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	−55°C to +125°C MIN	−55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	–	2	–	2	–	V
Low-Level Input Voltage	VIL			4.5 to 5.5	–	0.8	–	0.8	–	0.8	V
High-Level Output Voltage	VOH	VIH or	−15	MIN	2.4	–	2.4	–	–	–	V
		VIL	−12	MIN	2.4	–	–	–	2.4	–	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	–	0.55	–	0.55	–	–	V
		VIL	48	MIN	–	0.55	–	–	–	0.55	V
High-Level Input Current	IIH	VCC		MAX	–	0.1	–	1	–	1	µA
Low-Level Input Current	IIL	GND		MAX	–	−0.1	–	−1	–	−1	µA
3-State Leakage Current	IOZH	VCC		MAX	–	0.5	–	10	–	10	µA
	IOZL	GND		MAX	–	−0.5	–	−10	–	−10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	−60	–	−60	–	−60	–	mA
Input Clamp Voltage	VIK	VCC or GND	−18	MIN	–	−1.2	–	−1.2	–	−1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	–	8	–	80	–	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	–	1.6	–	1.6	–	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

Prerequisite for Switching

PARAMETER	SYMBOL	VCC (V)	+25°C	0°C to +70°C		-55°C to +125°C		UNITS
			TYP	MIN	MAX	MIN	MAX	
Clock Pulse Width CPA, CPB	tW	5†	-	3	-	3	-	ns
Setup Time An, Bn to CPA, CPB	tSU	5	-	2	-	2.5	-	ns
$\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	tSU	5	-	3	-	3	-	ns
Hold Time An, Bn to CPA, CPB	tH	5	-	2	-	2	-	ns
$\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	tH	5	-	2	-	2	-	

† 5V: min. is at 4.5V., min. is at 4.75V for 0°C to +70°C, typ. is at 5V.

Switching Specifications FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

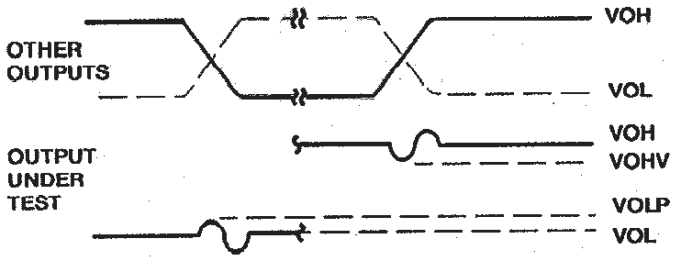
PARAMETER	SYMBOL	VCC (V)	+25°C	0°C to +70°C		-55°C to +125°C		UNITS
			TYP	MIN	MAX	MIN	MAX	
Propagation Delays CPA, CPB to Bn, An	tPLH, tPHL	5†	5.5	2	10	2	11	ns
Output EnableTime $\overline{OEA}$ or $\overline{OEB}$ to An or Bn	tPZL, tPZH	5	5.5	1.5	10.5	1.5	13	ns
Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An or Bn	tPLZ, tPHZ	5	5.5	1.5	10	1.5	10	ns
Power Dissipation Capacitance	CPD§	-	56 Typical					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 1	5	0.5 Typical at +25°C					V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 1	5	1 Typical at +25°C					V
Input Capacitance	CI	-	-	-	10	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	15	-	15	pF

† 5V: min. is at 5.5V, max. is at 4.5V.
5V: min. is at 5.25V for 0°C to +70°C, max. is at 4.75V for 0°C to +70°C, typ. is at 5V

§ CPD, measured per function, is used to determine the dynamic power consumption. PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:

VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

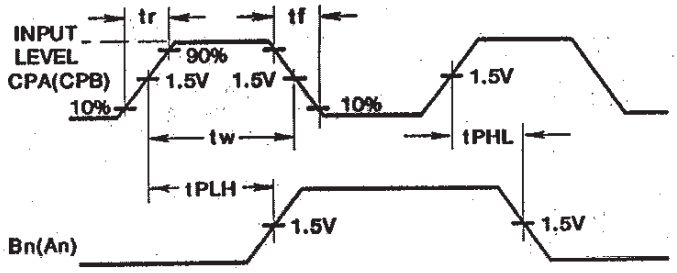


Figure 2 - CD54/74FCT2952A propagation delay times.

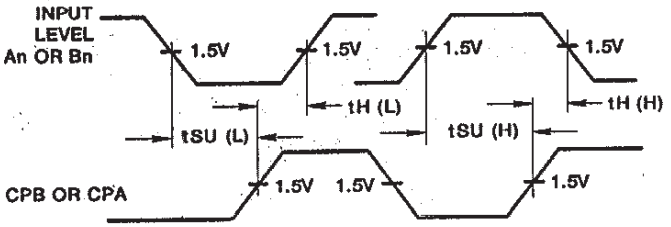
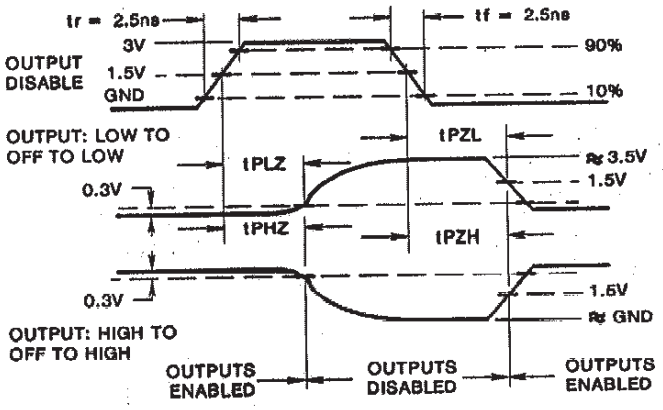
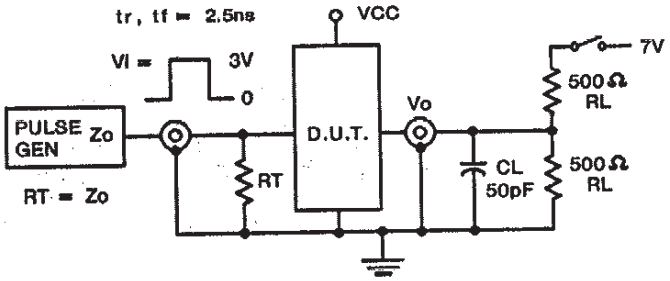


Figure 3 - Setup and hold times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

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