

8-Bit Latched Registered Transceiver

Features

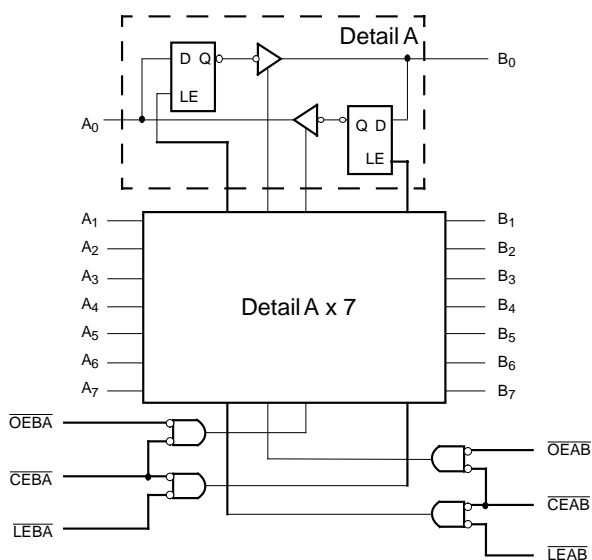
- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.3 ns max. (Com'l)
FCT-A speed at 6.5 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V
- Sink current 64 mA (Com'l), 48 mA (Mil)
Source current 32 mA (Com'l), 12 mA (Mil)
- Separation controls for data flow in each direction
- Back to back latches for storage
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$

Functional Description

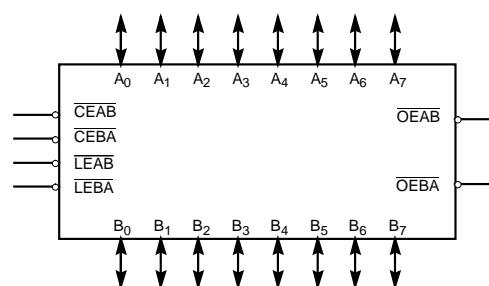
The FCT543T octal latched transceiver contains two sets of eight D-type latches with separate latch enable ($\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$) and output enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B enable ($\overline{\text{CEAB}}$) input must be LOW in order to enter data from A or to take data from B, as indicated in the truth table. With $\overline{\text{CEAB}}$ LOW, a LOW signal on the A-to-B latch enable ($\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their output no longer change with the A inputs. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both LOW, the three-stage B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Functional Block Diagram

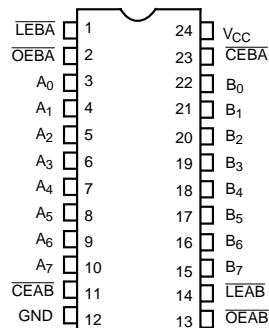


Logic Block Diagram



Pin Configurations

SOIC/QSOP Top View



Pin Description

Name	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
\overline{CEAB}	A-to-B Enable Input (Active LOW)
\overline{CEBA}	B-to-A Enable Input (Active LOW)
\overline{LEAB}	A-to-B Latch Enable Input (Active LOW)
\overline{LEBA}	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table^[1, 2]

Inputs			Latch	Outputs
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A-to-B ^[3]	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transpar-ent	Current A Inputs
L	H	L	Storing	Previous A Inputs

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- A-to-B data flow shown: B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .
- Before \overline{LEAB} LOW-to-HIGH Transition.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.

Maximum Ratings^[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-65°C to +135°C
Supply Voltage to Ground Potential.....	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage.....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, CT	-40°C to +85°C	5V ± 5%
Military ^[6]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[8]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current ^[8]	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current ^[8]	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} = 2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[8]

Parameter	Description	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is specified but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC}=\text{Max.}, V_{IN}\leq 0.2V, V_{IN}\geq V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	$V_{CC}=\text{Max.}, V_{IN}=3.4V,^{[10]}$ $f_1=0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[11]	$V_{CC}=\text{Max.}, \text{One Input Toggling,}$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\overline{CEAB} \text{ and } \overline{OEAB}=\text{LOW, } \overline{CEBA}=\text{HIGH,}$ $V_{IN}\leq 0.2V \text{ or } V_{IN}\geq V_{CC}-0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current ^[12]	$V_{CC}=\text{Max.}, f_0=10 \text{ MHz,}$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\text{One Bit Toggling at } f_1=5 \text{ MHz,}$ $\overline{CEAB} \text{ and } \overline{OEAB}=\text{LOW, } \overline{CEBA}=\text{HIGH,}$ $f_0=\overline{LEAB} = 10 \text{ MHz,}$ $V_{IN}\leq 0.2V \text{ or } V_{IN}\geq V_{CC}-0.2V$	0.7	1.4	mA
		$V_{CC}=\text{Max.}, f_0=10 \text{ MHz,}$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\text{One Bit Toggling at } f_1=5 \text{ MHz,}$ $\overline{CEAB} \text{ and } \overline{OEAB}=\text{LOW, } \overline{CEBA}=\text{HIGH,}$ $f_0=\overline{LEAB} = 10 \text{ MHz, } V_{IN}=3.4V \text{ or } V_{IN}=\text{GND}$	1.2	3.4	mA
		$V_{CC}=\text{Max.}, f_0=10 \text{ MHz,}$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\text{Eight Bits Toggling at } f_1=5 \text{ MHz,}$ $\overline{CEAB} \text{ and } \overline{OEAB}=\text{LOW, } \overline{CEBA}=\text{HIGH,}$ $f_0=\overline{LEAB} = 10 \text{ MHz,}$ $V_{IN}\leq 0.2V \text{ or } V_{IN}\geq V_{CC}-0.2V$	2.8	5.6 ^[13]	mA
		$V_{CC}=\text{Max.}, f_0=10 \text{ MHz,}$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\text{Eight Bits Toggling at } f_1=5 \text{ MHz,}$ $\overline{CEAB} \text{ and } \overline{OEAB}=\text{LOW, } \overline{CEBA}=\text{HIGH,}$ $f_0=\overline{LEAB} = 10 \text{ MHz, } V_{IN}=3.4V \text{ or } V_{IN}=\text{GND}$	5.1	14.6 ^[13]	mA

Notes:

10. Per TTL driven input ($V_{IN}=3.4V$); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN}=3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[14]

Parameter	Description	FCT543T				FCT543AT		Unit	Fig. No. ^[15]
		Military		Commercial		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.0	10.0	2.5	8.5	2.5	6.5	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A, LEAB to B	2.5	14.0	2.5	12.5	2.5	8.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	14.0	2.0	12.0	2.0	9.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	13.0	2.0	9.0	2.0	7.5	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW, A or B to LEBA or LEAB	3.0		2.0		2.0		ns	9
t _H	Hold Time HIGH or LOW, A or B to LEBA or LEAB	2.0		2.0		2.0		ns	9
t _W	Pulse Width LOW ^[8] LEBA or LEAB	5.0		5.0		5.0		ns	5

Parameter	Description	FCT543CT		Unit	Fig. No. ^[15]
		Commercial			
		Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A to B or B to A	2.5	5.3	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A, LEAB to B	2.5	7.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	8.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B	2.0	6.5	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW, A or B to LEBA or LEAB	2.0		ns	9
t _H	Hold Time, HIGH or LOW, A or B to LEBA or LEAB	2.0		ns	9
t _W	Pulse Width LOW LEBA or LEAB ^[8]	5.0		ns	5

Notes:

14. Minimum limits are specified but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.

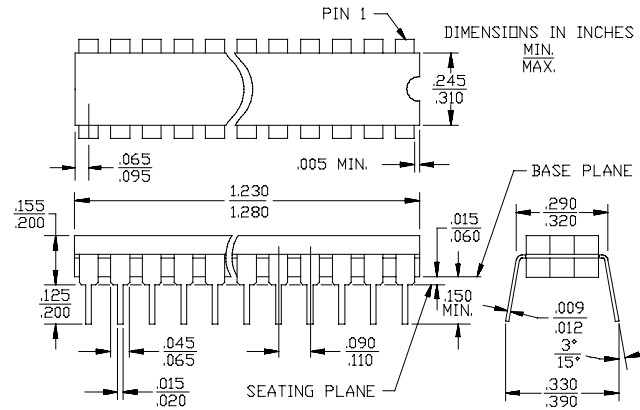
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.3	CY74FCT543CTQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT543CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
6.5	CY74FCT543ATQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT543ATSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
8.5	CY74FCT543TQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT543TSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY54FCT543TDMB	D14	24-Lead (300-Mil) CerDIP	Military

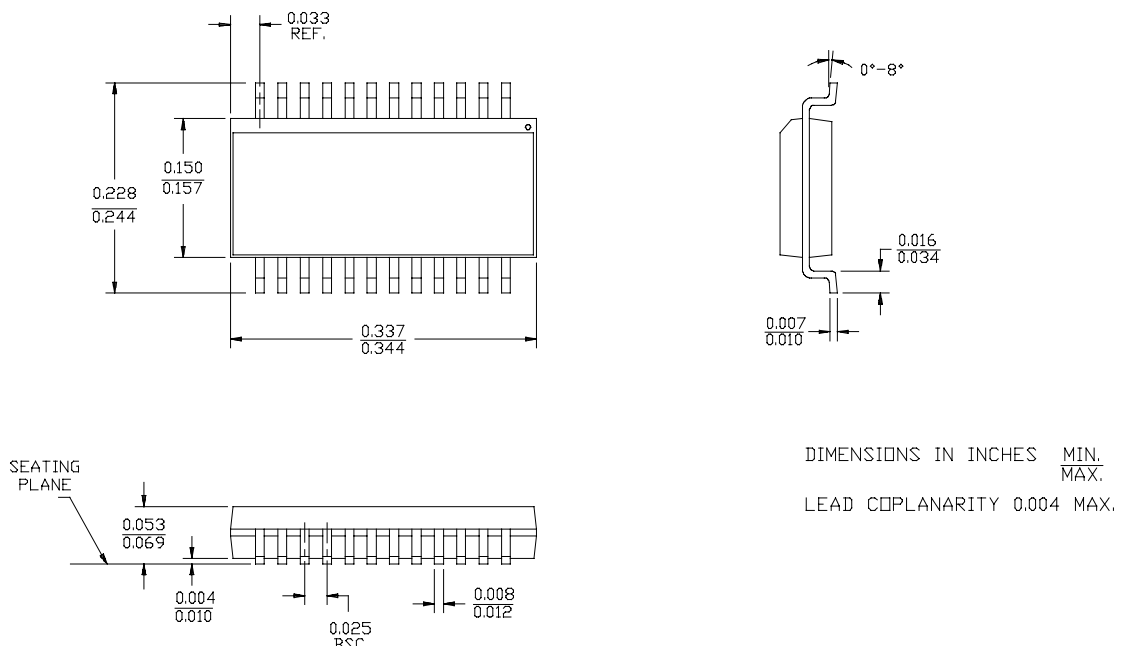
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Package Diagrams

24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D-9 Config.A

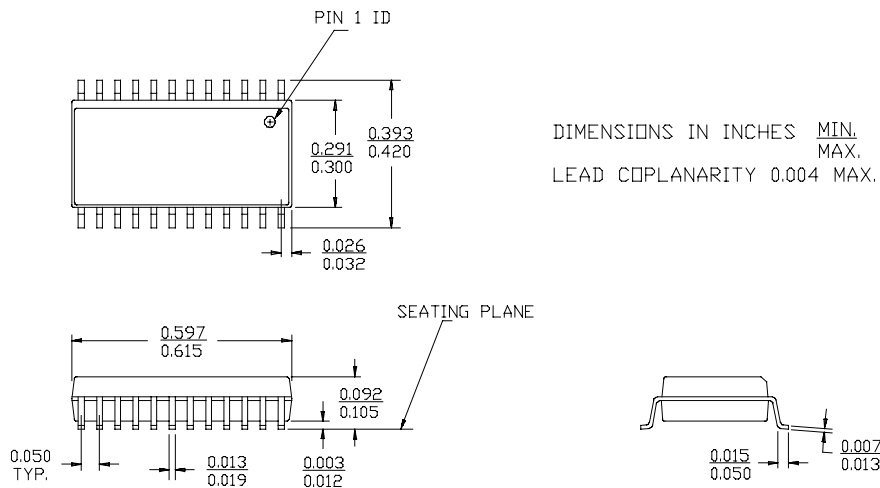


24-Lead Quarter Size Outline Q13



Package Diagrams (continued)

24-Lead (300-Mil) Molded SOIC S13



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