TEXAS INSTRUMENTS

# CY74FCT2543T

SCCS042 - September 1994 - Revised March 2000

# 8-Bit Latched Transceiver

## Features

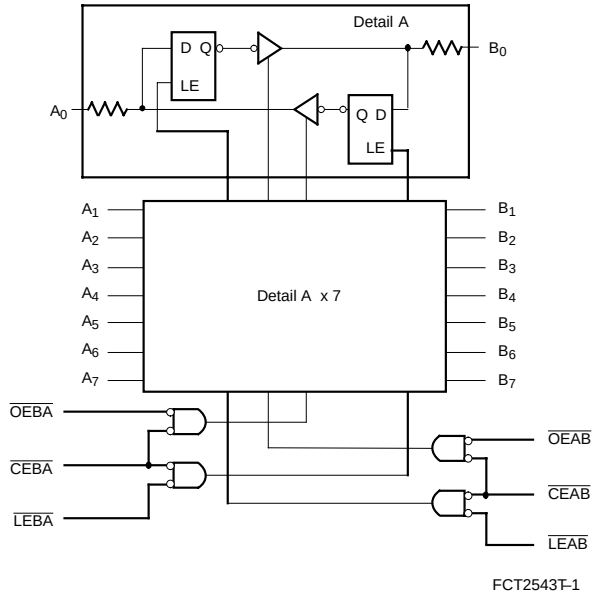
- **Function and pinout compatible with FCT and F logic**
- **FCT-C speed at 5.3 ns max.**
  **FCT-A speed at 6.5 ns max.**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced $V_{OH}$ (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 12 mA**
  **Source current 15 mA**
- **Separation controls for data flow in each direction**
- **Back to back latches for storage**
- **ESD > 2000V**
- **Extended commercial temp. range of –40˚C to +85˚C**

## Functional Description

The FCT2543T Octal Latched Tranceiver contains two sets of eight D-type latches. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) permits each latch set to have independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW to enter data from A or to take data from B, as indicated in the truth table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their output no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2543T can be used to replace the FCT543T to reduce noise in an existing design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

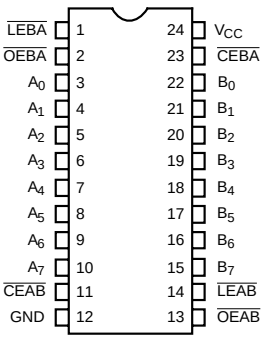
## Functional Block Diagram




FCT2543T–1

## Pin Configurations

**SOIC/QSOP**
**Top View**




FCT2543T–3

## Pin Description

| Name | Description |
|---|---|
| $\overline{OEAB}$ | A-to-B Output Enable Input (Active LOW) |
| $\overline{OEBA}$ | B-to-A Output Enable Input (Active LOW) |
| $\overline{CEAB}$ | A-to-B Enable Input (Active LOW) |
| $\overline{CEBA}$ | B-to-A Enable Input (Active LOW) |
| $\overline{LEAB}$ | A-to-B Latch Enable Input (Active LOW) |
| $\overline{LEBA}$ | B-to-A Latch Enable Input (Active LOW) |
| A | A-to-B Data Inputs or B-to-A Three-State Outputs |
| B | B-to-A Data Inputs or A-to-B Three-State Outputs |

## Function Table[1,2]

| Inputs | | | Latch | Outputs |
|---|---|---|---|---|
| $\overline{CEAB}$ | $\overline{LEAB}$ | $\overline{OEAB}$ | A-to-B[3] | B |
| H | X | X | Storing | High Z |
| X | H | X | Storing | X |
| X | X | H | X | High Z |
| L | L | L | Transparent | Current A Inputs |
| L | H | L | Storing | Previous A Inputs |

## Maximum Ratings[4,5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –65°C to +135°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage ..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... 120 mA

Power Dissipation ..... 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | –40°C to +85°C | 5V ± 5% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ.[7] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$=Min., $I_{OH}$=–15 mA | 2.4 | 3.3 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$=Min., $I_{OL}$=12 mA | | 0.3 | 0.55 | V |
| $R_{OUT}$ | Output Resistance | $V_{CC}$=Min., $I_{OL}$=12 mA | 20 | 25 | 40 | Ω |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $V_H$ | Hysteresis[8] | All inputs | | 0.2 | | V |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$=Min., $I_{IN}$=–18 mA | | –0.7 | –1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$=Max., $V_{IN}$=$V_{CC}$ | | | 5 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$=Max., $V_{IN}$=2.7V | | | ±1 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$=Max., $V_{IN}$=0.5V | | | ±1 | µA |
| $I_{OZH}$ | Off State HIGH-Level Output Current | $V_{CC}$=Max., $V_{OUT}$=2.7V | | | 15 | µA |
| $I_{OZL}$ | Off State LOW-Level Output Current | $V_{CC}$=Max., $V_{OUT}$=0.5V | | | –15 | µA |
| $I_{OS}$ | Output Short Circuit Current[9] | $V_{CC}$=Max., $V_{OUT}$=0.0V | –60 | –120 | –225 | mA |
| $I_{OFF}$ | Power-Off Disable | $V_{CC}$=0V, $V_{OUT}$=4.5V | | | ±1 | µA |

**Notes:**

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. A-to-B data flow shown: B-to-A is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
3. Before $\overline{LEAB}$ LOW-to-HIGH transition.
4. Unless otherwise noted, these limits are over the operating free-air temperature range.
5. Unused inputs must always be connected to an appropriate logic voltage level, preferably either $V_{CC}$ or ground.
6. $T_A$ is the "instant on" case temperature.

## Capacitance[8]

| Parameter | Description | Test Conditions | Typ.[7] | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 5 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 9 | 12 | pF |

## Power Supply Characteristics

| Parameter | Description | Test Conditions | Typ.[7] | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V | 0.1 | 0.2 | mA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs) | $V_{CC}$=Max., $V_{IN}$=3.4V,[10] $f_1$=0, Outputs Open | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[11] | $V_{CC}$=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V | 0.06 | 1.2 | mA/ MHz |
| $I_C$ | Total Power Supply Current[12] | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0$=$\overline{LEAB}$ =10 MHz, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V | 0.7 | 1.4 | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0$=$\overline{LEAB}$ =10 MHz, $V_{IN}$=3.4V or $V_{IN}$=GND | 1.2 | 3.4 | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0$=$\overline{LEAB}$ =10 MHz, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V | 2.8 | 5.6[13] | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $f_0$=$\overline{LEAB}$ =10 MHz, $V_{IN}$=3.4V or $V_{IN}$=GND | 5.1 | 14.6[13] | mA |

**Notes:**

7. Typical values are at $V_{CC}$=5.0V, $T_A$=+25°C ambient.
8. This parameter is specified but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.
10. Per TTL driven input ($V_{IN}$=3.4V); all other inputs at $V_{CC}$ or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    $I_{CC}$ = Quiescent Current with CMOS input levels
    $\Delta I_{CC}$ = Power Supply Current for a TTL HIGH input ($V_{IN}$=3.4V)
    $D_H$ = Duty Cycle for TTL inputs HIGH
    $N_T$ = Number of TTL inputs at $D_H$
    $I_{CCD}$ = Dynamic Current caused by an input transition pair (HLH or LHL)
    $f_0$ = Clock frequency for registered devices, otherwise zero
    $f_1$ = Input signal frequency
    $N_1$ = Number of inputs changing at $f_1$
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the $I_{CC}$ formula. These limits are specified but not tested.

## Switching Characteristics Over the Operating Range[14]

| Parameter | Description | CY74FCT2543T | | CY74FCT2543AT | | CY74FCT2543CT | | Unit | Fig. No.[15] |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Transparent Mode<br>A to B or B to A | 2.5 | 8.5 | 2.5 | 6.5 | 2.5 | 5.5 | ns | 1, 3 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{LEBA}$ to A $\overline{LEAB}$ to B | 2.5 | 12.5 | 2.5 | 8.0 | 2.5 | 7.0 | ns | 1, 5 |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>$\overline{OEBA}$ or $\overline{OEAB}$ to A or B<br>$\overline{CEBA}$ or $\overline{CEAB}$ to A or B | 2.0 | 12.0 | 2.0 | 9.0 | 2.0 | 8.0 | ns | 1, 7, 8 |
| $t_{PZH}$<br>$t_{PZL}$ | Output Disable Time<br>$\overline{OEBA}$ or $\overline{OEAB}$ to A or B<br>$\overline{CEBA}$ or $\overline{CEAB}$ to A or B | 2.0 | 9.0 | 2.0 | 7.5 | 2.0 | 6.5 | ns | 1, 7, 8 |
| $t_S$ | Set-Up Time HIGH or LOW,<br>A or B to $\overline{LEBA}$ or $\overline{LEAB}$ | 2.0 | | 2.0 | | 2.0 | | ns | 9 |
| $t_H$ | Hold Time HIGH or LOW,<br>A or B to $\overline{LEBA}$ or $\overline{LEAB}$ | 2.0 | | 2.0 | | 2.0 | | ns | 9 |
| $t_W$ | Pulse Width LOW<br>$\overline{LEBA}$ or $\overline{LEAB}$ | 5.0 | | 5.0 | | 5.0 | | ns | 5 |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 5.3 | CY74FCT2543CTQCT | Q13 | 24-Lead (150-Mil) QSOP | Commercial |
| | CY74FCT2543CTSOC/SOCT | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 6.5 | CY74FCT2543ATQCT | Q13 | 24-Lead (150-Mil) QSOP | Commercial |
| | CY74FCT2543ATSOC/SOCT | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 8.5 | CY74FCT2543TQCT | Q13 | 24-Lead (150-Mil) QSOP | Commercial |

**Notes:**
14. Minimum limits are specified but not tested on Propagation Delays.
15. See “Parameter Measurement Information” in the General Information section.

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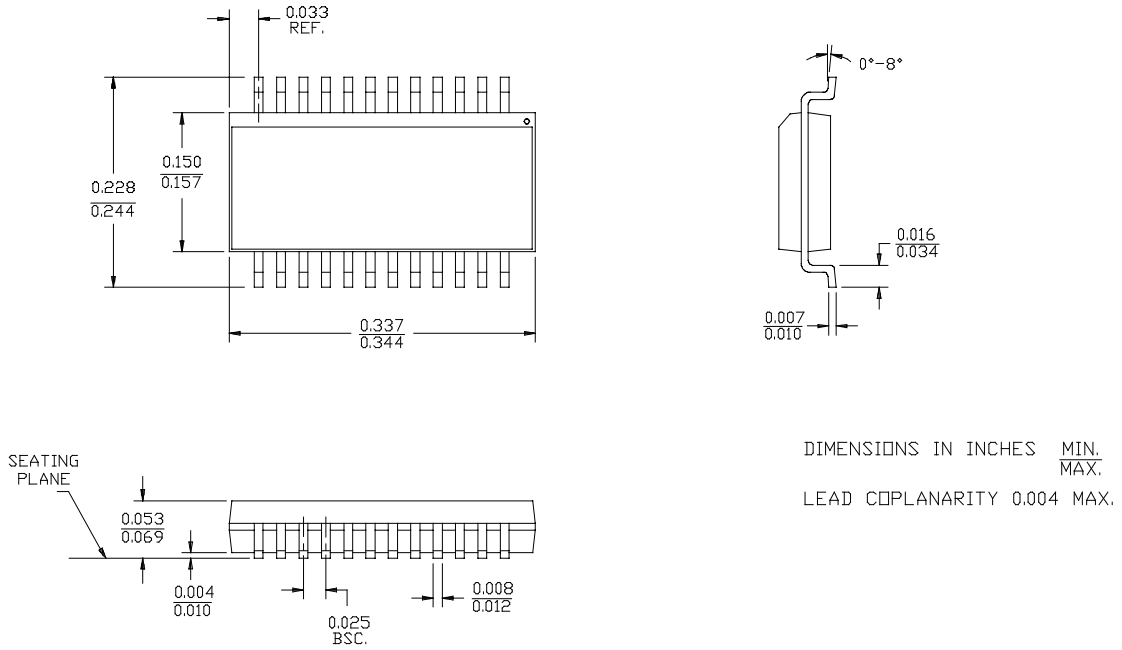
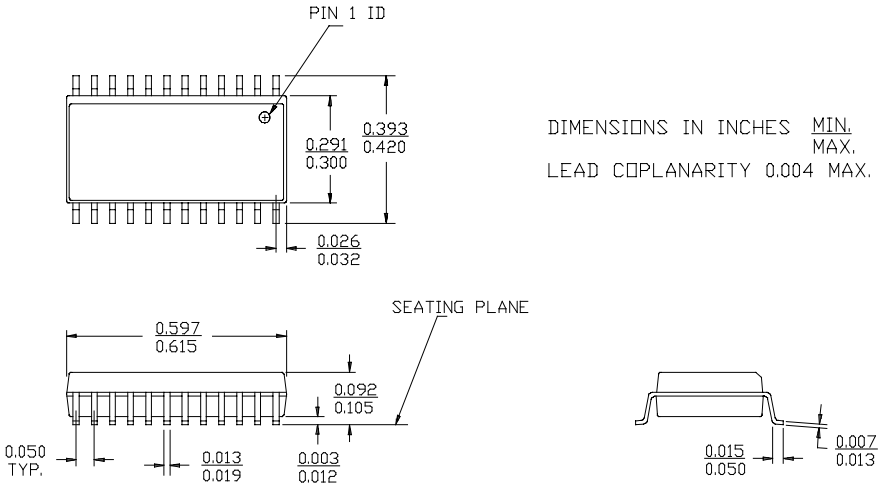
## Package Diagrams

**24-Lead Quarter Size Outline Q13**




**24-Lead (300-Mil) Molded SOIC S13**



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