

# SN54ABTH162460, SN74ABTH162460 4-TO-1 MULTIPLEXED/DEMULPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus™* Family
- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

The 'ABTH162460 are 4-bit to 1-bit multiplexed registered transceivers used in applications where four separate data paths must be multiplexed onto or demultiplexed from a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device also is useful in memory-interleaving applications.

Five 4-bit I/O ports (1A–4A, 1B1–4, 2B1–4, 3B1–4, and 4B1–4) are available for address and/or data transfer. The output-enable ( $\overline{\text{OEB}}$ ,  $\overline{\text{OEB1}}\text{--}\overline{\text{OEB4}}$ , and  $\overline{\text{OEA}}$ ) inputs control the bus-transceiver functions. These control signals also allow 4-bit or 16-bit control, depending on the  $\overline{\text{OEB}}$  level.

SN54ABTH162460 . . . WD PACKAGE  
SN74ABTH162460 . . . DL PACKAGE  
(TOP VIEW)

LEAB1	1	56	$\overline{\text{OEB1}}$
LEAB2	2	55	$\overline{\text{OEB2}}$
LEBA	3	54	SEL0
GND	4	53	GND
LEB1	5	52	1B1
LEB2	6	51	1B2
$V_{CC}$	7	50	$V_{CC}$
CLKBA	8	49	1B3
$\overline{\text{OEB}}$	9	48	1B4
CLKAB	10	47	2B1
GND	11	46	GND
1A	12	45	2B2
2A	13	44	2B3
CE_SEL0	14	43	2B4
CE_SEL1	15	42	3B1
3A	16	41	3B2
4A	17	40	3B3
GND	18	39	GND
CLKENAB	19	38	3B4
CLKENB	20	37	4B1
CLKENBA	21	36	4B2
$V_{CC}$	22	35	$V_{CC}$
LEB3	23	34	4B3
LEB4	24	33	4B4
GND	25	32	GND
$\overline{\text{OEA}}$	26	31	SEL1
LEAB3	27	30	$\overline{\text{OEB3}}$
LEAB4	28	29	$\overline{\text{OEB4}}$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

# SN54ABTH162460, SN74ABTH162460 4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

## description (continued)

Address and/or data information can be stored using the internal storage latches/flip-flops. The latch-enable (LEB1–LEB4, LEBA, and LEAB1–LEAB4) and clock/clock-enable (CLK/CLKEN) inputs are used to control data storage. When either one of the latch-enable inputs is high, the latch is transparent (clock is a don't care as long as the latch enable is high). When the latch-enable input goes low (providing that the clock does not transit from low to high), the data present at the inputs is latched and remains latched until the latch-enable input is returned high. When the clock enable is low and the corresponding latch enable is low, data can be clocked on the low-to-high transition of the clock. When either the clock enable or the corresponding latch enable is high, the clock is a don't care.

Four select (SEL0, SEL1, CE\_SEL0, and CE\_SEL1) pins are provided to multiplex data (A port), or to select one of four clock enables (B port). This allows the user the flexibility of controlling one bit at a time.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH162460 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABTH162460 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### Function Tables

A-TO-B OUTPUT ENABLE†

INPUTS		OUTPUT
$\overline{OEB}$	$\overline{OEBn}$	$Bn$
H	H	Z
H	L	Z
L	H	Z
L	L	Active

†  $n = 1, 2, 3, 4$

A-TO-B STORAGE  
(assuming  $\overline{OEB} = L$ ,  $\overline{OEBn} = L$ )‡

INPUTS								OUTPUTS			
$\overline{CLKENAB}$	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	H or L	H	L	L	L	A	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>
X	X	X	H or L	H	H	H	L	A	A	A	A <sub>0</sub>
L	X	X	L	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>
L	L	L	↑	L	L	L	L	A	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>
L	L	H	↑	L	L	L	L	A <sub>0</sub>	A	A <sub>0</sub>	A <sub>0</sub>
L	H	L	↑	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A	A <sub>0</sub>
L	H	H	↑	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>	A
H	X	X	↑	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>

‡ This table does not cover all the latch-enable cases since they have similar results.



SN54ABTH162460, SN74ABTH162460  
**4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS  
 WITH 3-STATE OUTPUTS**

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

**Function Tables (Continued)**

**B-TO-A STORAGE  
 (before point P)**

INPUTS								P		
CLKENB	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0			
X	X	H	L	L	L	L	L	B1		
X	X	L	H	L	L	L	H	B2		
X	X	L	L	H	L	H	L	B3		
X	X	L	L	L	H	H	H	B4		
L							↑	L	L	B1
								L	H	B2
								H	L	B3
								H	H	B4
L								L	L	B1 <sup>†</sup>
								L	H	B2 <sup>†</sup>
								H	L	B3 <sup>†</sup>
								H	H	B4 <sup>†</sup>

† Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE  
 (after point P)**

INPUTS					OUTPUT
CLKENB	CLKBA	LEBA	OEA	B	A
X	X	X	H	X	Z
X	X	H	L	L	L
X	X	H	L	H	H
H	X	L	L	X	A <sub>0</sub> <sup>†</sup>
L	↑	L	L	L	L
L	↑	L	L	H	H
L	L	L	L	X	A <sub>0</sub> <sup>†</sup>

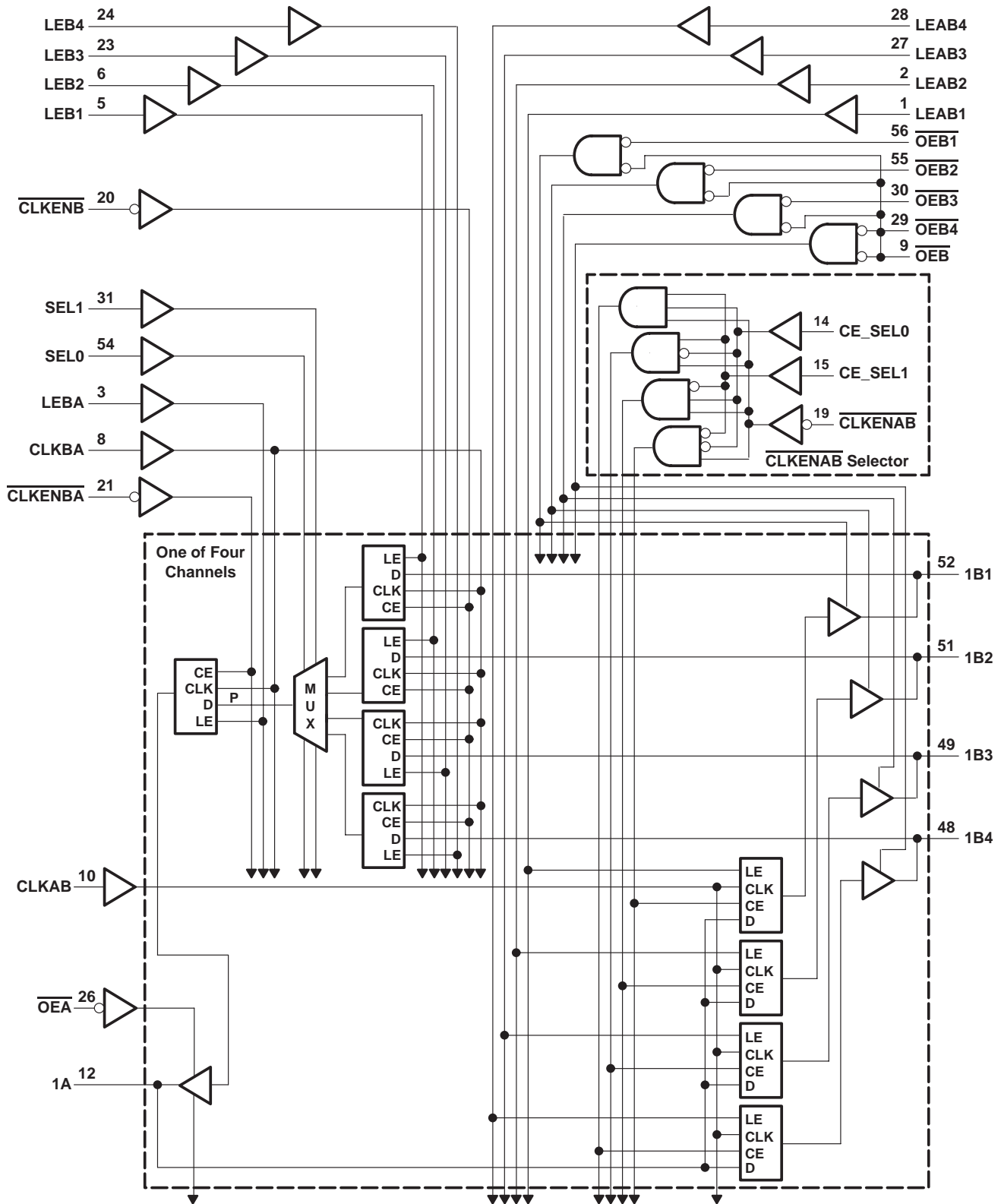
† Output level before the indicated steady-state input conditions were established

# SN54ABTH162460, SN74ABTH162460

## 4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCIEVERS WITH 3-STATE OUTPUTS

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

### logic diagram (positive logic)



# SN54ABTH162460, SN74ABTH162460 4-TO-1 MULTIPLEXED/DEMULPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_{O1}$ : SN54ABTH162460 (A port) .....	96 mA
SN74ABTH162460 (A port) .....	128 mA
B port .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DL package .....	74 °C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABTH162460			SN74ABTH162460			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$	High-level output current	A port		–24	B port		–32	mA
		B port		–12	A port		–12	
$I_{OL}$	Low-level output current	A port		48	B port		64	mA
		B port		12	A port		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			µs/V
$T_A$	Operating free-air temperature	–55	125		–40	85		°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54ABTH162460, SN74ABTH162460

## 4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ABTH162460			SN74ABTH162460			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$	-1.2			-1.2			V	
$V_{OH}$	A port	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$	3	3.4	3	3.4	V		
		$V_{CC} = 4.5\text{ V}$	2.5	3					
	B port	$V_{CC} = 5\text{ V}$ , $I_{OH} = -1\text{ mA}$	3.8	4.2	3.85				
		$V_{CC} = 4.5\text{ V}$	3.3	3.7	3.35				
		$I_{OH} = -3\text{ mA}$	3	3.6	3.1				
		$I_{OH} = -12\text{ mA}$			2.6				
$V_{OL}$	A port	$V_{CC} = 4.5\text{ V}$		0.25	0.55		V		
		$I_{OL} = 24\text{ mA}$				0.3		0.55	
	B port	$V_{CC} = 4.5\text{ V}$		0.4	0.8	0.4		0.65	
		$I_{OL} = 12\text{ mA}$				0.5		0.8	
$V_{hys}$		100			100			mV	
$I_I$	Control inputs	$V_{CC} = 0\text{ to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$	$\pm 1$			$\pm 1$			$\mu\text{A}$
	A or B ports	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$	$\pm 20$			$\pm 20$			$\mu\text{A}$
$I_I(\text{hold})$	A or B ports	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.8\text{ V}$	75	500	75	500	$\mu\text{A}$		
		$V_{CC} = 4.5\text{ V}$ , $V_I = 2\text{ V}$	-75	-500	-75	-500			
$I_{O\ddagger}$	A port	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-50	-110	-180	-50	-180	mA	
	B port	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-25	-55	-90	-25	-90		
		$V_O = 0$	-50	-110	-180	-50	-180		
$I_{CEX}$	Outputs high	$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$	50			50			$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or }V_O \leq 4.5\text{ V}$	$\pm 100$			$\pm 100$			$\mu\text{A}$
$I_{OZPU}\S$		$V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$	$\pm 50$			$\pm 50$			$\mu\text{A}$
$I_{OZPD}\S$		$V_{CC} = 2.1\text{ V to }0$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$	$\pm 50$			$\pm 50$			$\mu\text{A}$
$I_{CC}$	Outputs high	$V_{CC} = 5.5\text{ V}$ , Outputs open	1.5			0.7	1.5	mA	
	A port low		10			6	10		
	B port low		32			18	32		
	Outputs disabled		1.5			0.7	1.5		
$\Delta I_{CC}\P$		$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND	1			1			mA
$C_i$	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$	3.5			3.5			pF
$C_{iO}$	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$	8			8			pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This parameter is characterized but not production tested.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54ABTH162460, SN74ABTH162460 4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Figure 1)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABTH162460		SN74ABTH162460		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	160	0	160	0	160	MHz
t <sub>w</sub>	Pulse duration	CLKAB high or low	3.8	3.8	3.8	3.8	3.8	ns
		CLKBA high or low	4.5	4.5	4.5	4.5		
		LEAB1, 2, 3, or 4 high	2.8	2.8	2.8	2.8		
		LEBA high	2.8	2.8	2.8	2.8		
		LEB1, 2, 3, or 4 high	3	3	3	3		
t <sub>su</sub>	Before CLKAB↑	A bus	2.5	2.5	2.5	2.5	ns	
		CE_SEL0/1	3.2	3.2	3.2	3.2		
		$\overline{\text{CLKENAB}}$	3.2	3.2	3.2	3.2		
	Before LEAB1, 2, 3, or 4↓	A bus	3.6	3.6	3.6	3.6		
		Before CLKBA↑	B bus	3.8	3.8	3.8		3.8
			$\overline{\text{CLKENB}}$	2.3	2.3	2.3		2.3
	$\overline{\text{CLKENBA}}$		2.5	2.5	2.5	2.5		
	Before LEB1, 2, 3, or 4	LEB1, 2, 3, or 4	4.3	4.3	4.3	4.3		
		SEL0/1	4.5	4.5	4.5	4.5		
		Before LEB1, 2, 3, or 4↓	B bus	3.2	3.2	3.2		3.2
	Before LEBA↓		B bus	4	4	4		4
			LEB1, 2, 3, or 4	4.4	4.4	4.4		4.4
SEL0/1		4.3	4.3	4.3	4.3			
t <sub>h</sub>	After CLKAB↑	A bus	0.5	0.5	0.5	0.5	ns	
		CE_SEL0/1	1.1	1.1	1.1	1.1		
		$\overline{\text{CLKENAB}}$	0.5	0.5	0.5	0.5		
	After LEAB1, 2, 3, or 4↓	A bus	1.2	1.2	1.2	1.2		
		After CLKBA↑	B bus	1.3	1.3	1.3		1.3
			$\overline{\text{CLKENB}}$	1	1	1		1
	$\overline{\text{CLKENBA}}$		1	1	1	1		
	SEL0/1	0	0	0	0			
	After LEB1, 2, 3, or 4↓	B bus	1.5	1.5	1.5	1.5		
		After LEBA↓	B bus	0.4	0.4	0.4		0.4
			SEL0/1	0.1	0.1	0.1		0.1

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54ABTH162460, SN74ABTH162460**  
**4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABTH162460		SN74ABTH162460		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			160			160		160		MHz
$t_{PLH}$	B	A	2	3.6	5.9	2	7.1	2	6.5	ns
$t_{PHL}$			2	3.5	5.8	2	6.8	2	6.5	
$t_{PZH}$	$\overline{OEA}$	A	1.5	2.8	4.8	1.5	5.9	1.5	5.6	ns
$t_{PZL}$			1.5	2.6	4.8	1.5	5.7	1.5	5.5	
$t_{PHZ}$	$\overline{OEA}$	A	2	3.8	5.3	2	6	2	5.9	ns
$t_{PLZ}$			1.5	4	6.1	1.5	7	1.5	6.5	
$t_{PLH}$	A	B	2	3.3	5.5	2	6.5	2	6.2	ns
$t_{PHL}$			2	3.7	5.8	2	6.8	2	6.5	
$t_{PZH}$	$\overline{OEB}$	B	2	3.9	5.8	2	7.1	2	6.8	ns
$t_{PZL}$			2	3.7	5.6	2	6.6	1.5	6.3	
$t_{PHZ}$	$\overline{OEB}$	B	2	4	5.6	2	6.4	2	6.2	ns
$t_{PLZ}$			2	3.7	5.2	2	6.1	2	5.8	
$t_{PZH}$	$\overline{OEB1}, \overline{2}, \overline{3}, \overline{4}$	B	2	3.7	5.8	2	6.8	2	6.6	ns
$t_{PZL}$			2	3.5	5.4	2	6.4	2	6.2	
$t_{PHZ}$	$\overline{OEB1}, \overline{2}, \overline{3}, \overline{4}$	B	1.5	3.3	4.8	1.5	5.4	1.5	5.3	ns
$t_{PLZ}$			1.5	3.1	4.4	1.5	5.1	1.5	4.9	
$t_{PLH}$	CLKBA	A	1.5	4.2	6.7	1.5	8.1	1.5	7.4	ns
$t_{PHL}$			1.5	4.4	6.9	1.5	8.4	1.5	7.7	
$t_{PLH}$	CLKAB	B	2	3.5	5.8	2	6.9	2	6.5	ns
$t_{PHL}$			2	3.7	6	2	7	2	6.5	
$t_{PLH}$	LEBA	A	1.5	3	5.2	1.5	6.3	1.5	5.8	ns
$t_{PHL}$			1.5	3	5	1.5	6.3	1.5	5.8	
$t_{PLH}$	LEAB1, 2, 3, 4	B	2	3.4	5.4	2	6.5	2	6.2	ns
$t_{PHL}$			2	3.6	5.7	2	6.3	2	6.2	
$t_{PLH}$	LEBA1, 2, 3, 4	A	2	4	6.5	2	7.8	2	7.2	ns
$t_{PHL}$			2	4	6.1	2	7.5	2	6.8	
$t_{PLH}$	SEL	A	2	4.1	6.7	2	8.1	2	7.5	ns
$t_{PHL}$			2	3.8	6.2	2	7.3	2	6.9	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



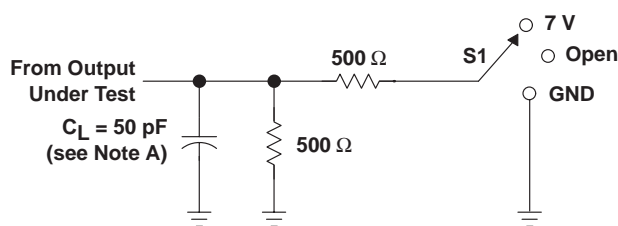
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



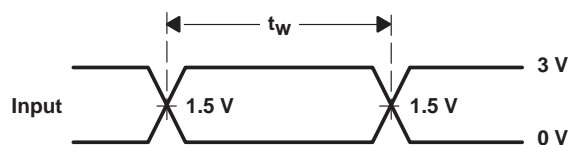
# SN54ABTH162460, SN74ABTH162460 4-TO-1 MULTIPLEXED/DEMULPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS241E – FEBRUARY 1993 – REVISED MAY 1997

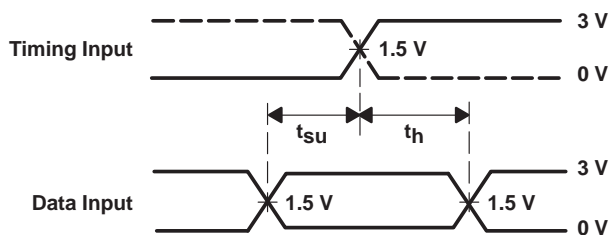
## PARAMETER MEASUREMENT INFORMATION



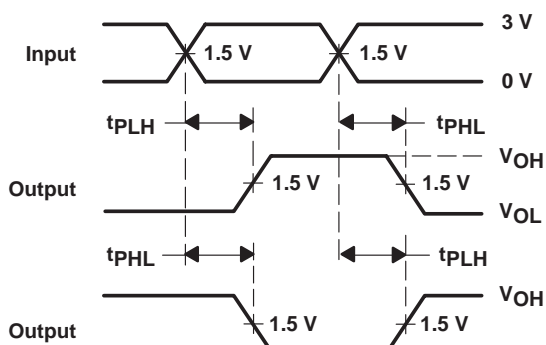
LOAD CIRCUIT



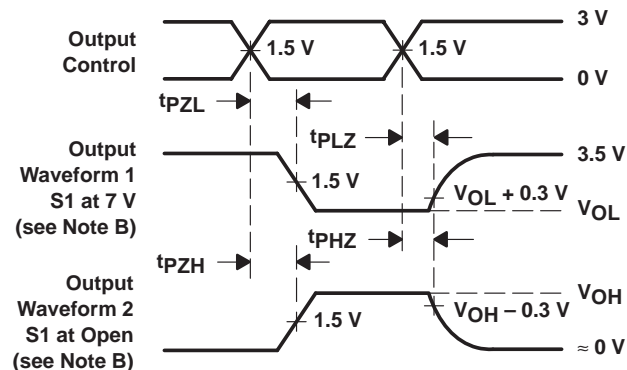
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

**CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.**

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.