

# SN74ALVCH16524

## 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES080C – JULY 1996 – REVISED FEBRUARY 1999

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

### description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ) and clock-enable ( $\overline{CLKENBA}$ ) inputs. For the A-to-B data flow, the data flows through a single buffer. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select ( $\overline{SEL}$ ) input.

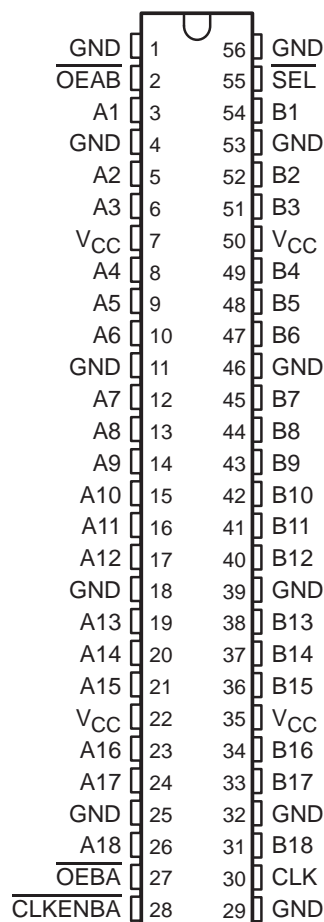
Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate  $\overline{CLKENBA}$  input is low. The B-to-A data transfer is synchronized with CLK.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16524 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DGG OR DL PACKAGE  
(TOP VIEW)



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INSTRUMENTS**

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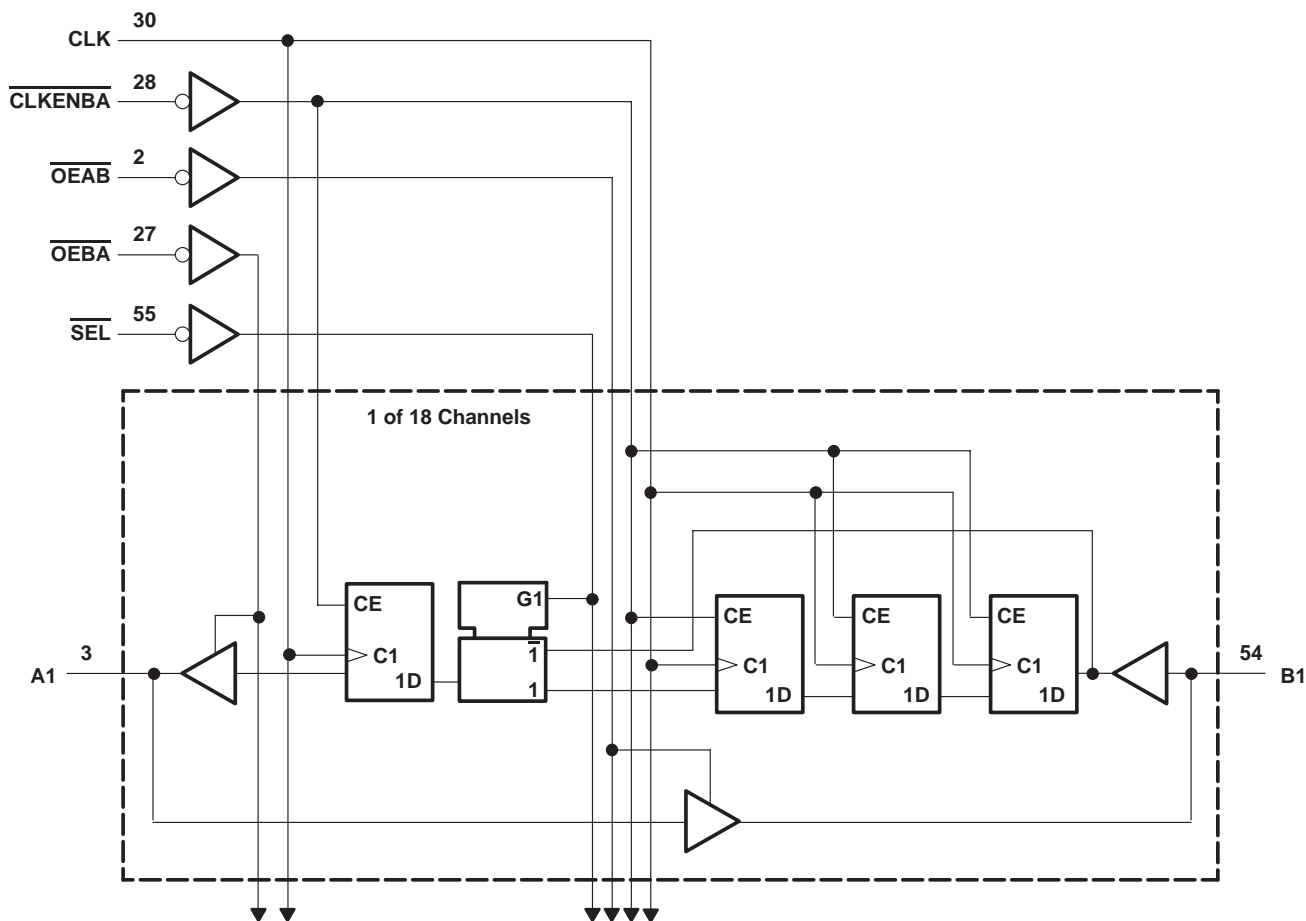
**FUNCTION TABLE**  
**B-TO-A STORAGE (OEBA = L)**

INPUTS				OUTPUT
CLKENBA	CLK	SEL	B	A
H	X	X	X	A <sub>0</sub> <sup>†</sup>
L	↑	H	L	L
L	↑	H	H	H
L	↑	L	L	L <sup>‡</sup>
L	↑	L	H	H <sup>‡</sup>

<sup>†</sup> Output level before the indicated steady-state input conditions were established

<sup>‡</sup> Four positive CLK edges are needed to propagate data from B to A when SEL is low.

#### logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1) .....	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through each $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	81°C/W
DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
		$V_{CC} = 2.7$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 2.7$ V to 3.6 V	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65$ V	–4	mA
		$V_{CC} = 2.3$ V	–12	
		$V_{CC} = 2.7$ V	–12	
		$V_{CC} = 3$ V	–24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65$ V	4	mA
		$V_{CC} = 2.3$ V	12	
		$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -6 mA	2.3 V	2			
	I <sub>OH</sub> = -12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
I <sub>OH</sub> = -24 mA	3 V	2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 6 mA	2.3 V			0.4	
	I <sub>OL</sub> = 12 mA	2.3 V			0.7	
		2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.58 V	1.65 V	25			μA
	V <sub>I</sub> = 1.07 V	1.65 V	-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V	2.3 V	-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	-75			
	V <sub>I</sub> = 0 to 3.6 V‡	3.6 V			±500	
I <sub>OZ</sub> §	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3	pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		7	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

		V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	¶		120		125		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	¶		3.2		3.2		3		ns
t <sub>su</sub>	Setup time	B data before CLK↑		¶		1.5		1.2		ns
		SEL before CLK↑		¶		2.7		2.4		
		CLKENBA before CLK↑		¶		2.7		2.6		
t <sub>h</sub>	Hold time	B data after CLK↑		¶		1		0.6		ns
		SEL after CLK↑		¶		0.5		0.2		
		CLKENBA after CLK↑		¶		0.1		0.1		

¶ This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			†		120		125		150		MHz
t <sub>pd</sub>	A	B		†	1	3.9		3.8	1	3.2	ns
	CLK	A		†	1	6.1		6.2	1	5.2	
t <sub>en</sub>	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B		†	1	6.1		6.1	1	5.1	ns
t <sub>dis</sub>	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B		†	1	6.3		5.4	1	4.9	ns

† This information was not available at the time of publication.

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 50 pF, f = 10 MHz	†	160	160	pF
		Outputs disabled		†	160	160	

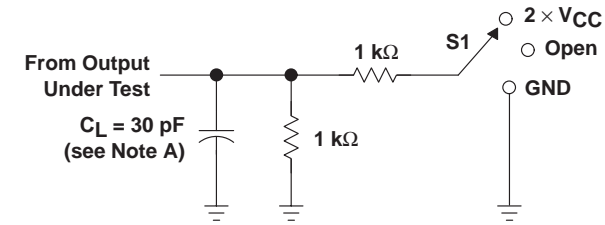
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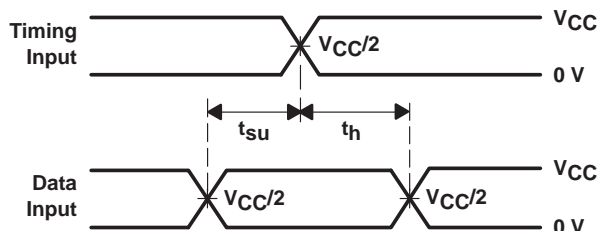
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**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 1.8\text{ V}$

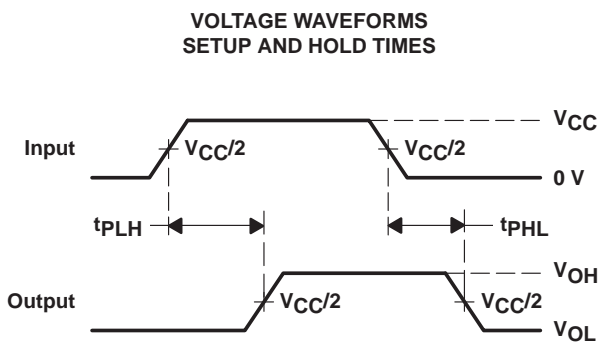


**LOAD CIRCUIT**

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

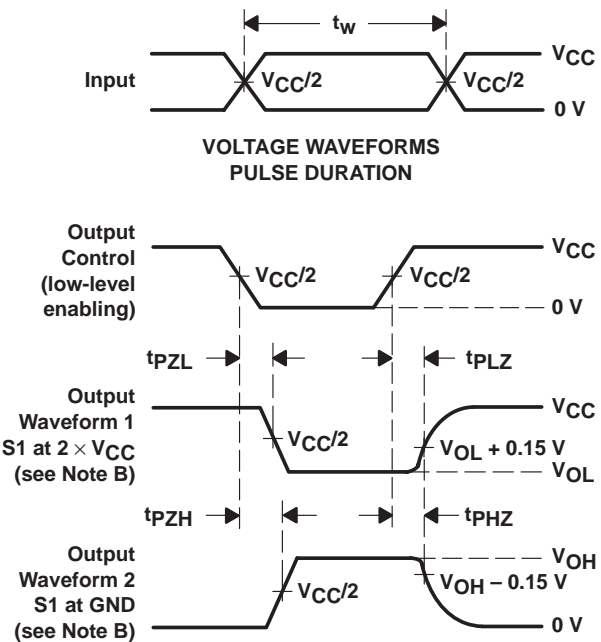


**VOLTAGE WAVEFORMS PULSE DURATION**



**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

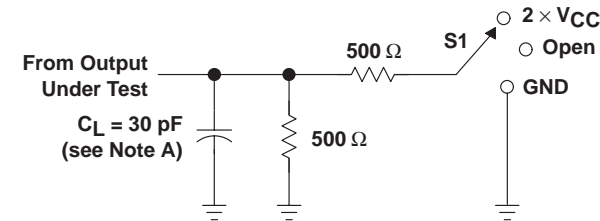


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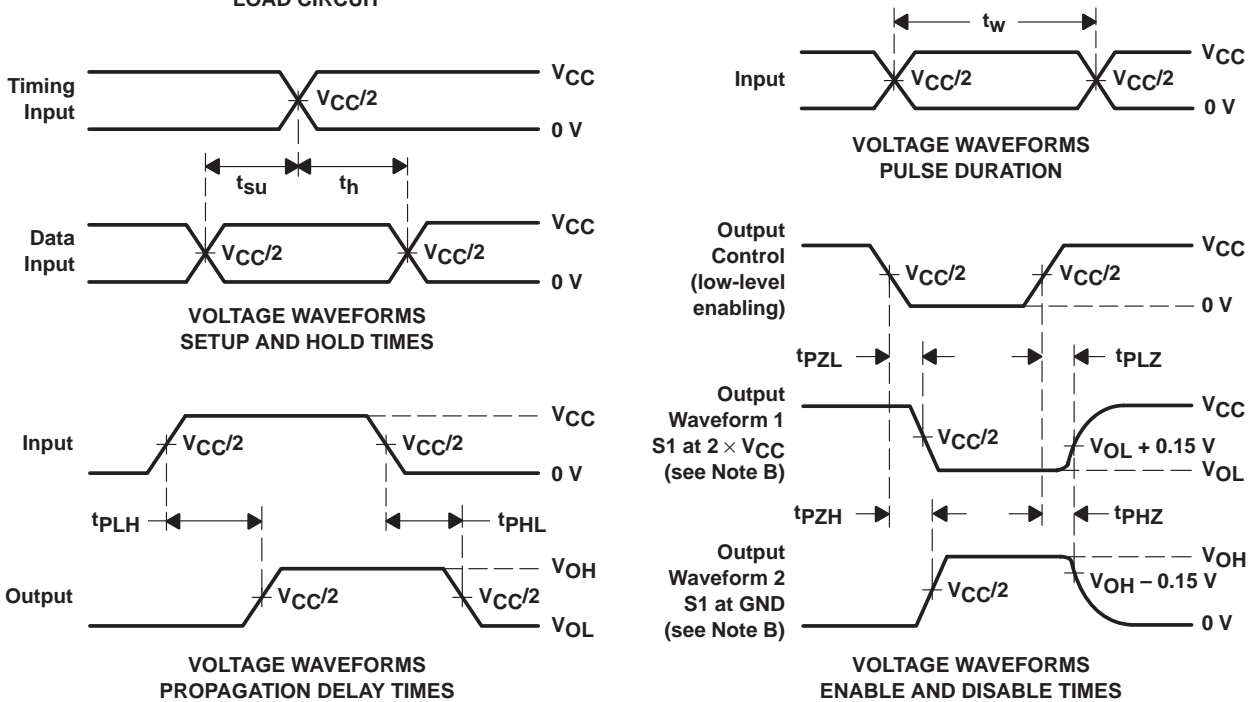
## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



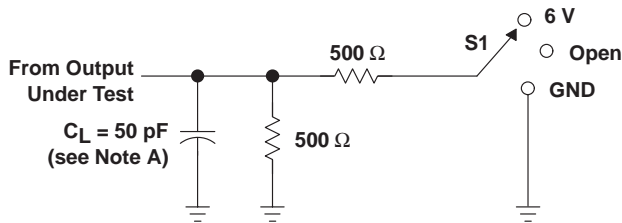
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

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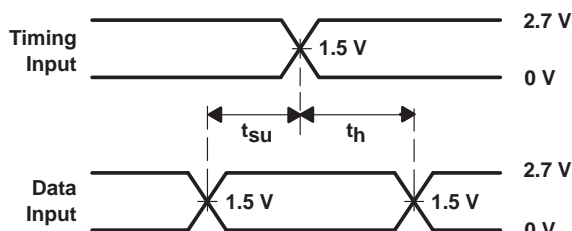
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**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

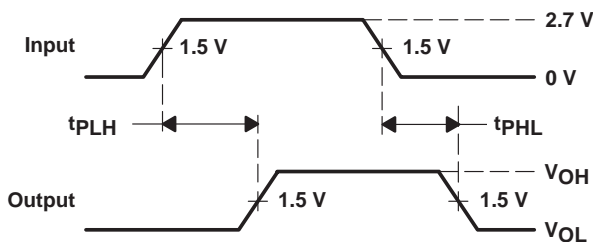


TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

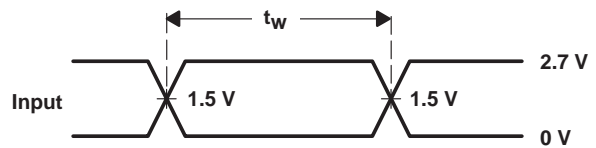
**LOAD CIRCUIT**



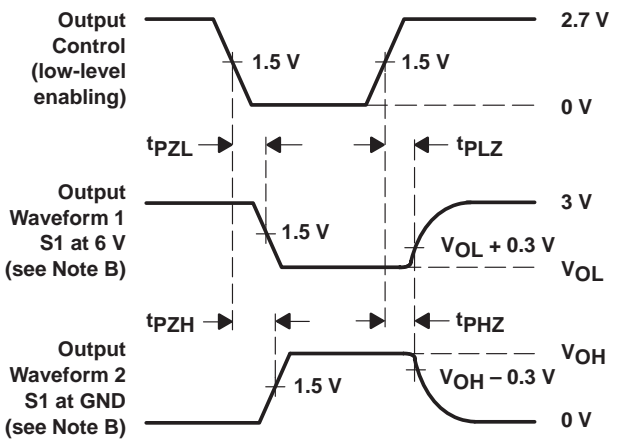
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



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 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**





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