

SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS706D – AUGUST 1997 – REVISED APRIL 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

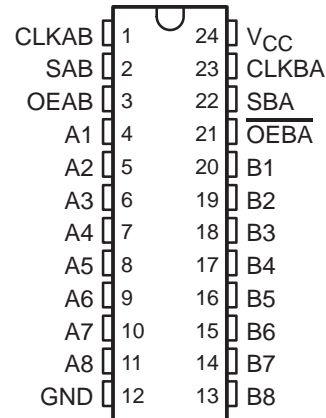
description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

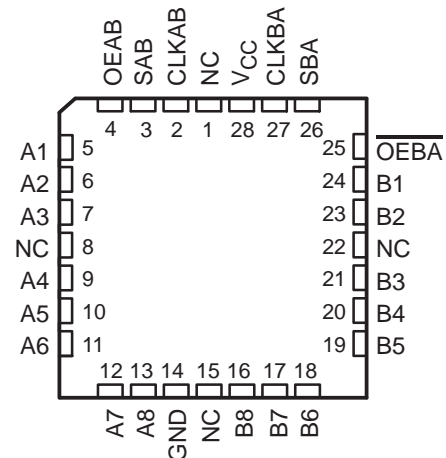
The 'LVTH652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input selects real-time data and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH652 devices.

SN54LVTH652 . . . JT OR W PACKAGE
SN74LVTH652 . . . DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH652 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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**TEXAS
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description (continued)

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input; therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH652 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH652 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

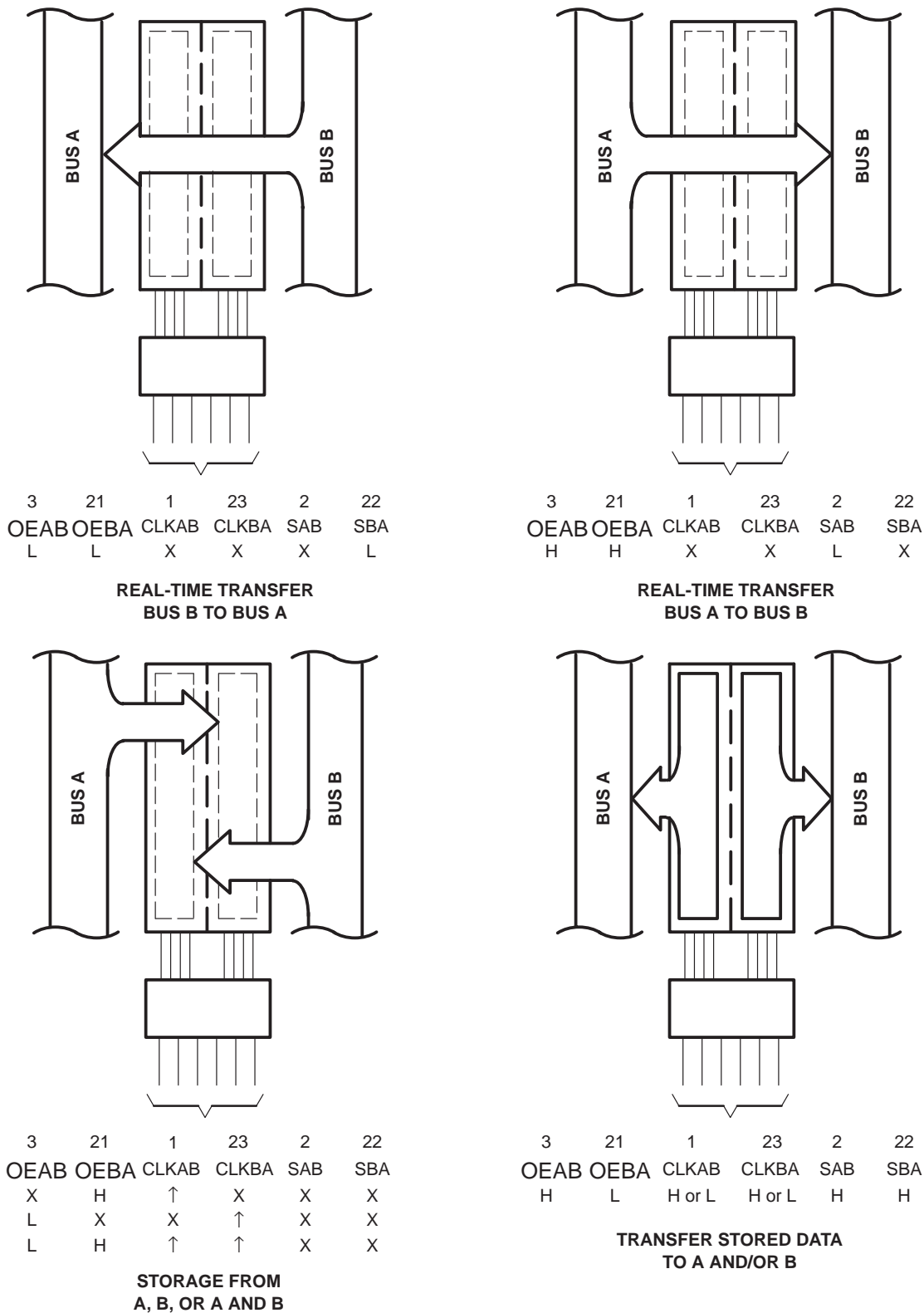
‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.



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Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

Figure 1. Bus-Management Functions

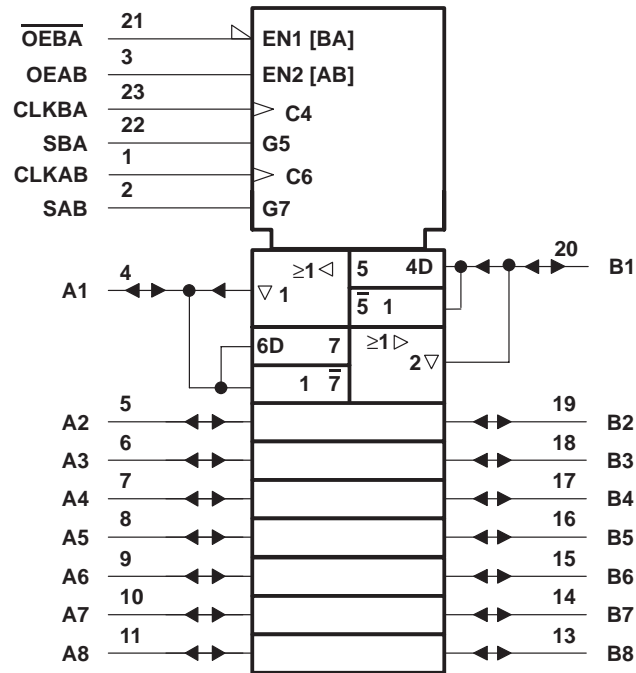
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logic symbol†

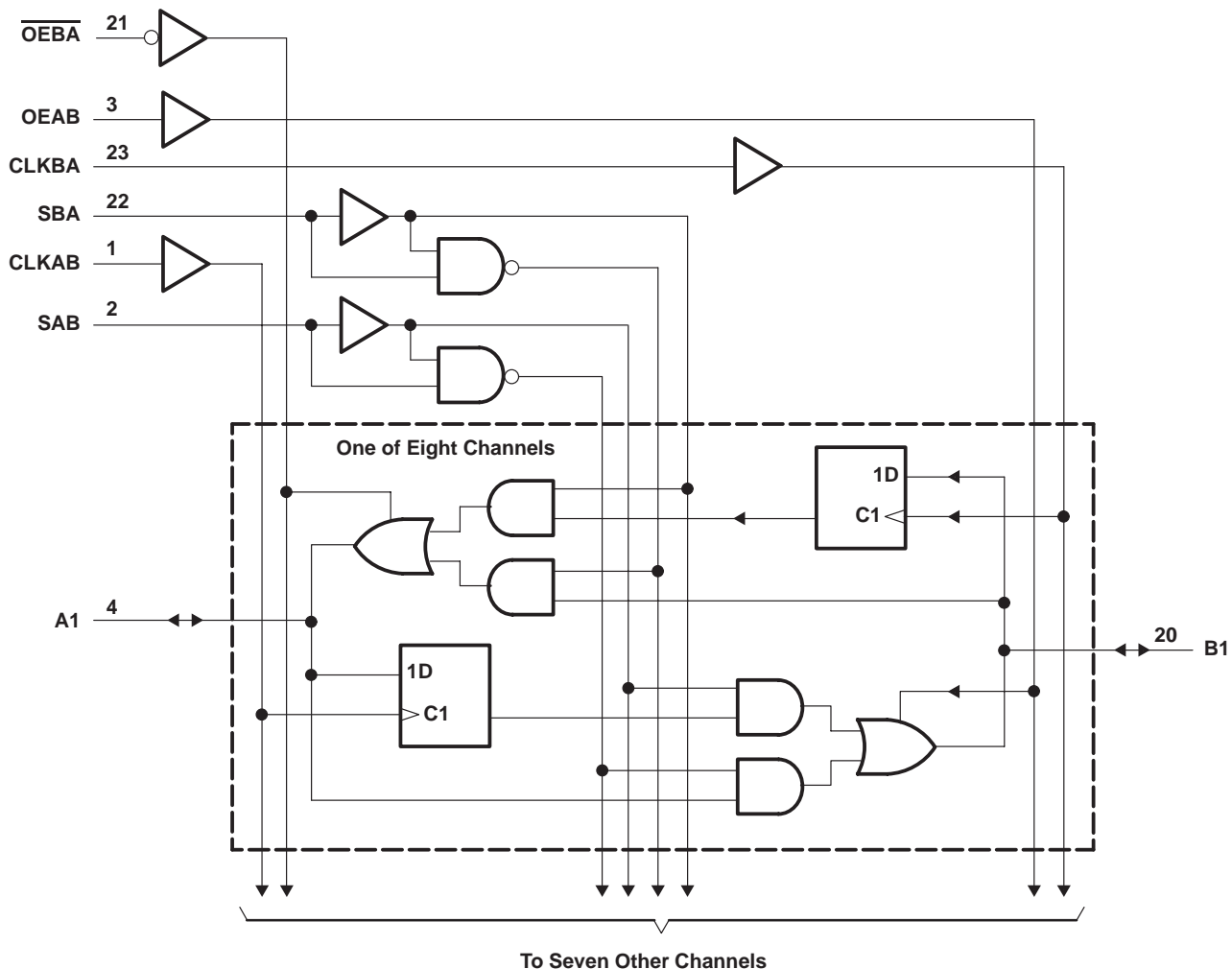


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH652	96 mA
SN74LVTH652	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH652	48 mA
SN74LVTH652	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH652		SN74LVTH652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH652		SN74LVTH652		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V		
V_{OH}		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V		
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4				
		$V_{CC} = 3\text{ V}$		$I_{OH} = -24\text{ mA}$		2			$I_{OH} = -32\text{ mA}$	
V_{OL}		$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		
				$I_{OL} = 24\text{ mA}$		0.5		0.5		
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4		0.4		
				$I_{OL} = 32\text{ mA}$		0.5		0.5		
				$I_{OL} = 48\text{ mA}$		0.55		0.55		
				$I_{OL} = 64\text{ mA}$				0.55		
I_I		Control inputs $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		± 1		± 1		μA		
				$V_{CC} = 0$ or 3.6 V , $V_I = 5.5\text{ V}$		10			10	
		A or B ports‡ $V_{CC} = 3.6\text{ V}$		$V_I = 5.5\text{ V}$		20			20	
				$V_I = V_{CC}$		1			1	
		$V_I = 0$		-5		-5				
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA		
$I_I(\text{hold})$		$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75		75		
				$V_I = 2\text{ V}$		-75		-75		
		$V_{CC} = 3.6\text{ V}\S$		$V_I = 0$ to 3.6 V				± 500		
I_{OZPU}		$V_{CC} = 0$ to 1.5 V , $V_O = 0.5$ to 3 V , OE/OE = don't care		$\pm 100^*$		± 100		μA		
I_{OZPD}		$V_{CC} = 1.5\text{ V}$ to 0 , $V_O = 0.5$ to 3 V , OE/OE = don't care		$\pm 100^*$		± 100		μA		
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		0.19		0.19		
				Outputs low		5		5		
				Outputs disabled		0.19		0.19		
$\Delta I_{CC}\P$		$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND		0.2		0.2		mA		
C_i		$V_I = 3\text{ V}$ or 0		4		4		pF		
C_{io}		$V_O = 3\text{ V}$ or 0		9		9		pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN54LVTH652				SN74LVTH652				UNIT
		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	150		150		150		150		MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB \uparrow or CLKBA \uparrow	Data high	1.3	1.6	1.2	1.5			ns	
		Data low	1.9	2.6	1.6	2.2				
t_h	Hold time, A or B after CLKAB \uparrow or CLKBA \uparrow	1.2		1.2		0.8		0.8		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH652				SN74LVTH652				UNIT	
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$			
			MIN	MAX	MIN	MAX	MIN	TYP \dagger	MAX	MIN		MAX
f_{max}			150		150			150			150	MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.7	5		5.9	1.8	3.1	4.7		5.6	ns
t_{PHL}			1.7	5		5.9	1.8	3.1	4.7		5.6	
t_{PLH}	A or B	B or A	1.2	3.7		4.3	1.3	2.3	3.5		4.1	ns
t_{PHL}			1.2	3.7		4.3	1.3	2.4	3.5		4.1	
t_{PLH}	SBA or SAB \ddagger	A or B	1.4	5.2		6.3	1.5	3.1	4.9		6	ns
t_{PHL}			1.4	5.2		6.3	1.5	3.4	4.9		6	
t_{PZH}	\overline{OEBA}	A	1	5.4		6.7	1.1	2.9	5.2		6.5	ns
t_{PZL}			1	5.4		6.7	1.1	3.1	5.2		6.5	
t_{PHZ}	\overline{OEBA}	A	2.2	5.9		6.5	2.3	3.5	5.5		6.1	ns
t_{PLZ}			2.2	5.9		6.3	2.3	3.7	5.5		5.9	
t_{PZH}	OEAB	B	1.2	4.9		5.9	1.3	3	4.7		5.7	ns
t_{PZL}			1.2	4.9		5.9	1.3	3.3	4.7		5.7	
t_{PHZ}	OEAB	B	1.4	5.8		7	1.5	3.6	5.6		6.7	ns
t_{PLZ}			1.4	5.9		6.6	1.5	3.7	5.6		6.3	

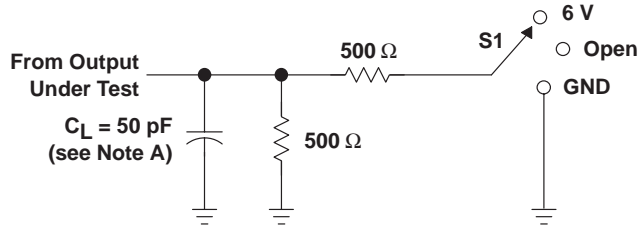
\dagger All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

\ddagger These parameters are measured with the internal output state of the storage register opposite that of the bus input.

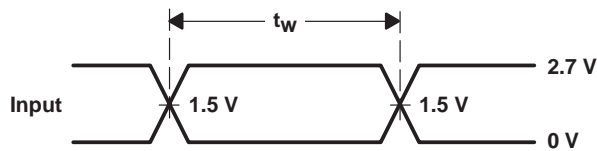
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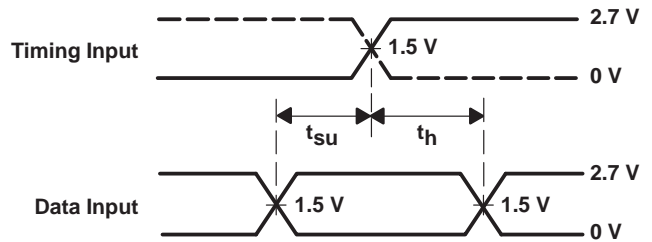
PARAMETER MEASUREMENT INFORMATION



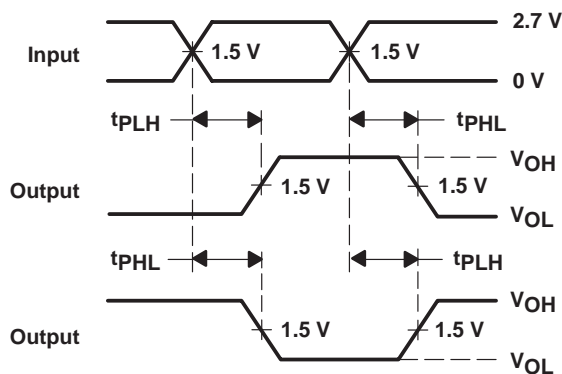
LOAD CIRCUIT



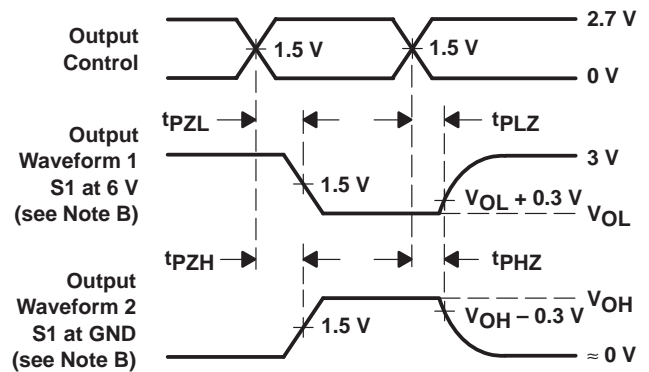
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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