- **Members of the Texas Instruments Widebus™ Family**

- **Inputs are TTL-Voltage Compatible**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**

- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

```
        54ACT16623 . . . WD PACKAGE
        75ACT16623 . . . DL PACKAGE
                 (TOP VIEW)

    1OEAB [  1      48 ] 1OEBA
      1B1 [  2      47 ] 1A1
      1B2 [  3      46 ] 1A2
      GND [  4      45 ] GND
      1B3 [  5      44 ] 1A3
      1B4 [  6      43 ] 1A4
      VCC [  7      42 ] VCC
      1B5 [  8      41 ] 1A5
      1B6 [  9      40 ] 1A6
      GND [ 10      39 ] GND
      1B7 [ 11      38 ] 1A7
      1B8 [ 12      37 ] 1A8
      2B1 [ 13      36 ] 2A1
      2B2 [ 14      35 ] 2A2
      GND [ 15      34 ] GND
      2B3 [ 16      33 ] 2A3
      2B4 [ 17      32 ] 2A4
      VCC [ 18      31 ] VCC
      2B5 [ 19      30 ] 2A5
      2B6 [ 20      29 ] 2A6
      GND [ 21      28 ] GND
      2B7 [ 22      27 ] 2A7
      2B8 [ 23      26 ] 2A8
    2OEAB [ 24      25 ] 2OEBA
```
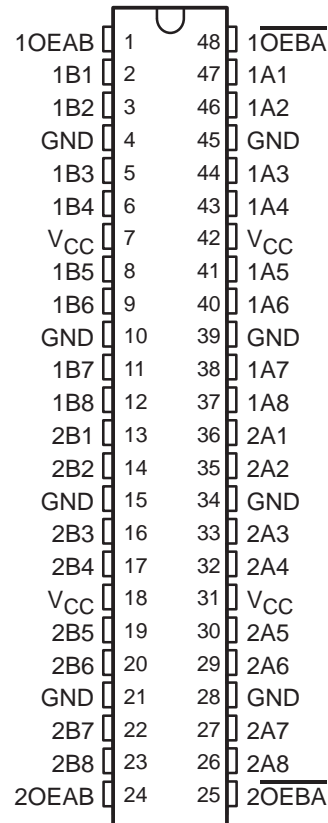
description

The 'ACT16623 are 16-bit transceivers designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the output-enable ($\overline{\text{OEBA}}$ and OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneously enabling $\overline{\text{OEBA}}$ and OEAB. Each output reinforces its input in this transceiver configuration. When both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74ACT16623 is packaged in TI's shrink small-outline package, which provides twice the functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16623 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16623 is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

logic symbol†

1$\overline{\text{OEBA}}$	48
1OEAB	1
2$\overline{\text{OEBA}}$	25
2OEAB	24

EN1
EN2
EN3
EN4

| 1A1 | 47 | | ▽ 1 | 1 | | 2 | 1B1 |
			1	2 ▽			
1A2	46					3	1B2
1A3	44					5	1B3
1A4	43					6	1B4
1A5	41					8	1B5
1A6	40					9	1B6
1A7	38					11	1B7
1A8	37					12	1B8
2A1	36		▽ 3	1		13	2B1
			1	4 ▽			
2A2	35					14	2B2
2A3	33					16	2B3
2A4	32					17	2B4
2A5	30					19	2B5
2A6	29					20	2B6
2A7	27					22	2B7
2A8	26					23	2B8
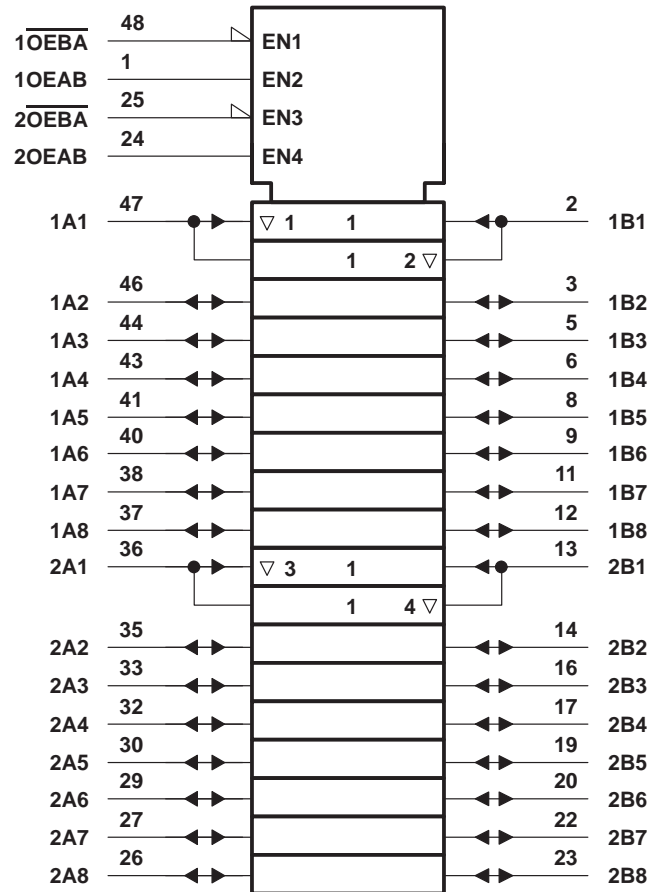
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels
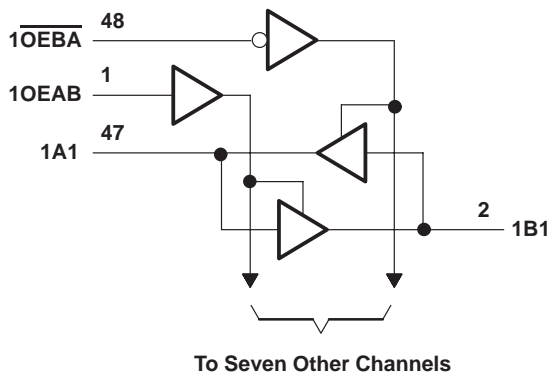
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±400 mA
Maximum power package dissipation at T_A = 55°C (in still air) (see Note 2): DL package .... 1.2 W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16623			74ACT16623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 4)	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTES: 3. Unused inputs should be connected to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
4. All V_{CC} and GND pins must be connected to the proper power supply.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT16623		74ACT16623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -24\ mA$	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		$I_{OH} = -75\ mA$†	5.5 V				3.85		3.85		
V_{OL}		$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		$I_{OL} = 24\ mA$	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		$I_{OL} = 75\ mA$†	5.5 V					1.65		1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54ACT16623		74ACT16623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4.2	7.3	9.5	4.2	10.4	4.2	10.4	ns
t_{PHL}			3.1	7.3	9.5	3.1	10.3	3.1	10.3	
t_{PZH}	$\overline{OEBA}$	A	2.7	6.8	8.8	2.7	9.5	2.7	9.5	ns
t_{PZL}			3.5	8.2	10.2	3.5	11.1	3.5	11.1	
t_{PHZ}	$\overline{OEBA}$	A	6	9.6	11.3	6	12	6	12	ns
t_{PLZ}			5.3	8.6	10.3	5.3	10.7	5.3	10.7	
t_{PZH}	OEAB	B	4.1	6.9	8.7	4.1	9.3	4.1	9.3	ns
t_{PZL}			5.1	7.9	9.7	5.1	10.6	5.1	10.6	
t_{PHZ}	OEAB	B	5.1	8.2	10.2	5.1	10.4	5.1	10.4	ns
t_{PLZ}			4.4	7.4	9.3	4.4	9.5	4.4	9.5	

operating characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\ pF$, $f = 1\ MHz$	56	pF
		Outputs disabled		11	

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PARAMETER MEASUREMENT INFORMATION
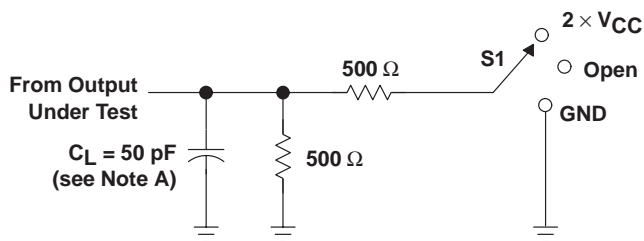
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND
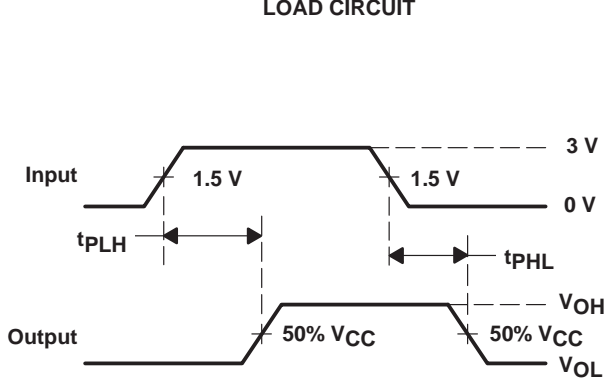
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS
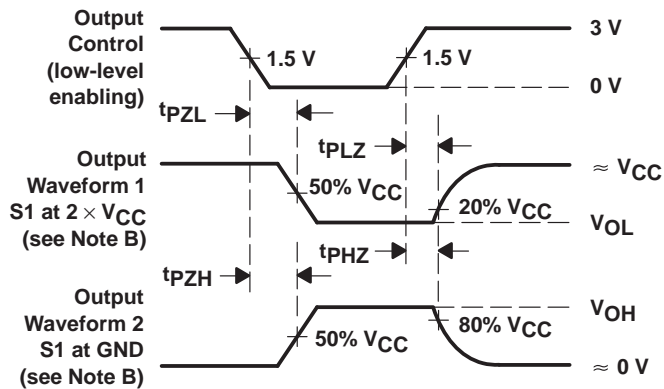
Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

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