SCLS304A - JANUARY 1996 - REVISED MAY 1997

- True Logic
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

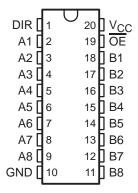
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN54HC645 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC645 is characterized for operation from –40°C to 85°C.

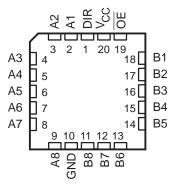
FUNCTION TABLE

INP	UTS	ODED ATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

SN54HC645...J OR W PACKAGE SN74HC645...DW OR N PACKAGE (TOP VIEW)



SN54HC645 . . . FK PACKAGE (TOP VIEW)

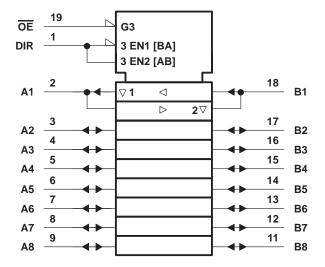




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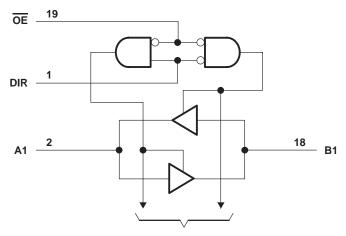


logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Transceivers

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Package thermal impedance, θ _{JA} (see Note 2): DW package	
N package	67°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SI	SN54HC645		SN74HC645			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
VIH	High-level input voltage	$V_{CC} = 4.5 \text{ V}$	3.15			3.15			V
		V _{CC} = 6 V	4.2			4.2			
	Low-level input voltage	V _{CC} = 2 V	0		0.5	0		0.5	
VIL		V _{CC} = 4.5 V	0		1.35	0		1.35	V
		VCC = 6 V	0		1.8	0		1.8	
VI	Input voltage		0		VCC	0		VCC	V
Vo	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V	0		1000	0		1000	
t _t	Input transition (rise and fall) time	V _{CC} = 4.5 V	0		500	0		500	ns
		VCC = 6 V	0		400	0		400	
TA	Operating free-air temperature		-55		125	-40		85	°C



SN54HC645, SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD	AMETED	TEST CONDITIONS		Vaa	T	A = 25°C	;	SN54H	C645	SN74HC645		UNIT
PARAMETER		1231 CONDITIONS		vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
				2 V	1.9	1.998		1.9		1.9		
			$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		4.4		
Vон		VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
			$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
			$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
		VI = VIH or VIL	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	
				4.5 V		0.001	0.1		0.1		0.1	
VOL				6 V		0.001	0.1		0.1		0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
			$I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
Ц	DIR or OE	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
loz	A or B	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	μΑ
Icc		$V_I = V_{CC}$ or 0,	I _O = 0	6 V			8		160		80	μΑ
Ci	DIR or OE			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Vaa	T,	ղ = 25°C	;	SN54HC645		SN74HC645		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			2 V		40	105		160		130		
^t pd	A or B	B or A	4.5 V		15	21		32		26	ns	
			6 V		12	18		27		22		
	ŌĒ	A or B	2 V		125	230		340		290	ns	
^t en			4.5 V		23	46		68		58		
				6 V		20	39		58		49	
	ŌĒ		2 V		74	200		300		250		
^t dis		ŌĒ	A or B	4.5 V		25	40		60		50	ns
			6 V		21	34		51		43		
		A or B	2 V		20	60		90		75		
t _t			A or B	4.5 V		8	12		18		15	ns
			6 V		6	10		15		13		



SN54HC645, SN74HC645 **OCTAL BUS TRÂNSCEIVERS** WITH 3-STATE OUTPUTS SCLS304A - JANUARY 1996 - REVISED MAY 1997

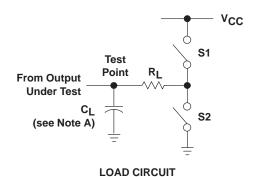
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	Vaa	T,	Վ = 25 °C	;	SN54H	IC645	SN74H	C645	UNIT								
TAKAWILTEK	(INPUT)		(OUTPUT)	(OUTPUT)	(OUTPUT)	(OUTPUT)	(OUTPUT)	(OUTPUT)	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT		
			2 V		54	135		200		170									
t _{pd}	A or B	B or A	4.5 V		18	27		40		34	ns								
				ľ		ľ				Ī	Ī	6 V		15	23		34		29
	ŌĒ	OE A or B	2 V		150	270		405		335									
t _{en}			4.5 V		31	54		81		67	ns								
					6 V		25	46		69		56							
				2 V		45	210		315		265								
t _t		A or B	4.5 V		17	42		63		53	ns								
			6 V		13	36		53		45									

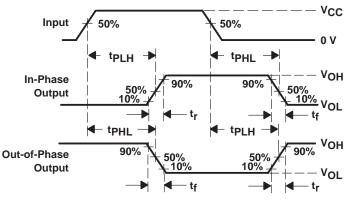
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance per transceiver	No load	40	pF

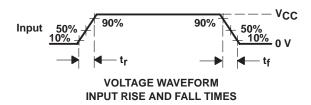
PARAMETER MEASUREMENT INFORMATION

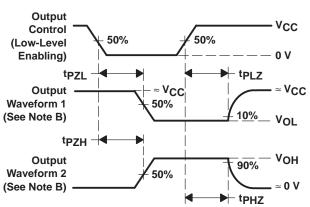


PARAI	METER	RL	CL	S1	S2	
	tPZH 1 kΩ		50 pF or	Open	Closed	
ten	tPZL	1 K22	150 pF	Closed	Open	
t	tPHZ	1 kΩ	50 pF	Open	Closed	
tdis	tPLZ	1 K22	30 pi	Closed	Open	
t _{pd} or t _t		_	50 pF or 150 pF	Open	Open	



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 6 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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