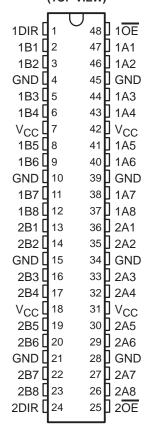- Members of the Texas Instruments *Widebus*™ Family

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process

- Inputs Are TTL-Voltage Compatible

- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise

- Flow-Through Architecture Optimizes PCB Layout

- Latch-Up Performance Exceeds 250 mA Per JESD 17

- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54AHCT16245 . . . WD PACKAGE
SN74AHCT16245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	$1\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	$2\overline{OE}$

description

The 'AHCT16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHCT16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit transceiver)

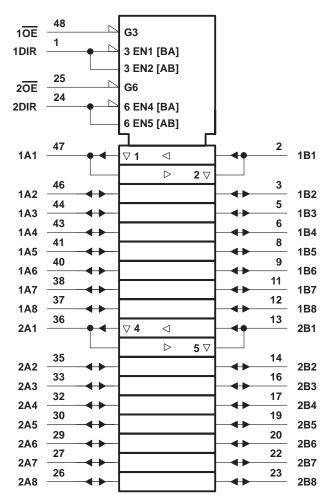| INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

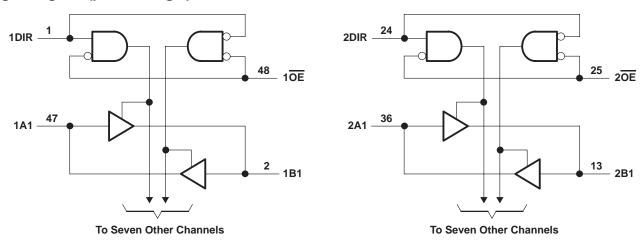EPIC and Widebus are trademarks of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

logic symbol†

1OE	48 → G3
1DIR	1 → 3 EN1 [BA]
	3 EN2 [AB]
2OE	25 → G6
2DIR	24 → 6 EN4 [BA]
	6 EN5 [AB]

1A1	47	▽ 1 ◁	2	1B1
		▷ 2 ▽		
1A2	46		3	1B2
1A3	44		5	1B3
1A4	43		6	1B4
1A5	41		8	1B5
1A6	40		9	1B6
1A7	38		11	1B7
1A8	37		12	1B8
2A1	36	▽ 4 ◁	13	2B1
		▷ 5 ▽		
2A2	35		14	2B2
2A3	33		16	2B3
2A4	32		17	2B4
2A5	30		19	2B5
2A6	29		20	2B6
2A7	27		22	2B7
2A8	26		23	2B8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

1DIR 1

48 1OE

1A1 47

2 1B1

To Seven Other Channels

2DIR 24

25 2OE

2A1 36

13 2B1

To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through each V_{CC} or GND .... ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 70°C/W
                                                      DGV package .... 58°C/W
                                                      DL package .... 63°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
             2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54AHCT16245		SN74AHCT16245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IO}	Input/output voltage, A or B pins	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	SN54AHCT16245 MIN	MAX	SN74AHCT16245 MIN	MAX	UNIT
V_{OH}		$I_{OH} = -50 \ \mu A$	4.5 V	4.4	4.5		4.4		4.4		V
		$I_{OH} = -8 \ mA$		3.94			3.8		3.8		
V_{OL}		$I_{OL} = 50 \ \mu A$	4.5 V			0.1		0.1		0.1	V
		$I_{OL} = 8 \ mA$				0.36		0.44		0.44	
I_I	$\overline{OE}$ or DIR	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I_{OZ}†	A or B inputs	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	$\overline{OE}$ or DIR	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_{io}	A or B inputs	$V_I = V_{CC}$ or GND	5 V		4						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
† For I/O ports, the parameter I_{OZ} includes the input leakage current.
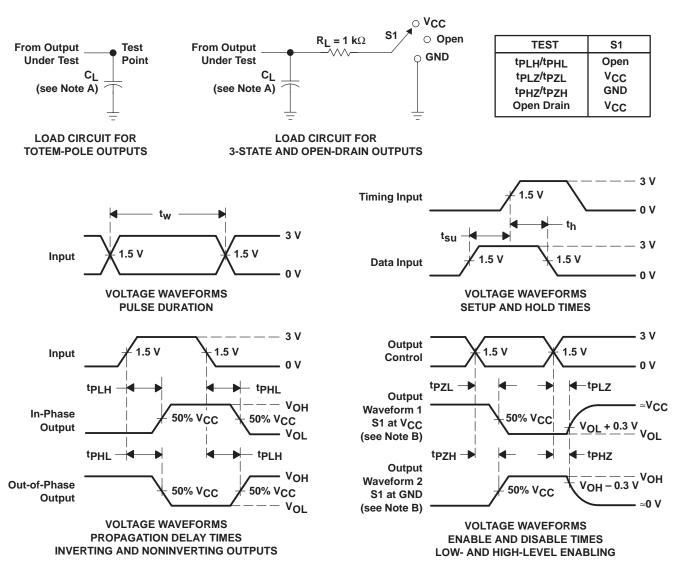‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$ MIN	TYP	MAX	SN54AHCT16245 MIN	MAX	SN74AHCT16245 MIN	MAX	UNIT
t_{PLH}	A or B	B or A	C_L = 15 pF		4.5**	8.5**	1**	10**	1	9.5	ns
t_{PHL}					4.5**	8.5**	1**	10**	1	9.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF		8.9**	13**	1**	14**	1	14	ns
t_{PZL}					8.9**	13**	1**	14**	1	14	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF		9.2**	14**	1**	15**	1	15	ns
t_{PLZ}					9.2**	14**	1**	15**	1	15	
t_{PLH}	A or B	B or A	C_L = 50 pF		7	9.5	1	11	1	10.5	ns
t_{PHL}					5.3	9.5	1	11	1	10.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		8.3	14	1	15	1	15	ns
t_{PZL}					8.3	14	1	15	1	15	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		8	14	1	15	1	15	ns
t_{PLZ}					8	14	1	15	1	15	
$t_{sk(o)}$			C_L = 50 pF		1***					1	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.
*** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, $T_A = 25°C$ (see Note 4)

PARAMETER		SN74AHCT16245 MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

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operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	17	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
        Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
     D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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