- **Members of the Texas Instruments *Widebus*™ Family**
- **D-Type Flip-Flops With Qualified Storage Enable**
- **Translate Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltages With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down-Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND-Pin Configuration Minimizes High-Speed Switching Noise**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Ceramic Quad Flat (HV) Packages**

description

The ’GTL16923 devices are 18-bit registered bus transceivers that provide LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. They are partitioned as two 9-bit transceivers with individual output-enable controls and contain D-type flip-flops for temporary storage of data flowing in either direction. The devices provide an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and output edge control (OEC™).

The user has the flexibility of using these devices at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels. All inputs can be driven from either 3.3-V or 5-V devices which allows use in a mixed 3.3-V/5-V system environment. V_{REF} is the reference input voltage for the B port.

Data flow in each direction is controlled by the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock (CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs are used to enable or disable the clock for all 18 bits at a time. However, $\overline{OEAB}$ and $\overline{OEBA}$ are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

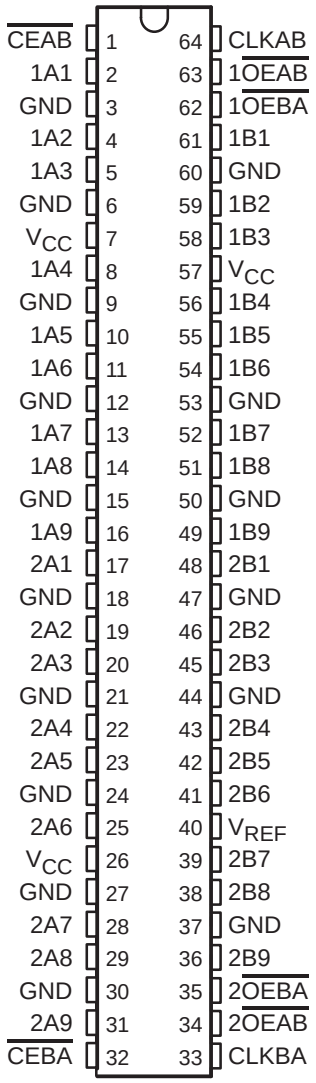
These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

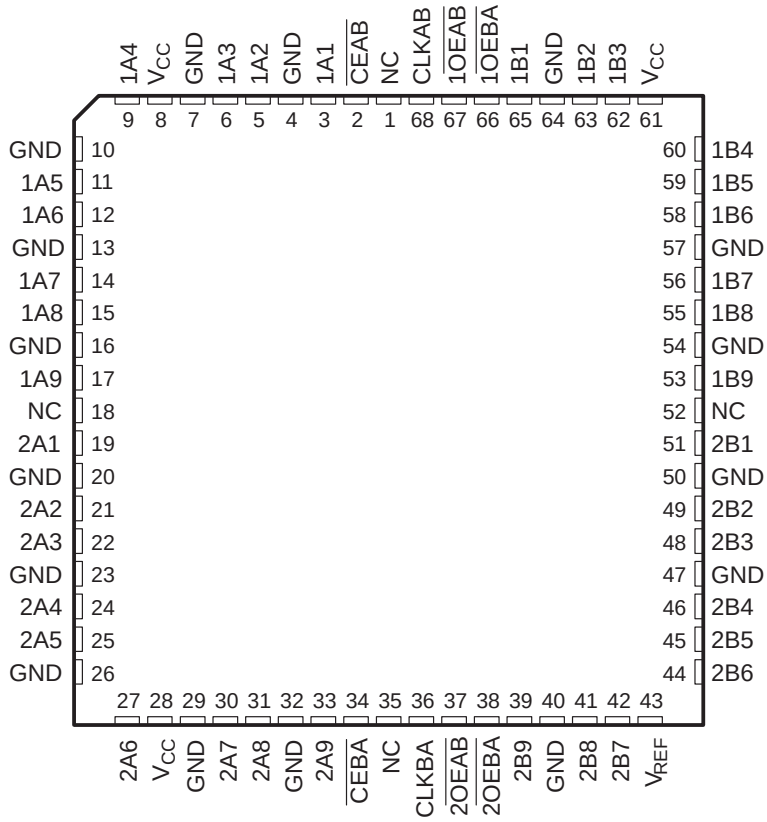
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16923 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74GTL16923 is characterized for operation from –40°C to 85°C.

SN74GTL16923 . . . DGG PACKAGE
(TOP VIEW)



SN54GTL16923 . . . HV PACKAGE
(TOP VIEW)



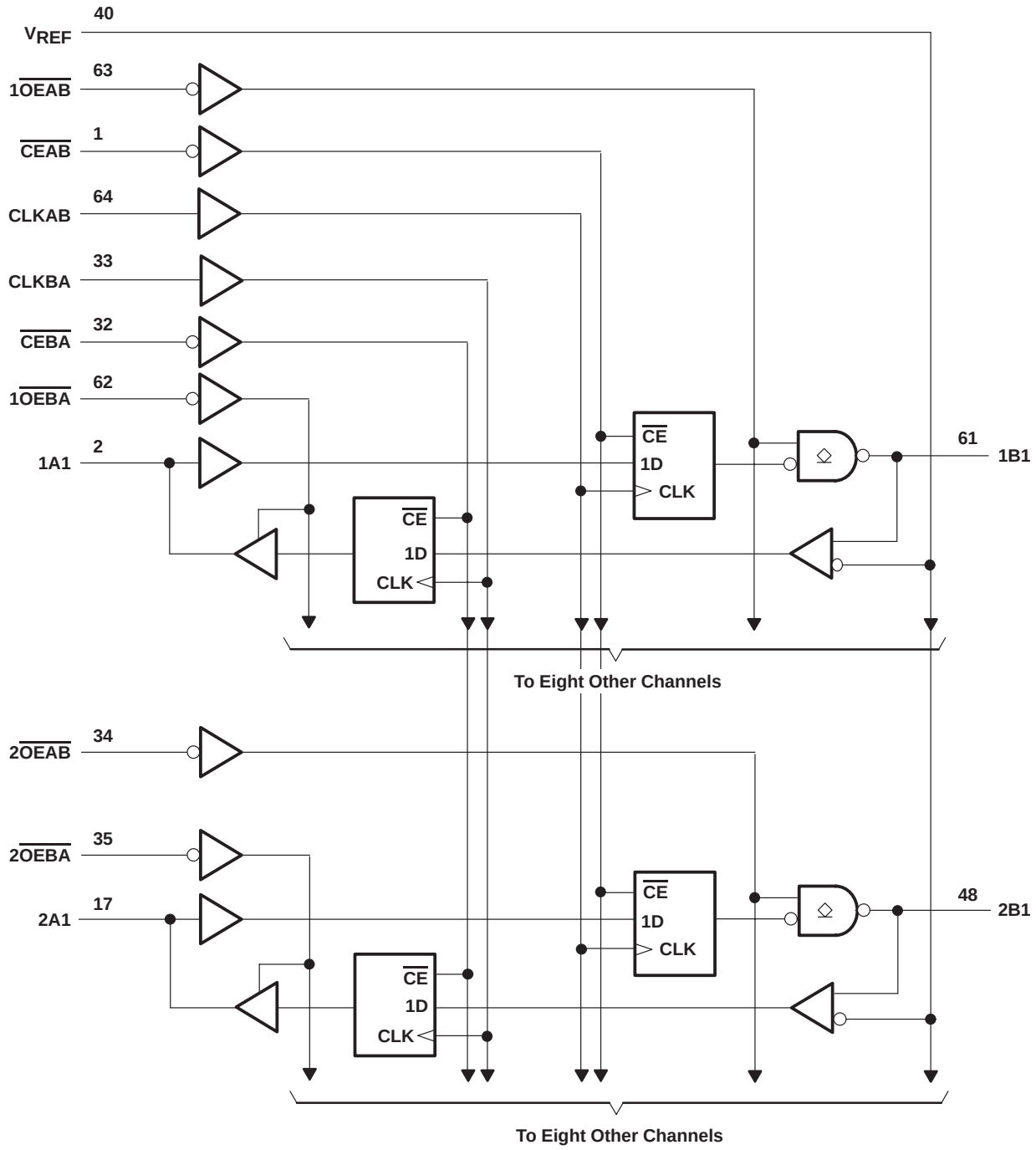
NC – No internal connection

FUNCTION TABLE†

INPUTS				OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A		
X	H	X	X	Z	Isolation
H	L	X	X	B_0‡	Latched storage of A data
X	L	H or L	X	B_0‡	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

† A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



Pin numbers shown are for the DGG package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1) . . . . . –0.5 V to 7 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 100 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 55°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Notes 4 through 6)

			SN54GTL16923			SN74GTL16923			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3.15	3.3	3.45	3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	
V_I	Input voltage	B port	0		V_{TT}	0		V_{TT}	V
		Except B port	0		5.5	0		5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V_{REF}+50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV			V_{REF}–50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–24			–24	mA
I_{OL}	Low-level output current	A port			24			24	mA
		B port			50			50	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTES: 4. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is 2/3 V_{TT}.

electrical characteristics over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16923			SN74GTL16923			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 μA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			2.4			
			I_{OH} = –24 mA	2			2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 μA			0.2			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4			0.4	
			I_{OL} = 24 mA			0.5			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 μA			0.2			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2			0.2	
			I_{OL} = 40 mA			0.4			0.4	
			I_{OL} = 50 mA			0.55			0.55	
I_I	B port	V_{CC} = 3.45 V	V_I = 5.5 V or GND			±5			±5	μA
	A-port and control inputs	V_{CC} = 3.45 V	V_I = V_{CC} or GND			±5			±5	
			V_I = 5.5 V or GND			±20			±20	
I_{off}		V_{CC} = 0, V_I or V_O = 0 to 5.5 V							±100	μA
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	–75			–75			
		V_{CC} = 3.45 V‡,	V_I = 0.8 V to 2 V			±500			±500	
I_{OZ}§	A port	V_{CC} = 3.45 V,	V_O = V_{CC} or GND			±10			±10	μA
I_{OZH}	B port	V_{CC} = 3.45 V,	V_O = 1.5 V			10			10	μA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			60			60	mA
			Outputs low			60			60	
			Outputs disabled			60			60	
ΔI_{CC}¶		V_{CC} = 3.45 V, A-port or control inputs at V_{CC} or GND, One input at V_{CC} – 0.6 V				500			500	μA
C_i	Control inputs	V_I = 3.15 V or 0			2.5	3		2.5	3	pF
C_{io}	A port	V_O = 3.15 V or 0			6	8.5		6	8.5	pF
	B port	V_O = 3.15 V or 0			7	9.5		7	9.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)

			SN54GTL16923		SN74GTL16923		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			200		200	MHz
t_w	Pulse duration, CLK high or low		2.5		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.7		2.6		ns
		$\overline{CE}$ before CLK↑	3.5		3.3		
t_h	Hold time	Data after CLK↑	0.2		0.1		ns
		$\overline{CE}$ after CLK↑	0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16923			SN74GTL16923			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			200			200			MHz
t_{PLH}	CLKAB	B	2.1		6	2.2		5.8	ns
t_{PHL}			2		6.5	2.1		6.3	
t_{dis}	$\overline{OEAB}$	B	1.6		5.6	1.7		5.3	ns
t_{en}			1.9		5.2	2		5	
Slew rate	Both transitions			0.5			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1 V)		0.2		3	0.3		2.9	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0		4.3	0.1		3.9	ns
t_{PLH}	CLKBA	A	1.7		5.3	1.8		5	ns
t_{PHL}			1.6		5.1	1.7		4.8	
t_{en}	$\overline{OEBA}$	A	1.2		5.1	1.3		4.8	ns
t_{dis}			1.9		5.1	2		4.8	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

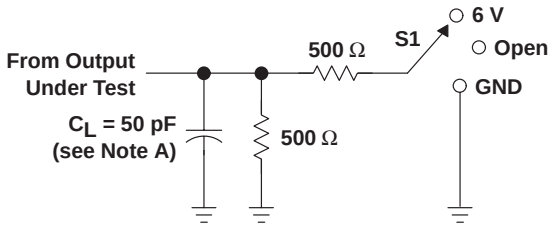
			SN54GTL16923		SN74GTL16923		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			200		200	MHz
t_w	Pulse duration, CLK high or low		2.5		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.4		2.3		ns
		$\overline{CE}$ before CLK↑	3.5		3.3		
t_h	Hold time	Data after CLK↑	0.2		0.1		ns
		$\overline{CE}$ after CLK↑	0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16923			SN74GTL16923			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			200			200			MHz
t_{PLH}	CLKAB	B	2.1		6.1	2.2	4	5.9	ns
t_{PHL}			2		6.3	2.1	4	6.1	
t_{PLH}	$\overline{OEAB}$	B	1.8		5.4	1.9	3.4	5.2	ns
t_{PHL}			1.6		5.4	1.7	3.1	5.1	
Slew rate	Both transitions			0.5			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1.3 V)		0.5		2.7	0.6	1.3	2.6	ns
t_f	Transition time, B outputs (1.3 V to 0.6 V)		0.3		3.4	0.4	1.3	3	ns
t_{PLH}	CLKBA	A	1.7		5.4	1.8	3.5	5.1	ns
t_{PHL}			1.6		5.2	1.7	3.3	4.9	
t_{en}	$\overline{OEBA}$	A	1.2		5.1	1.3	2.9	4.8	ns
t_{dis}			1.9		5.3	2	3.2	5	

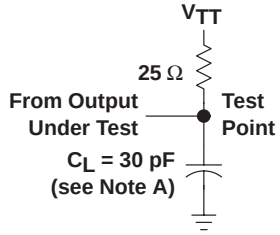
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.5 V, V_{REF} = 1 V

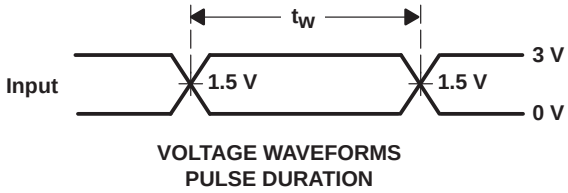


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

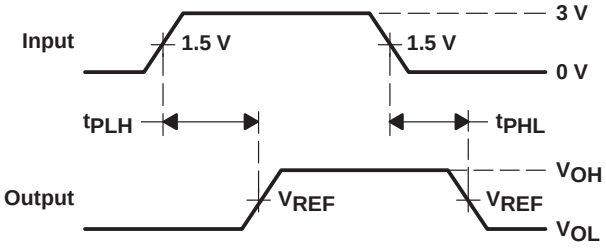
LOAD CIRCUIT FOR A OUTPUTS



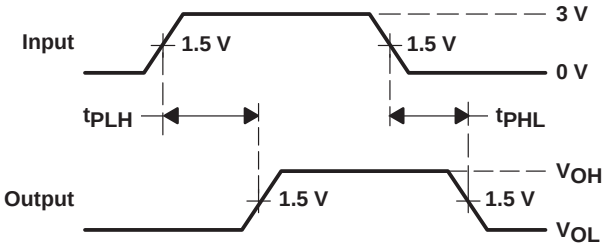
LOAD CIRCUIT FOR B OUTPUTS



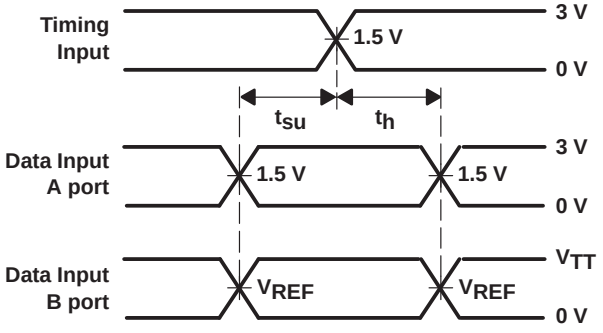
VOLTAGE WAVEFORMS
PULSE DURATION



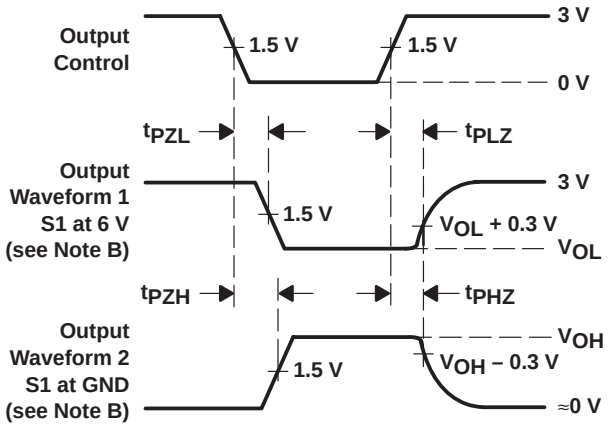
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKAB to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKBA to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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