



SCCS066 - June 1997 - Revised March 2000

# CY74FCT163500

## 18-Bit Registered Transceiver

### Features

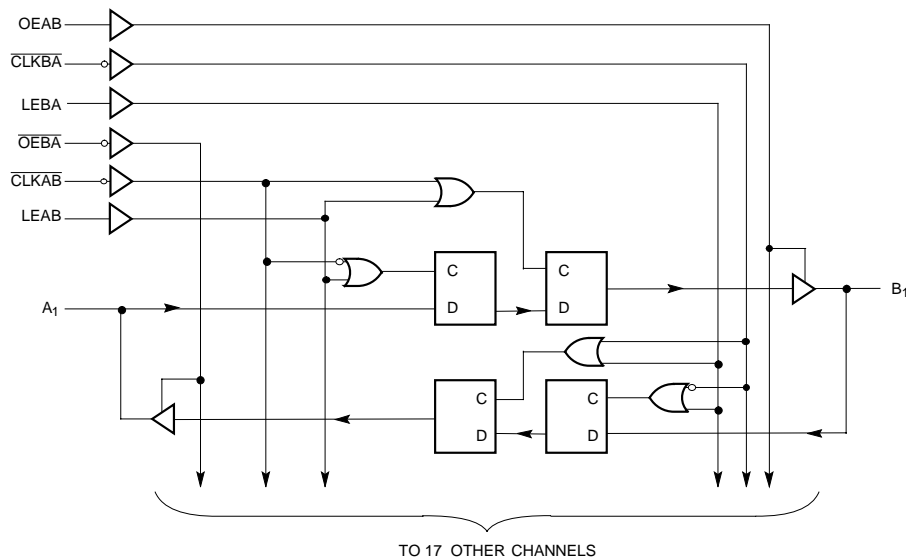
- Low power, pin-compatible replacement for LCX and LPT families
- 5V tolerant inputs and outputs
- 24 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 4.6 ns
- Latch-up performance exceeds JEDEC standard no. 17
- ESD > 2000V per MIL-STD-883D, Method 3015
- Typical output skew < 250ps
- Industrial temperature range of -40°C to +85°C
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical  $V_{olp}$  (ground bounce) performance exceeds Mil Std 883D
- $V_{CC} = 2.7V$  to 3.6V

### Functional Description

The CY74FCT163500 is an 18-bit universal bus transceiver that can be operated in transparent, latched, or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch enable ( $\overline{LEAB}$  and  $\overline{LEBA}$ ), and clock inputs ( $\overline{CLKAB}$  and  $\overline{CLKBA}$ ) inputs. For A-to-B data flow, the device operates in transparent mode when  $\overline{LEAB}$  is HIGH. When  $\overline{LEAB}$  is LOW, the A data is latched if  $\overline{CLKAB}$  is held at a HIGH or LOW logic level. If  $\overline{LEAB}$  is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of  $\overline{CLKAB}$ .  $\overline{OEAB}$  performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by  $\overline{OEBA}$ ,  $\overline{LEBA}$ , and  $\overline{CLKBA}$ .

The CY74FCT163500 has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The inputs and outputs are capable of being driven by 5.0V busses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power off disable feature enabling them to be used in applications requiring live insertion.

### Logic Block Diagram



### Pin Configuration

SSOP/TSSOP  
Top View

$\overline{OEAB}$	1	56	GND
$\overline{LEAB}$	2	55	$\overline{CLKAB}$
A <sub>1</sub>	3	54	B <sub>1</sub>
GND	4	53	GND
A <sub>2</sub>	5	52	B <sub>2</sub>
A <sub>3</sub>	6	51	B <sub>3</sub>
V <sub>CC</sub>	7	50	V <sub>CC</sub>
A <sub>4</sub>	8	49	B <sub>4</sub>
A <sub>5</sub>	9	48	B <sub>5</sub>
A <sub>6</sub>	10	47	B <sub>6</sub>
GND	11	46	GND
A <sub>7</sub>	12	45	B <sub>7</sub>
A <sub>8</sub>	13	44	B <sub>8</sub>
A <sub>9</sub>	14	43	B <sub>9</sub>
A <sub>10</sub>	15	42	B <sub>10</sub>
A <sub>11</sub>	16	41	B <sub>11</sub>
A <sub>12</sub>	17	40	B <sub>12</sub>
GND	18	39	GND
A <sub>13</sub>	19	38	B <sub>13</sub>
A <sub>14</sub>	20	37	B <sub>14</sub>
A <sub>15</sub>	21	36	B <sub>15</sub>
V <sub>CC</sub>	22	35	V <sub>CC</sub>
A <sub>16</sub>	23	34	B <sub>16</sub>
A <sub>17</sub>	24	33	B <sub>17</sub>
GND	25	32	GND
A <sub>18</sub>	26	31	B <sub>18</sub>
$\overline{OEBA}$	27	30	$\overline{CLKBA}$
$\overline{LEBA}$	28	29	GND

**Pin Summary**

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{CLKAB}$	A-to-B Clock Input (Active LOW)
$\overline{CLKBA}$	B-to-A Clock Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

**Function Table<sup>[1, 2]</sup>**

Inputs				Outputs
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	$\downarrow$	L	L
H	L	$\downarrow$	H	H
H	L	H	X	B <sup>[3]</sup>
H	L	L	X	B <sup>[4]</sup>

**Notes:**

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance.  $\downarrow$  = HIGH-to-LOW Transition.
2. A-to-B data flow is shown, B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that  $\overline{CLKAB}$  was LOW before LEAB went LOW.
5. Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range.
6. Unused inputs must always be connected to an appropriate logic voltage level, preferably either  $V_{CC}$  or ground.

**Maximum Ratings<sup>[5, 6]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-55°C to +125°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage Range .....	0.5V to +4.6V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Voltage .....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin) .....	-60 to +120 mA
Power Dissipation .....	1.0W
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Industrial	-40°C to +85°C	2.7V to 3.6V

**Electrical Characteristics** Over the Operating Range  $V_{CC}=2.7V$  to  $3.6V$ 

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage	All Inputs	2.0		5.5	V
$V_{IL}$	Input LOW Voltage				0.8	V
$V_H$	Input Hysteresis <sup>[8]</sup>			100		mV
$V_{IK}$	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}$ , $I_{IN}=-18\text{ mA}$		-0.7	-1.2	V
$I_{IH}$	Input HIGH Current	$V_{CC}=\text{Max.}$ , $V_I=5.5V$			$\pm 1$	$\mu A$
$I_{IL}$	Input LOW Current	$V_{CC}=\text{Max.}$ , $V_I=\text{GND.}$			$\pm 1$	$\mu A$
$I_{OZH}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}$ , $V_{OUT}=5.5V$			$\pm 1$	$\mu A$
$I_{OZL}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}$ , $V_{OUT}=\text{GND}$			$\pm 1$	$\mu A$
$I_{ODL}$	Output LOW Current <sup>[9]</sup>	$V_{CC}=3.3V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	45		180	mA
$I_{ODH}$	Output HIGH Current <sup>[9]</sup>	$V_{CC}=3.3V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	-45		-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC}=\text{Min.}$ , $I_{OH}= -0.1\text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=3.0V$ , $I_{OH}= -8\text{ mA}$	2.4	3.0		V
		$V_{CC}=3.0V$ , $I_{OH}= -24\text{ mA}$	2.0	3.0		V
$V_{OL}$	Output LOW Voltage	$V_{CC}=\text{Min.}$ , $I_{OL}= 0.1\text{ mA}$			0.2	V
		$V_{CC}=\text{Min.}$ , $I_{OL}= 24\text{ mA}$		0.3	0.5	
$I_{OS}$	Short Circuit Current <sup>[9]</sup>	$V_{CC}=\text{Max.}$ , $V_{OUT}=\text{GND}$	-60	-135	-240	mA
$I_{OFF}$	Power-Off Disable	$V_{CC}=0V$ , $V_{OUT}\leq 4.5V$			$\pm 100$	$\mu A$

**Capacitance<sup>[8]</sup>** ( $T_A = +25^\circ C$ ,  $f = 1.0\text{ MHz}$ )

Parameter	Description	Test Conditions	Typ. <sup>[7]</sup>	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

**Notes:**

7. Typical values are at  $V_{CC}=3.3V$ ,  $T_A = +25^\circ C$  ambient.
8. This parameter is specified but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

**Power Supply Characteristics**

Parameter	Description	Test Conditions		Typ. <sup>[7]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}$	$V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC}-0.2V$	0.1	10	$\mu A$
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}$	$V_{IN}=V_{CC}-0.6V^{[10]}$	2.0	30	$\mu A$
$I_{CCD}$	Dynamic Power Supply Current <sup>[11]</sup>	$V_{CC}=\text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, OEAB=OEBA= $V_{CC}$ or GND	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	50	75	$\mu A/\text{MHz}$
$I_C$	Total Power Supply Current <sup>[12]</sup>	$V_{CC}=\text{Max.}$ , $f_0=10$ MHz (CLKAB), $f_1=5$ MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OEAB=OEBA= $V_{CC}$ LEAB=GND	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	0.5	0.8	mA
			$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=\text{GND}$	0.5	0.8	mA
		$V_{CC}=\text{Max.}$ , $f_0=10$ MHz, $f_1=2.5$ MHz, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, OEAB=OEBA= $V_{CC}$ LEAB=GND	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	2.5	3.8 <sup>[13]</sup>	mA
			$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=\text{GND}$	2.6	4.1 <sup>[13]</sup>	mA

**Notes:**

10. Per TTL driven input; all other inputs at  $V_{CC}$  or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0 N_C / 2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $N_C$  = Number of clock inputs changing at  $f_1$   
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range  $V_{CC} = 3.0V$  to  $3.6V$ <sup>[14, 15]</sup>

Parameter	Description	CY74FCT163500A		CY74FCT163500C		Unit	Fig. No. <sup>[16]</sup>
		Min.	Max.	Min.	Max.		
$f_{MAX}$	$\overline{CLKAB}$ or $\overline{CLKBA}$ frequency		150		150	MHz	
$t_{PLH}$ $t_{PHL}$	Propagation Delay A to B or B to A	1.5	5.1	1.5	4.6	ns	1, 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay LEBA to A, LEAB to B	1.5	5.6	1.5	5.3	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CLKBA}$ to A, $\overline{CLKAB}$ to B	1.5	5.6	1.5	5.3	ns	1, 5
$t_{PZH}$ $t_{PZL}$	Output Enable Time OEBA to A, OEAB to B	1.5	6.0	1.5	5.4	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time OEBA to A, OEAB to B	1.5	5.6	1.5	5.2	ns	1, 7, 8
$t_{SU}$	Set-Up Time, HIGH or LOW A to $\overline{CLKAB}$ , B to $\overline{CLKBA}$	3.0		3.0		ns	9
$t_H$	Hold Time, HIGH or LOW A to $\overline{CLKAB}$ , B to $\overline{CLKBA}$	0		0		ns	9
$t_{SU}$	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock HIGH	3.0		3.0	ns	4
		Clock LOW	1.5		1.5	ns	4
$t_H$	Hold Time, HIGH or LOW A to LEAB, B to LEBA	1.5		1.5		ns	4
$t_W$	LEAB or LEBA Pulse Width HIGH	3.0		2.5		ns	5
$t_W$	$\overline{CLKAB}$ or $\overline{CLKBA}$ Pulse Width HIGH or LOW	3.0		3.0		ns	5
$t_{SK(O)}$	Output Skew <sup>[17]</sup>		0.5		0.5	ns	

**Ordering Information CY74FCT163500**

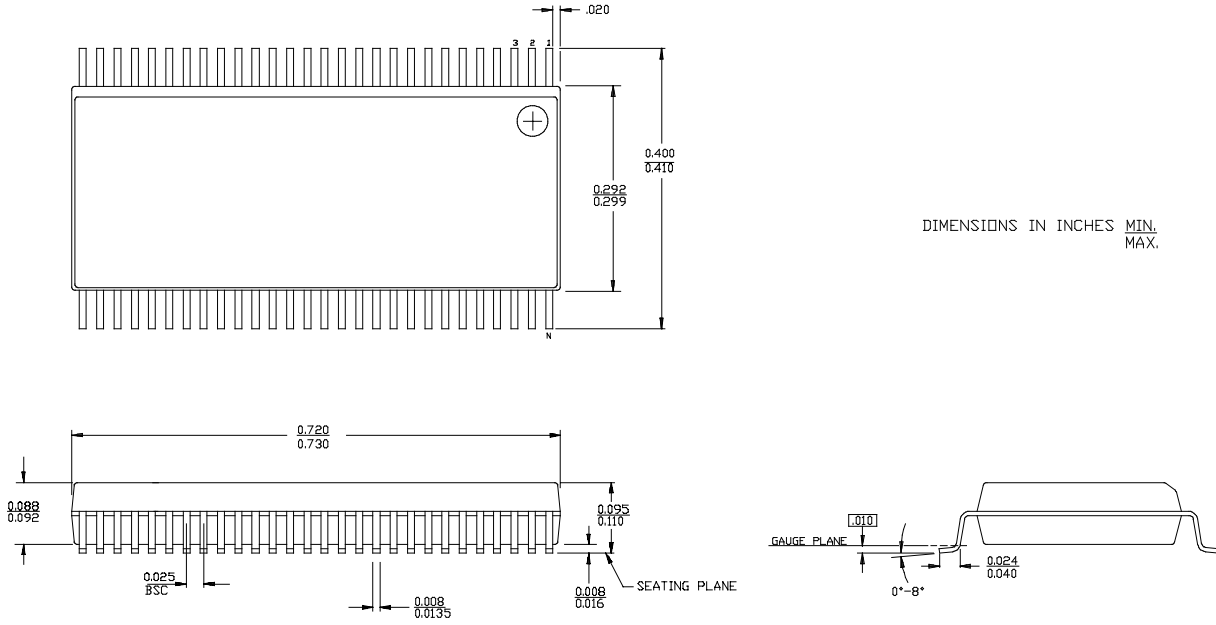
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT163500CPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163500CPVC/PVCT	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT163500APVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

**Notes:**

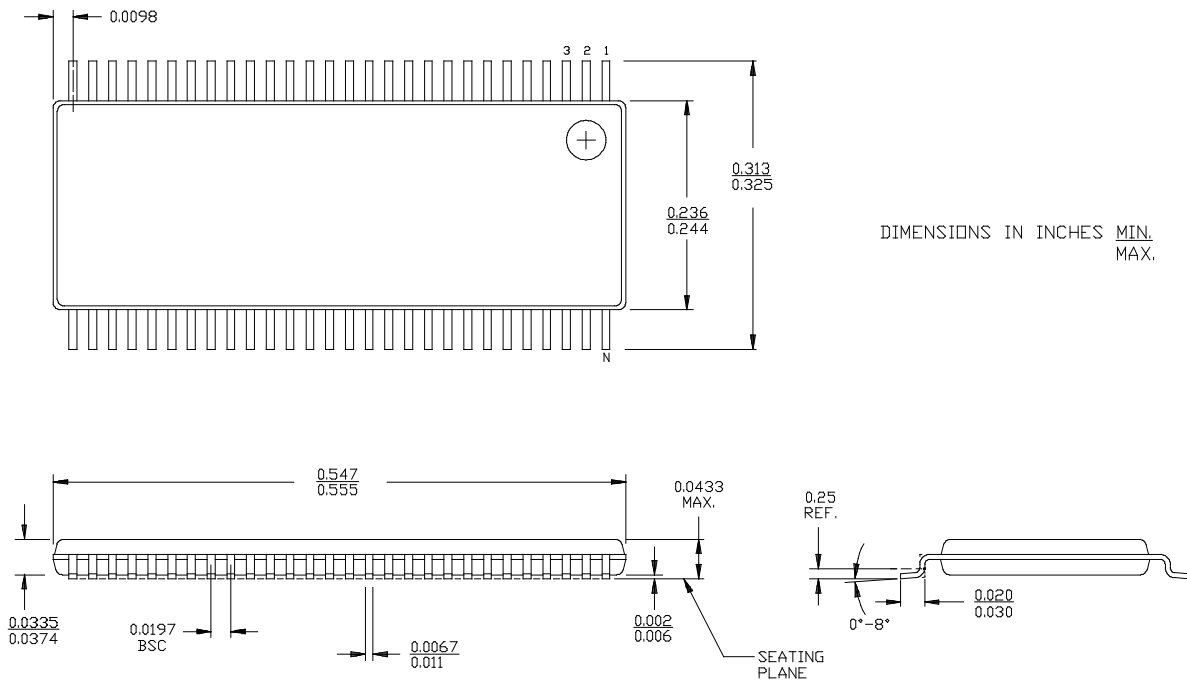
14. Minimum limits are specified but not tested on Propagation Delays.
15. For  $V_{CC} = 2.7$ , propagation delay, output enable and output disable times should be degraded by 20%.
16. See "Parameter Measurement Information" in the General Information section.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Package Diagrams**

**56-Lead Shrunk Small Outline Package O56**



**56-Lead Thin Shrunk Small Outline Package Z56**



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