Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

TEXAS INSTRUMENTS

CY74FCT163501
CY74FCT163H501

SCCS047 - January 1998 - Revised March 2000

18-Bit Registered Transceivers

Features

- **Low power, pin-compatible replacement for LCX and LPT families**
- **5V tolerant inputs and outputs**
- **24 mA balanced drive outputs**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for reduced noise**
- **FCT-C speed at 4.6 ns**
- **Latch-up performance exceeds JEDEC standard no. 17**
- **ESD > 2000V per MIL-STD-883D, Method 3015**
- **Typical output skew < 250ps**
- **Industrial temperature range of –40˚C to +85˚C**
- **TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)**
- **Typical V_{olp} (ground bounce) performance exceeds Mil Std 883D**
- **V_{CC} = 2.7V to 3.6V**

CY74FCT163501 Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 3.3V, T_A= 25˚C**

CY74FCT163H501 Features:

- **Bus hold retains the last active state**
- **Devices with bus hold are not recommended for translating rail-to-rail CMOS signals to 3.3V logic levels**
- **Eliminates the need for external pull-up or pull-down resistors**

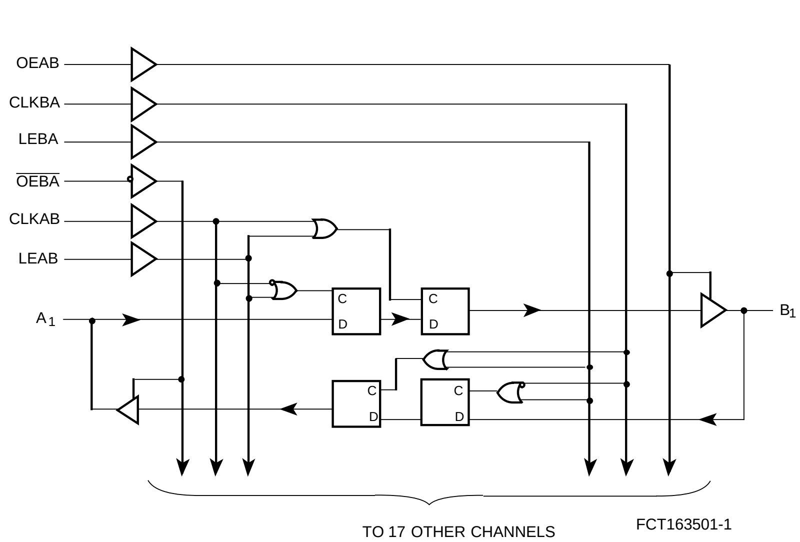
Functional Description

These 18-bit universal bus transceivers can be operated in transparent, latched or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock inputs (CLKAB and CLKBA). For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

THE CY74FCT163501 has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors, as well as provides for minimal undershoot and reduced ground bounce. The CY74FCT163501 is ideal for driving transmission lines.

The CY74FCT163H501 is a 24-mA balanced output part, that has “bus hold” on the data inputs. The device retains the input’s last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Functional Block Diagram; CY74FCT163501, CY74FCT163H501



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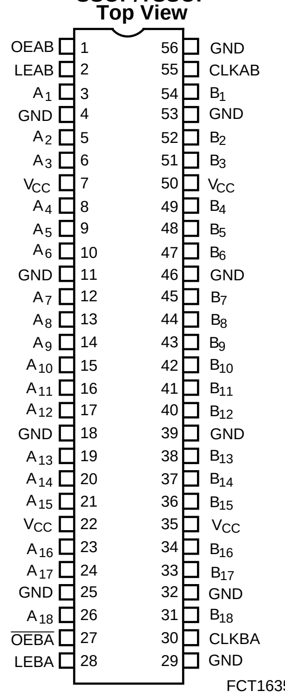
Pin Configuration

SSOP/TSSOP
Top View



FCT163501-2

Pin Description

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[1]

Function Table[2, 3]

Inputs				Outputs
OEAB	**LEAB**	**CLKAB**	**A**	**B**
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B[4]
H	L	H	X	B[5]

Maximum Ratings[6, 7]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–55°C to +125°C

Ambient Temperature with
Power Applied ....–55°C to +125°C

DC Input Voltage ....–0.5V to +7.0V

DC Output Voltage ....–0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) ....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage...>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V

1. On the 74FCT163H501 these pins have bus hold.
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ↑ = LOW-to-HIGH Transition
4. Output level before the indicated steady-state input conditions were established.
5. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
6. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
7. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics for Non Bus Hold Devices Over the Operating Range V_{CC} = 2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{IH}	Input HIGH Voltage	All Inputs	2.0		5.5	V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[9]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=5.5			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=5.5V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=GND			±1	µA
I_{OS}	Short Circuit Current[10]	V_{CC}=Max., V_{OUT}=GND	–60	–135	–240	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±100	µA
I_{CC}	Quiescent Power Supply Current	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V; V_{CC}=Max.		0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{IN}=V_{CC}–0.6V[11]; V_{CC}=Max.		2.0	30	µA

Notes:

8. Typical values are at V_{CC}=3.3V, T_A = +25˚C ambient.
9. This parameter is specified but not tested.
10. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
11. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

Electrical Characteristics For Bus Hold Devices Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions		Min.	Typ.[8]	Max.	Unit
V_{IH}	Input HIGH Voltage	All Inputs		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Input Hysteresis[9]				100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}				±100	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND				±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[12]	V_{CC}=Min.	V_I=2.0V	–50			µA
			V_I=0.8V	+50			µA
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[12]	V_{CC}=Max., V_I=1.5V				±500	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=V_{CC}				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=GND				±1	µA
I_{OS}	Short Circuit Current[10]	V_{CC}=Max., V_{OUT}=GND		–60	–135	–240	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V				±100	µA
I_{CC}	Quiescent Power Supply Current	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V	V_{CC}=Max.			+40	µA
ΔI_{CC}	Quiescent Power supply Current (TTL inputs HIGH)	V_{IN}=V_{CC}–0.6V[11]	V_{CC}=Max.			+350	µA

Electrical Characteristics For Balanced Drive Devices Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current[10]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	45		180	mA
I_{ODH}	Output HIGH Dynamic Current[10]	V_{CC}=3.3V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–45		–180	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}= –0.1 mA	V_{CC}–0.2			V
		V_{CC}=3.0V, I_{OH}= –8 mA	2.4[13]	3.0		V
		V_{CC}=3.0V, I_{OH}= –24 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}= 0.1mA			0.2	V
		V_{CC}=Min., I_{OL}= 24 mA		0.3	0.55	

Capacitance[9] (T_A = +25˚C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[8]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

12. Pins with bus hold are described in Pin Description.
13. V_{OH}=V_{CC} – 0.6V at rated current.

Power Supply Characteristics

Sym.	Parameter	Test Conditions[14]		Min.	Typ.[8]	Max.	Unit
I_{CCD}	Dynamic Power Supply Current[15]	V_{CC}=Max., Outputs Open OEAB=$\overline{OEBA}$=V_{CC} or GND One Input Toggling, 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[16]	V_{CC}=Max., Outputs Open f_0 =10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB = GND, One Bit Toggling f_1 = 5MHz, 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max., Outputs Open f_0 = 10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB=GND Eighteen Bits Toggling f_1=2.5MHz, 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	3.8	6.5[17]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.5	20.8[17]	

Notes:

14. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
15. This parameter is not directly testable, but is derived for use in Total Power Supply Current.
16. I_C= $I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
17. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range V_{CC}=3.0V to 3.6V[18]

Parameter	Description		CY74FCT163501C CY74FCT163H501C Min.	Max.	Unit	Fig.No.[19]
f_{MAX}	CLKAB or CLKBA frequency[9]		—	150	MHz	—
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A		1.5	4.6	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	5.3	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay CLKBA to A, CLKAB to B		1.5	5.3	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to A, OEAB to B		1.5	5.6	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to A, OEAB to B		1.5	5.2	ns	1,7,8
t_{SU}	Set-Up Time, HIGH or LOW A to CLKAB, B to CLKBA		3.0	—	ns	4
t_H	Hold Time HIGH or LOW A to CLKAB, B to CLKBA		0	—	ns	4
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock LOW	3.0	—	ns	4
		Clock HIGH	1.5	—	ns	4
t_H	Hold Time, HIGH or LOW, A to LEAB, B to LEBA		1.5	—	ns	4
t_W	LEAB or LEBA Pulse Width HIGH[9]		3.0	—	ns	5
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[9]		3.0	—	ns	5
$t_{SK(O)}$	Output Skew[20]		—	0.5	ns	—

Notes:

18. Minimum limits are specified, but not tested, on propagation delays.
19. See “Parameter Measurement Information” in the General Information section.
20. Skew between any two outputs of the same package switching in the same direction. This parameter ensured by design.

Ordering Information CY74FCT163501T

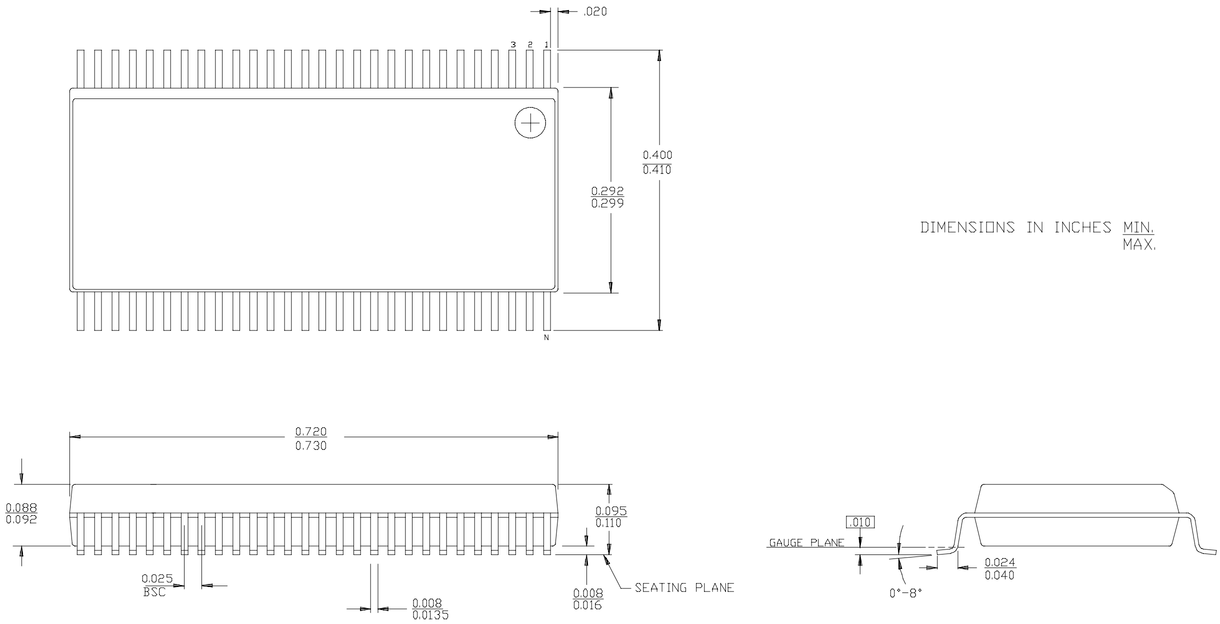
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT163501CPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163501CPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163H501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	74FCT163H501CPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H501CPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT163H501CPVCT	O56	56-Lead (300-Mil) SSOP	

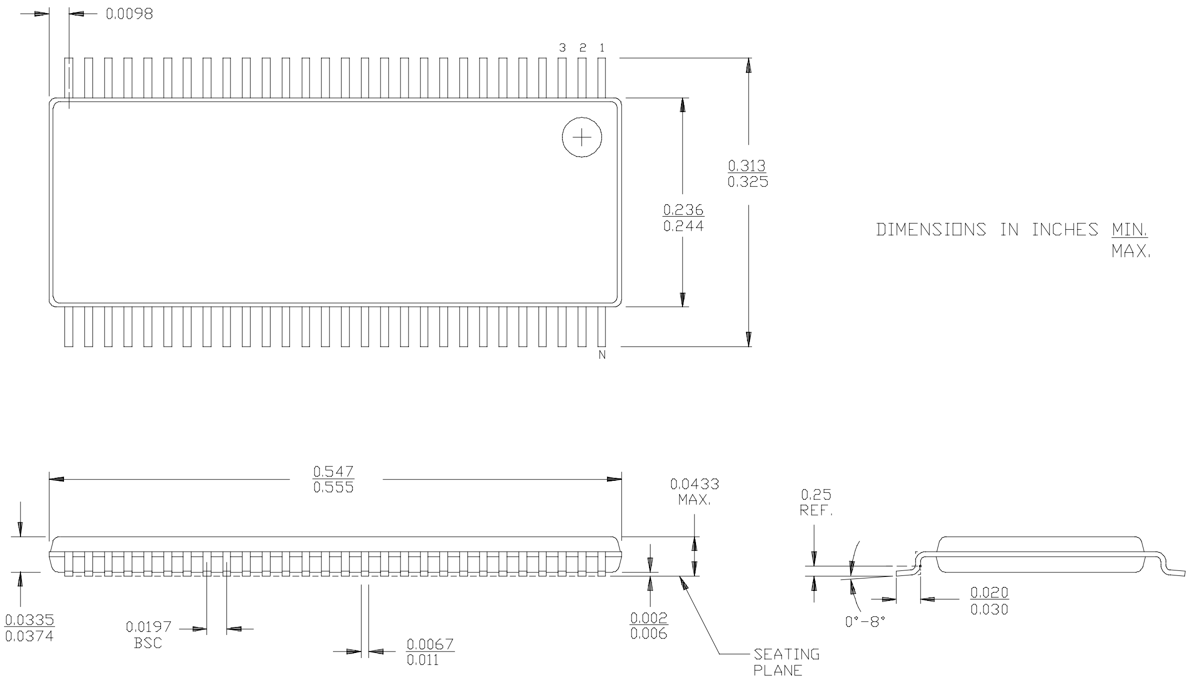
Package Diagrams

56-Lead Shrunk Small Outline Package O56



Package Diagrams (continued)

56-Lead Thin Shrunk Small Outline Package Z56



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