

SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

- Members of the Texas Instruments *Widebus*™ Family
- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

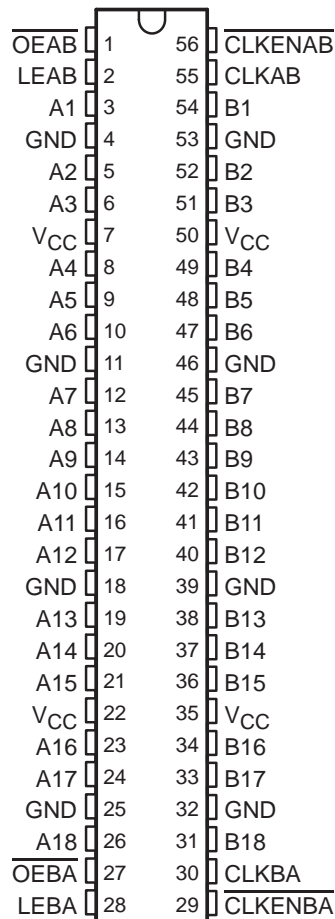
Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable \overline{OEAB} is active-low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and $\overline{CLKENBA}$.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT162601 . . . WD PACKAGE
SN74ABT162601 . . . DGG OR DL PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus, EPIC-II B, and UBT are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

description (continued)

The SN54ABT162601 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74ABT162601 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0^{\ddagger}
H	L	L	X	X	B_0^{\ddagger}
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0^{\ddagger}
L	L	L	H	X	B_0^{\S}

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

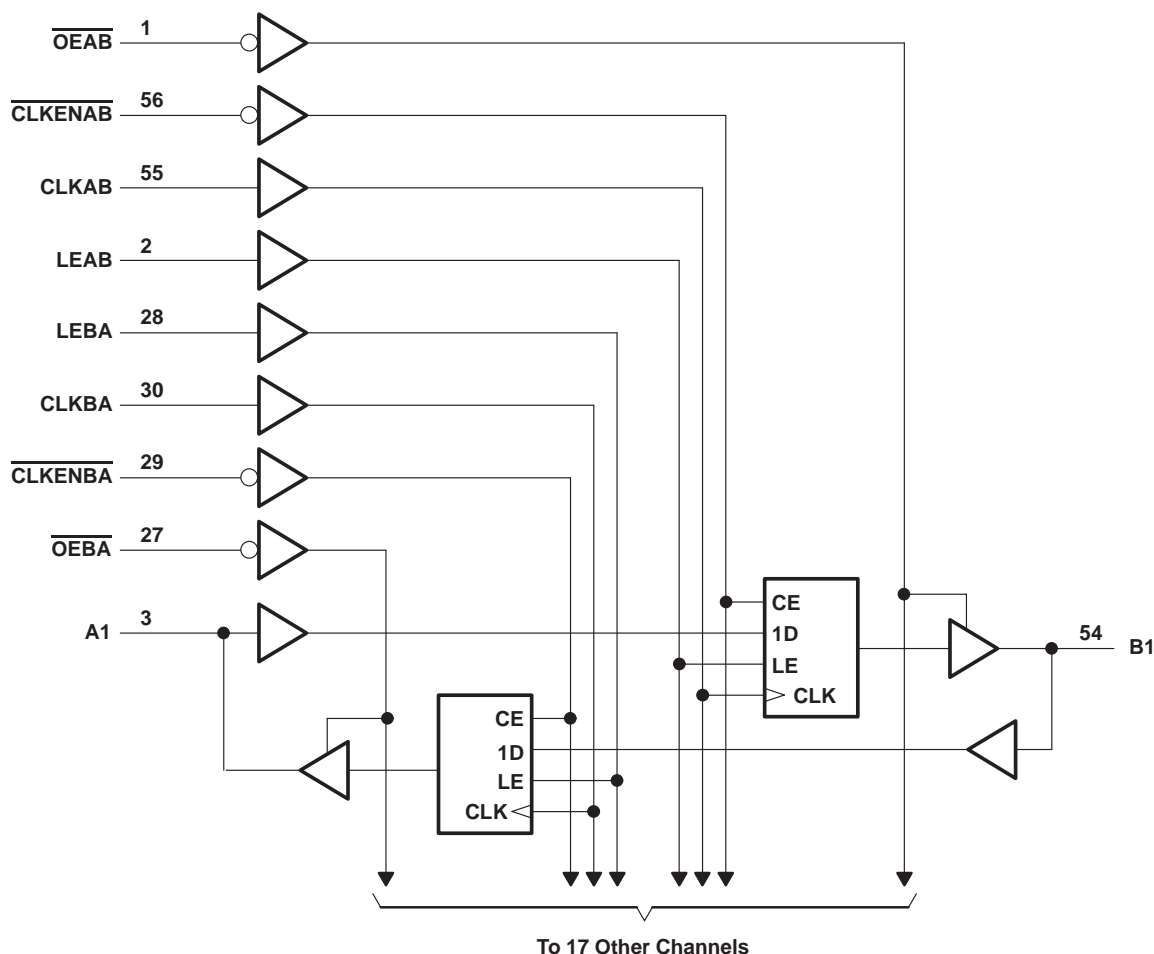
‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT162601 (A port)	96 mA
SN74ABT162601 (A port)	128 mA
B port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT162601, SN74ABT162601
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

recommended operating conditions (see Note 3)

		SN54ABT162601		SN74ABT162601		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	A port		–32		mA
		B port		–12		
I _{OL}	Low-level output current	A port		64		mA
		B port		12		
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the devices must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ABT162601, SN74ABT162601
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT162601		SN74ABT162601		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	A port	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5		2.5		2.5	V	
		V _{CC} = 5 V, I _{OH} = -3 mA		3		3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA		2		2				
		I _{OH} = -32 mA		2*				2		
	B port	V _{CC} = 4.5 V, I _{OH} = -1 mA		3.35		3.3		3.35		
		V _{CC} = 5 V, I _{OH} = -1 mA		3.85		3.8		3.85		
V _{CC} = 4.5 V		I _{OH} = -3 mA		3.1		3		3.1		
	I _{OH} = -12 mA		2.6				2.6			
V _{OL}	A port	V _{CC} = 4.5 V	I _{OL} = 48 mA				0.55		V	
			I _{OL} = 64 mA				0.55*			0.55
	B port	V _{CC} = 4.5 V, I _{OL} = 12 mA				0.8		0.8		
V _{hys}			100					mV		
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND				±1		±1	μA	
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND				±20		±20		
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$				±50		±50**	±50	μA	
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$				±50		±50**	±50	μA	
I _{OZH} ‡	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2 V$				10		10	10	μA	
I _{OZL} ‡	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2 V$				-10		-10	-10	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100*			±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high				50		50	μA	
I _O §	A port	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180		-50	-180	mA	
	B port		-25	-55	-100		-25	-100		
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high				3		3	mA
			Outputs low				36		36	
			Outputs disabled				3		3	
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				50		50		50	μA
C _i	Control inputs	V _I = 2.5 V or 0.5 V				3			pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V				9			pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Figure 1)

		SN54ABT162601		SN74ABT162601		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high		2.5		ns
		CLKAB or CLKBA high or low		3.3		
t_{su}	Setup time	A before CLKAB \uparrow or B before CLKBA \uparrow		4.8		ns
		A before LEAB \downarrow or B before LEBA \downarrow	CLK high	2.5		
			CLK low	1.2		
		CLKEN before CLK \uparrow		2.7		
t_h	Hold time	A after CLKAB \uparrow or B after CLKBA \uparrow		0.5		ns
		A after LEAB \downarrow or B after LEBA \downarrow		2		
		CLKEN after CLK \uparrow		0.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

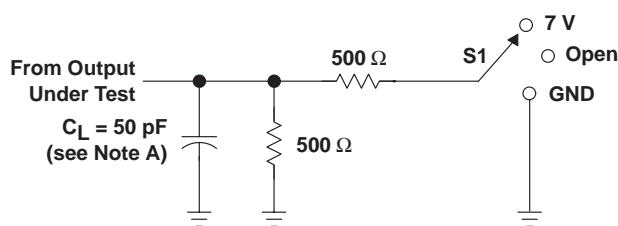
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT162601		SN74ABT162601		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	A	B	1.5	2.8	4	1.5	5.1	1.5	4.8	ns
t_{PHL}			2	3.7	5.2	2	6.1	2	5.7	
t_{PLH}	B	A	1	2.5	3.6	1	4.5	1	4	ns
t_{PHL}			2	3.3	4.5	2	5.1	2	4.9	
t_{PLH}	LEBA	A	2	3.3	4.5	2	5.6	2	5	ns
t_{PHL}			2	3.6	4.7	2	5.4	2	5	
t_{PLH}	LEAB	B	2	3.4	4.8	2	6.1	2	5.6	ns
t_{PHL}			2	3.8	5.2	2	6.4	2	5.9	
t_{PLH}	CLKBA	A	1.5	3.1	4.7	1.5	5.4	1.5	5.3	ns
t_{PHL}			1.5	3.1	4.3	1.5	5.2	1.5	5	
t_{PLH}	CLKAB	B	1.5	3.3	4.7	1.5	6	1.5	5.5	ns
t_{PHL}			1.5	3.5	4.8	1.5	5.8	1.5	5.3	
t_{PZH}	$\overline{\text{OEBA}}$	A	2	3.5	4.6	2	5.5	2	5.1	ns
t_{PZL}			2	3.7	4.7	2	5.8	2	5.4	
t_{PZH}	$\overline{\text{OEAB}}$	B	2	3.8	5.3	1.5	6.6	2	6.1	ns
t_{PZL}			2	3.6	5.1	2	6.2	2	5.7	
t_{PHZ}	$\overline{\text{OEBA}}$	A	2	3.6	5.4	1.4	6.6	2	6.2	ns
t_{PLZ}			1.5	3.2	4.7	1.5	5.8	1.5	5.4	
t_{PHZ}	$\overline{\text{OEAB}}$	B	2	3.4	4.8	1.4	5.6	2	5.4	ns
t_{PLZ}			1.5	3.2	4.5	1.5	5.7	1.5	5.2	



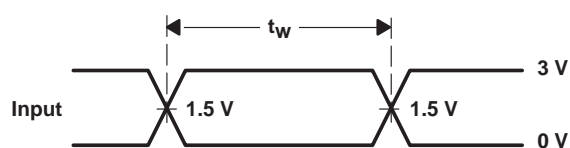
SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

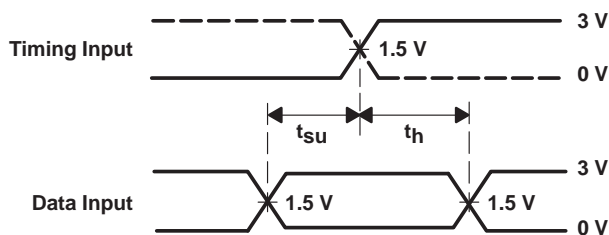
PARAMETER MEASUREMENT INFORMATION



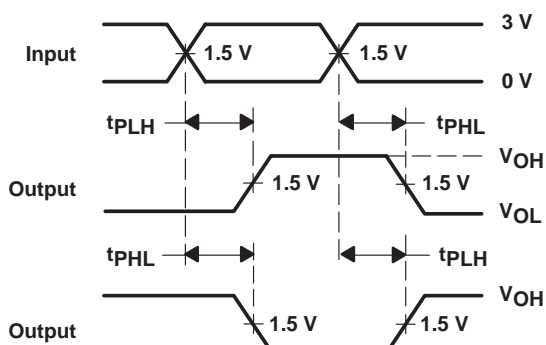
LOAD CIRCUIT



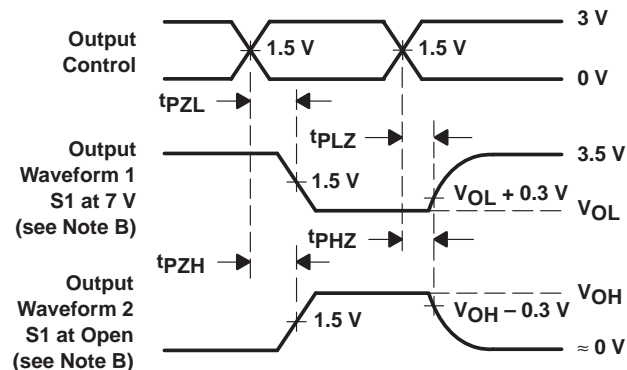
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.