

SN74ALVCH16500

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES023G – JULY 1995 – REVISED MAY 2000

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (\overline{LEAB} and \overline{LEBA}), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when \overline{LEAB} is high. When \overline{LEAB} is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If \overline{LEAB} is low, the A data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . Output-enable \overline{OEAB} is active high. When \overline{OEAB} is high, the B-port outputs are active. When \overline{OEAB} is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , \overline{LEBA} , and \overline{CLKBA} . The output enables are complementary (\overline{OEAB} is active high, and \overline{OEBA} is active low).

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor and \overline{OEAB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

\overline{OEAB}	1		56	\overline{GND}
\overline{LEAB}	2		55	\overline{CLKAB}
A1	3		54	B1
\overline{GND}	4		53	\overline{GND}
A2	5		52	B2
A3	6		51	B3
V_{CC}	7		50	V_{CC}
A4	8		49	B4
A5	9		48	B5
A6	10		47	B6
\overline{GND}	11		46	\overline{GND}
A7	12		45	B7
A8	13		44	B8
A9	14		43	B9
A10	15		42	B10
A11	16		41	B11
A12	17		40	B12
\overline{GND}	18		39	\overline{GND}
A13	19		38	B13
A14	20		37	B14
A15	21		36	B15
V_{CC}	22		35	V_{CC}
A16	23		34	B16
A17	24		33	B17
\overline{GND}	25		32	\overline{GND}
A18	26		31	B18
\overline{OEBA}	27		30	\overline{CLKBA}
\overline{LEBA}	28		29	\overline{GND}



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FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	O	L	L
H	L	↓	H	H
H	L	H	X	B ₀ ‡
H	L	L	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

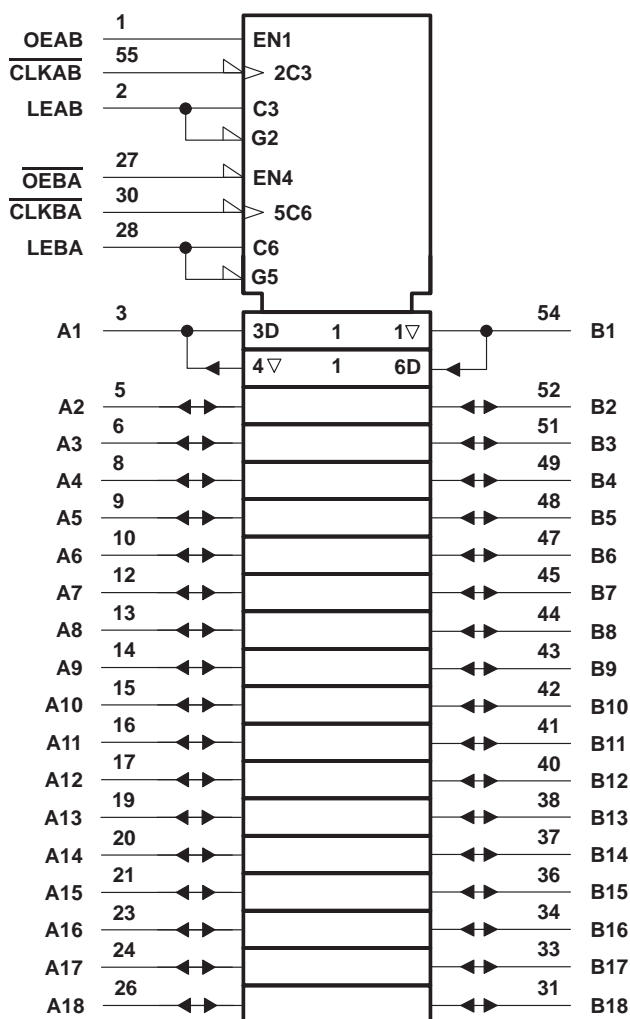


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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

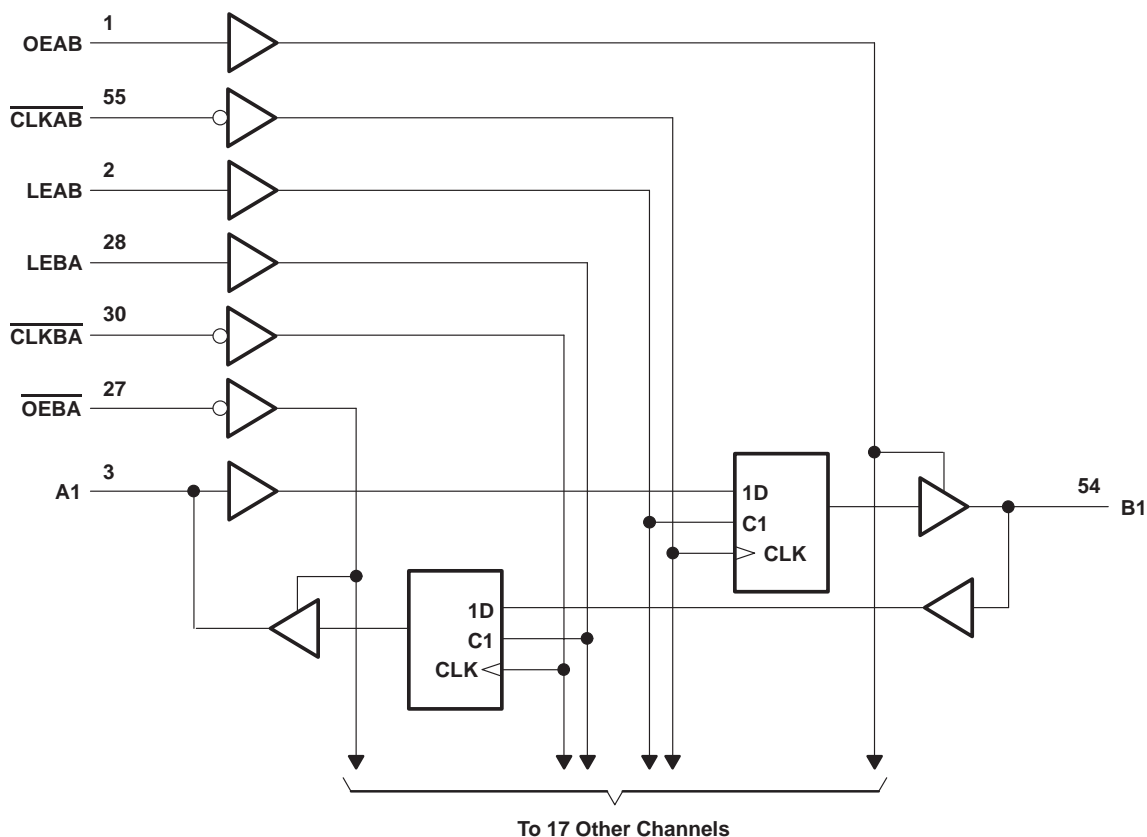
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through each V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-4	mA
		V _{CC} = 2.3 V	-12	
		V _{CC} = 2.7 V	-12	
		V _{CC} = 3 V	-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	12	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -6 mA	2.3 V	2			
	I _{OH} = -12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
I _{OH} = -24 mA	3 V	2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 6 mA	2.3 V			0.4	
	I _{OL} = 12 mA	2.3 V			0.7	
		2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _I (hold)	V _I = 0.58 V	1.65 V	25			μA
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V	2.3 V	-45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	V _I = 0 to 3.6 V‡	3.6 V			±500	
I _{OZ} §	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		4	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		8	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	†		150		150		150		MHz	
t _w	Pulse duration	LE high		†		3.3		3.3		ns	
		CLK high or low		†		3.3		3.3			
t _{su}	Setup time	Data before CLK↓		†		1.7		1.4		ns	
		Data before LE↓	CLK high		†		1.1		1		
			CLK low		†		1.9		1.6		
t _h	Hold time	Data after CLK↓		†		1.7		1.6		ns	
		Data after LE↓	CLK high		†		2		1.8		
			CLK low		†		1.6		1.5		

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	A or B	B or A	†		1	5.1	4.7		1	3.9	ns
	LEAB or LEBA	A or B	†		1	5.9	5.5		1	4.7	
	CLKAB or CLKBA		†		1	6.6	6.6		1.1	5.5	
t _{en}	OEAB	B	†		1	5.7	5.4		1	4.6	ns
t _{dis}	OEAB	B	†		1	6.1	5.7		1.5	5	ns
t _{en}	OEBA	A	†		1	6.2	6.2		1	5.2	ns
t _{dis}	OEBA	A	†		1	5.4	4.6		1	4.3	ns

† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	Outputs enabled	†	40	51	pF
		Outputs disabled	†	6	6	

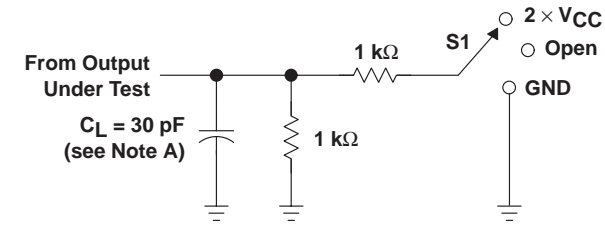
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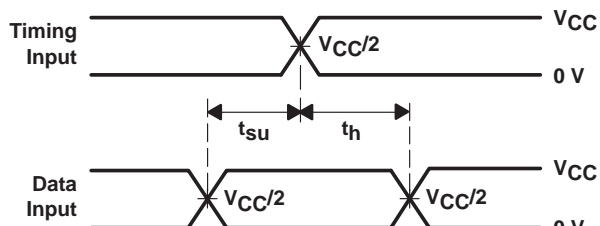
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PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V}$

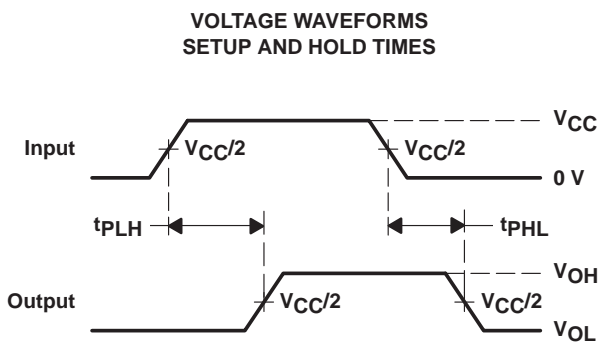


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



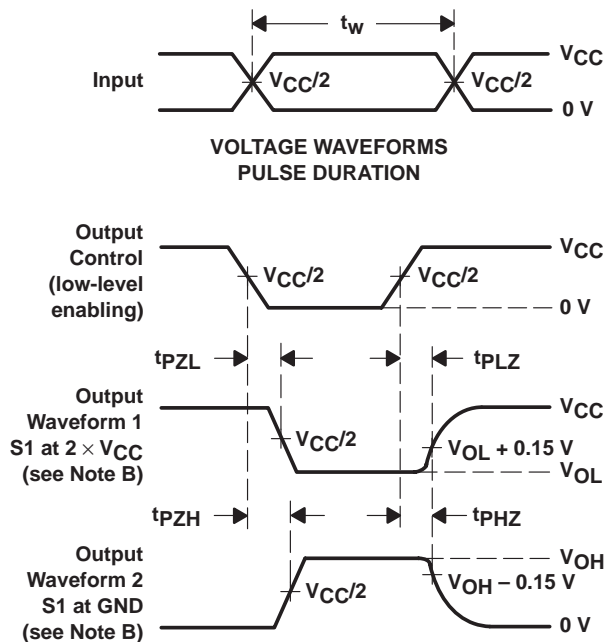
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

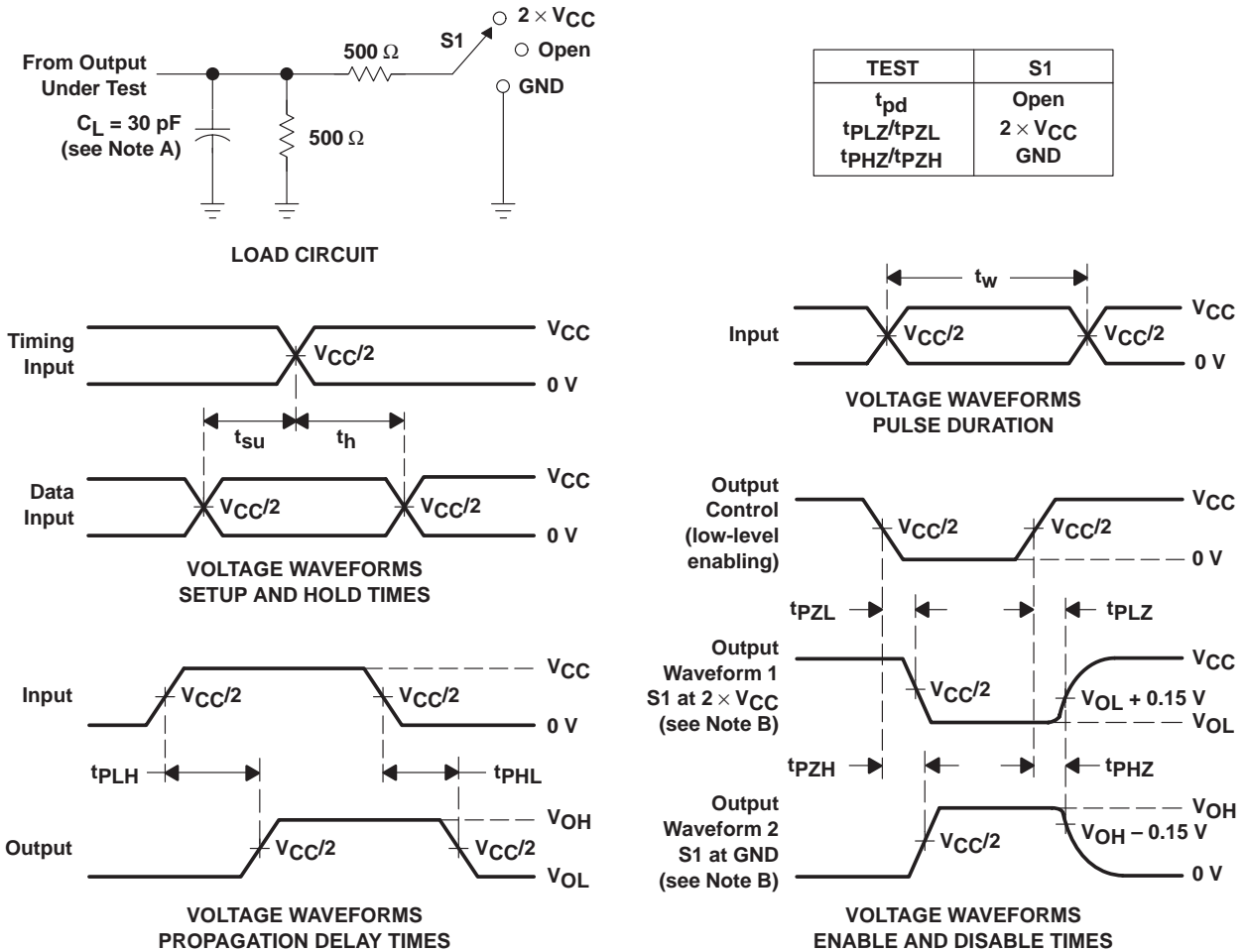


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PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



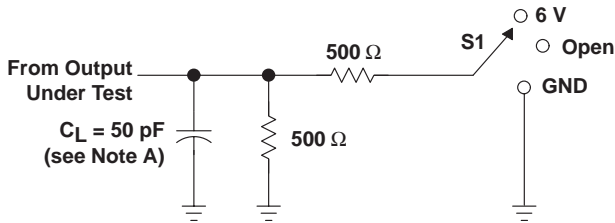
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 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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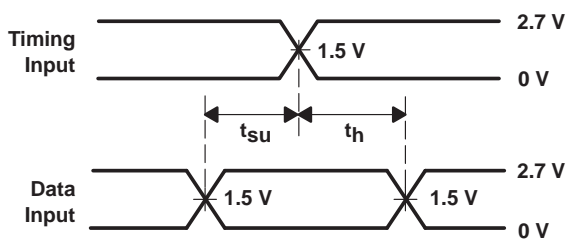
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PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

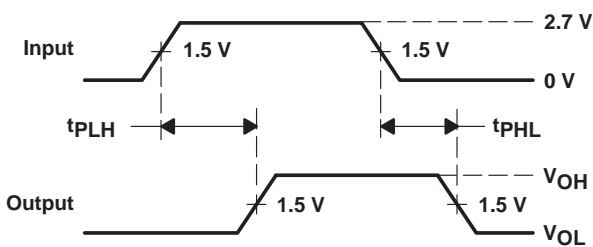


LOAD CIRCUIT

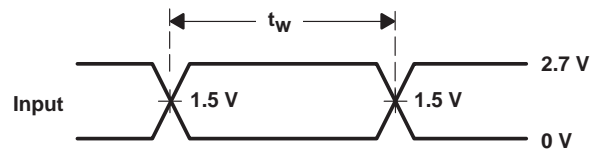
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



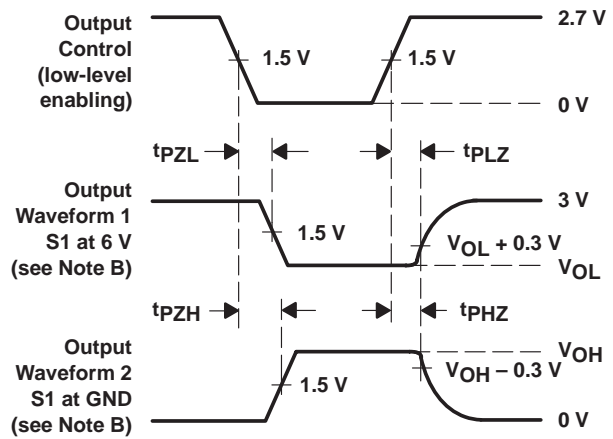
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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