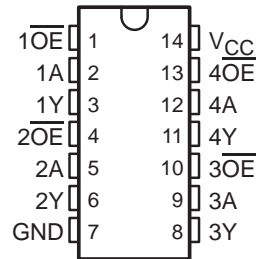


SN64BCT125A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCBS052B – JULY 1990 – REVISED MAY 1994

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- High-Impedance State During Power-Up and Power-Down
- 3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)

D OR N PACKAGE
(TOP VIEW)



description

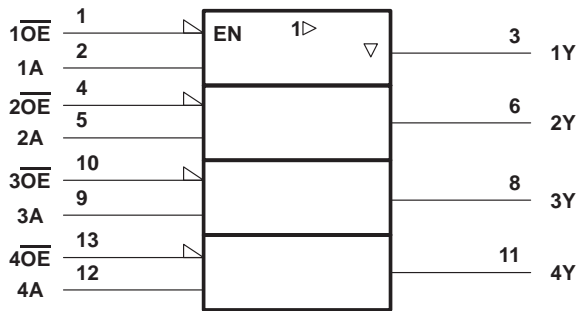
The SN64BCT125A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

The SN64BCT125A is characterized for operation from -40°C to 85°C and 0°C to 70°C .

FUNCTION TABLE
(each buffer)

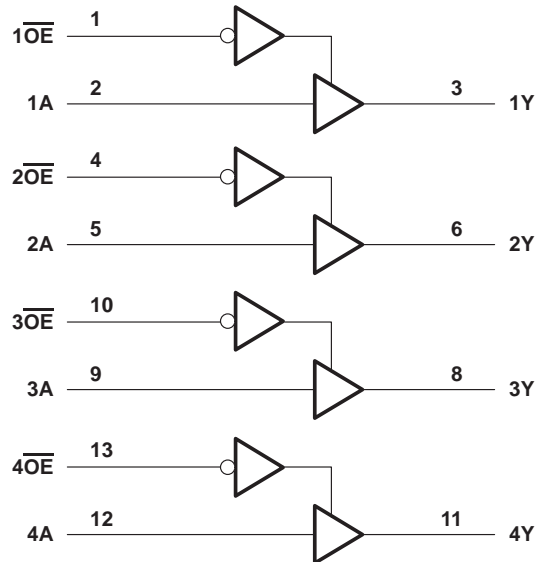
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN64BCT125A

QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range, V_I (see Note 1)	– 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	– 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	– 0.5 V to V_{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	– 40°C to 85°C
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{IK} Input clamp current			–18	mA
I_{OH} High-level output current			–15	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.3	V
		$I_{OH} = -15$ mA	2	3.1	
V_{OL}	$V_{CC} = 4.5$ V, $I_{OH} = 64$ mA		0.42	0.55	V
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50	μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.5$ V			–50	μA
I_{OZ}	$V_{CC} = 0$ to 1.3 V (power up) $V_{CC} = 1.3$ V to 0 (power down)	$V_O = 2.7$ V or 0.5 V, \overline{OE} at 0.8 V		± 50	μA
				± 50	
I_I	$V_{CC} = 0$, $V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			25	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.5$ V			–20	μA
I_{OS}^{\S}	$V_{CC} = 5.5$ V, $V_O = 0$	–100		–225	mA
I_{CCL}	$V_{CC} = 5.5$ V		46	49	mA
I_{CCH}	$V_{CC} = 5.5$ V		19	31	mA
I_{CCZ}	$V_{CC} = 5.5$ V		6	14	mA
C_i	$V_{CC} = 5$ V, $V_I = 2.5$ V or 0.5 V		4		pF
C_o	$V_{CC} = 5$ V, $V_O = 2.5$ V or 0.5 V		9		pF

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



SN64BCT125A
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS
 SCBS052B – JULY 1990 – REVISED MAY 1994

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
						T _A = -40°C to 85°C		T _A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t _{PHL}			2.7	5	6.9	2.7	8	2.7	7.7	
t _{PZH}	$\overline{\text{OE}}$	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t _{PZL}			5	8.2	10.4	5	12.8	5	11.7	
t _{PHZ}	$\overline{\text{OE}}$	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t _{PLZ}			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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