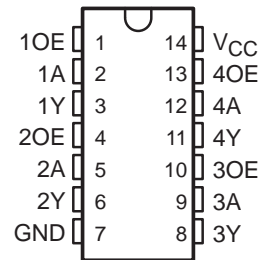


SN64BCT126A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCBS051C – AUGUST 1990 – REVISED JULY 1998

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-STD-883 Method 3015
- High-Impedance State During Power Up and Power Down
- Package Options Include Plastic Small-Outline (D) and Standard Plastic 300-mil DIPs (N)

D OR N PACKAGE
(TOP VIEW)



description

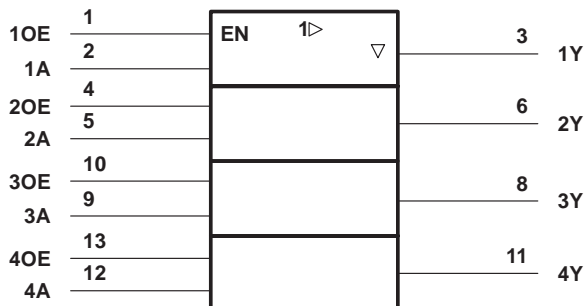
The SN64BCT126A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

The SN64BCT126A is characterized for operation from -40°C to 85°C and 0°C to 70°C .

FUNCTION TABLE
(each buffer)

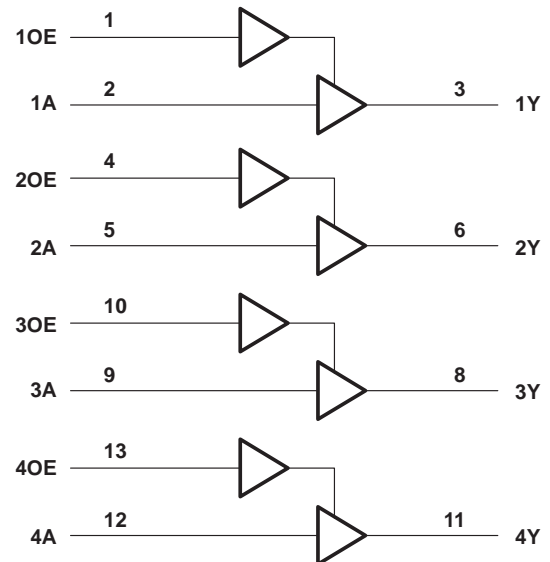
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

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SN64BCT126A

QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

SCBS051C – AUGUST 1990 – REVISED JULY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Current into any output in the low state, I_O	128 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
N package	78°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative voltage rating may be exceeded if the input clamp current rating is observed.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{IK} Input clamp current			-18	mA
I_{OH} High-level output current			-15	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN64BCT126A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
V _{OH}	V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4	3.3		V
		I _{OH} = -15 mA	2	3.1		
V _{OL}	V _{CC} = 4.5 V,	I _{OH} = 64 mA		0.42	0.55	V
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V			50	μA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.5 V			-50	μA
I _{OZ}	V _{CC} = 0 to 1.3 V (power up)	V _O = 2.7 V or 0.5 V, OE at 2 V			±50	μA
	V _{CC} = 1.3 V to 0 (power down)				±50	
I _I	V _{CC} = 0,	V _I = 7 V			0.1	mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V			25	μA
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.5 V			-20	μA
I _{OS} ‡	V _{CC} = 5.5 V,	V _O = 0	-100		-225	mA
I _{CCL}	V _{CC} = 5.5 V			35	51	mA
I _{CCH}	V _{CC} = 5.5 V			21	33	mA
I _{CCZ}	V _{CC} = 5.5 V			5	10	mA
C _i	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		4		pF
C _o	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		9		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Figure 1)

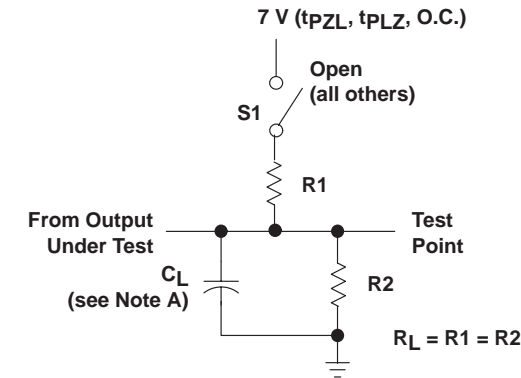
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω				UNIT
						T _A = -40°C to 85°C		T _A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.5	3.6	4.9	1.5	6.3	1.5	6.3	ns
t _{PHL}			2.7	5.3	6.9	2.7	7.7	2.7	7.4	
t _{PZH}	OE	Y	2.6	4.8	6.4	2.6	7.9	2.6	7.9	ns
t _{PZL}			3.7	6.4	8.3	3.7	10.5	3.7	10	
t _{PHZ}	OE	Y	3.2	6.6	8.2	3.2	10	3.2	10	ns
t _{PLZ}			3.4	6.5	8	3.4	12.3	3.4	10.7	



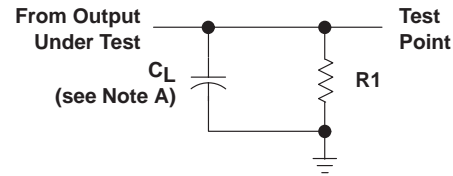
SN64BCT126A
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

SCBS051C – AUGUST 1990 – REVISED JULY 1998

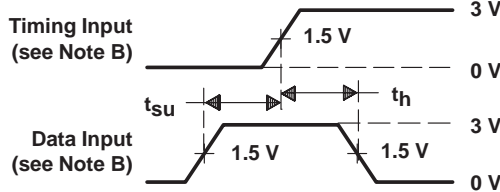
PARAMETER MEASUREMENT INFORMATION



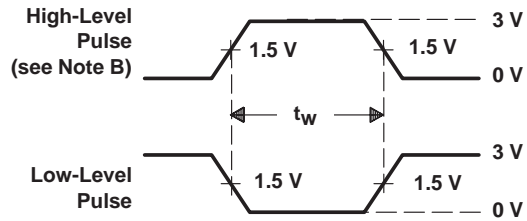
LOAD CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR OUTPUTS



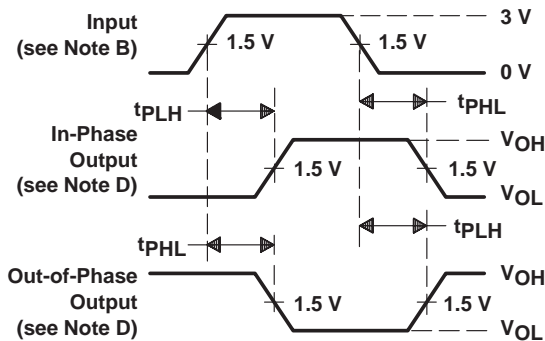
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



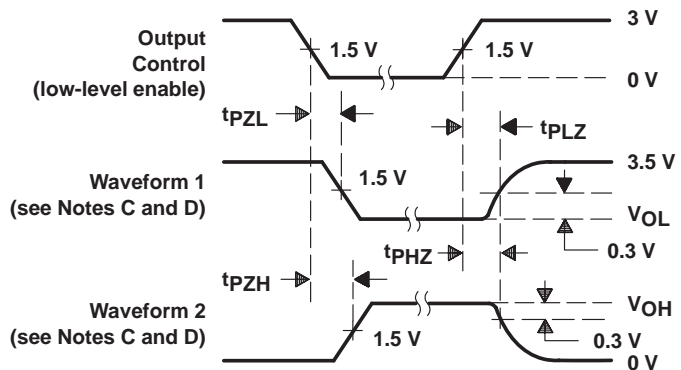
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuits and Voltage Waveforms



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