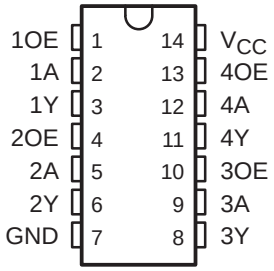
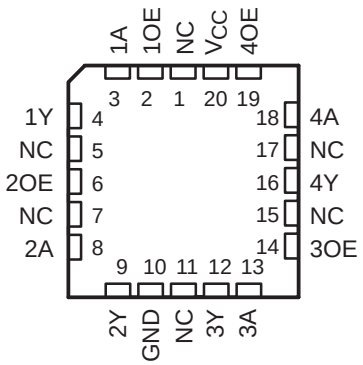
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs**

SN54ABT126 . . . J PACKAGE
SN74ABT126 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54ABT126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ABT126 bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

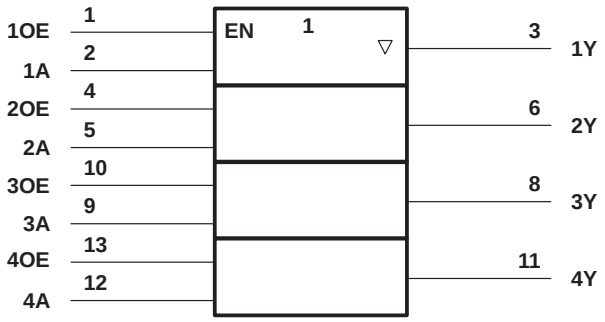
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT126 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

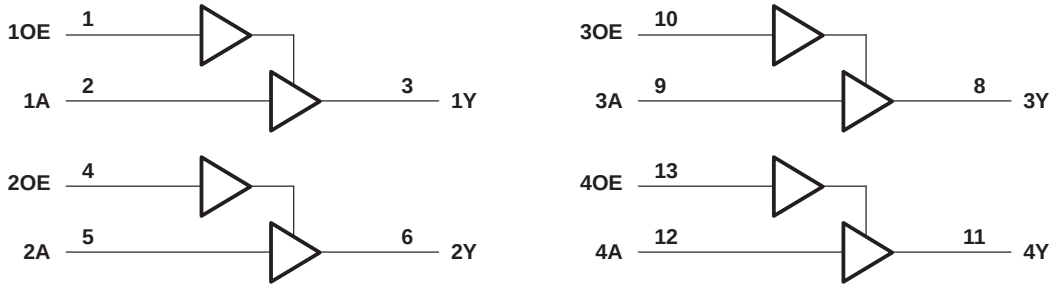
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT126 . . . . . 96 mA
SN74ABT126 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stressratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT126		SN74ABT126		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		µs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT126		SN74ABT126		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
		I_{OH} = –32 mA	2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
		I_{OL} = 64 mA			0.55*				0.55	
V_{hys}				100						mV
I_I	V_{CC} = 0 to 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZPU}	V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, OE = X‡				±50		±50		±50	µA
I_{OZPD}	V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, OE = X‡				±50		±50		±50	µA
I_{OZH}	V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, OE ≤ 0.8 V				10		10		10	µA
I_{OZL}	V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, OE ≤ 0.8 V				–10		–10		–10	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			7						pF

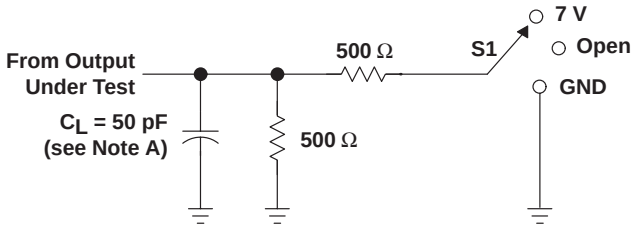
* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ For V_{CC} between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT126		SN74ABT126		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.9	4.9	1	7.3	1	6.3	ns
t_{PHL}			1	2.5	5.1	1	5.9	1	5.7	
t_{PZH}	OE	Y	1	4.4	5.8	1	5.3	1	6.5	ns
t_{PZL}			1	4.4	5.9	1	6.4	1	6.5	
t_{PHZ}	OE	Y	1	3	5.7	1	6.9	1	6.8	ns
t_{PLZ}			1	3	5.8	1	7.2	1	6.7	

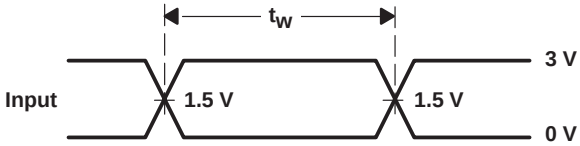
NOTE 4: Limits may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

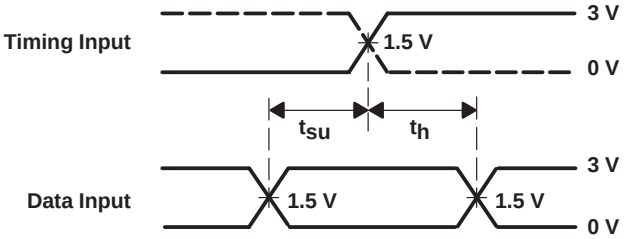


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

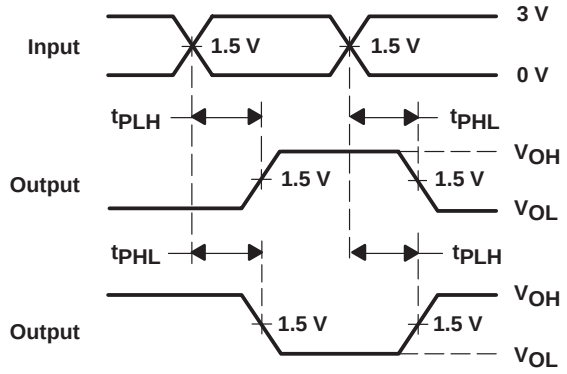
LOAD CIRCUIT



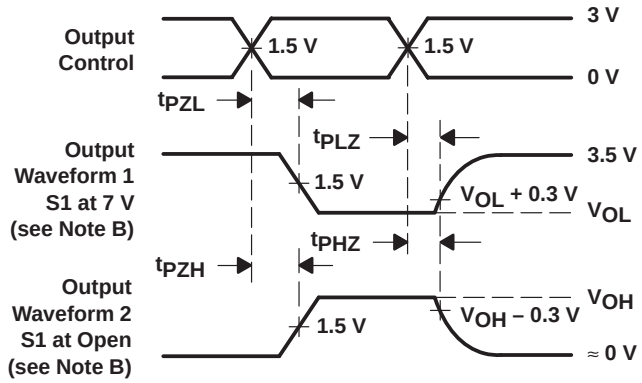
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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