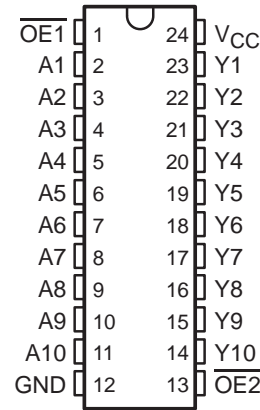


SN54ABT2827, SN74ABT2827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW) Package, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

SN54ABT2827 . . . JT PACKAGE
SN74ABT2827 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit buffers or bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

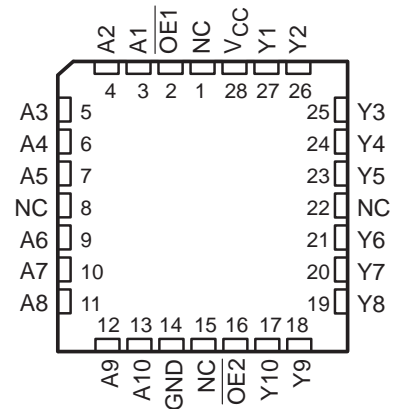
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The 'ABT2827 provide true data at their outputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

The SN54ABT2827 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT2827 is characterized for operation from -40°C to 85°C .

SN54ABT2827 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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EPIC-II B is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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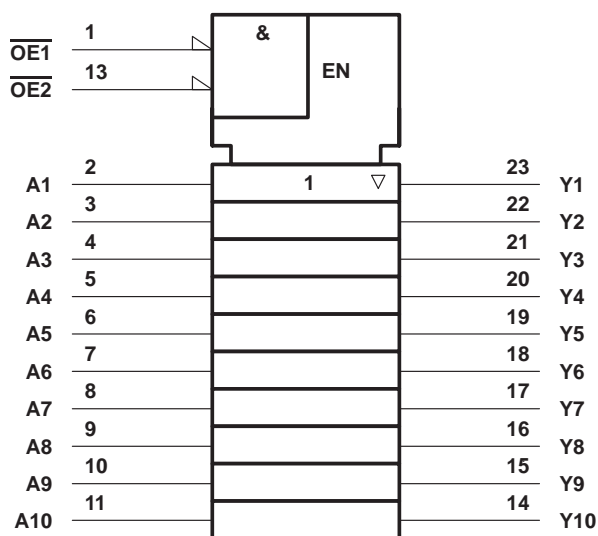
SN54ABT2827, SN74ABT2827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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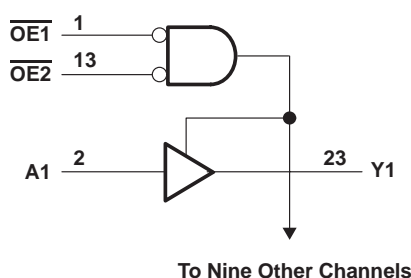
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT2827	96 mA
SN74ABT2827	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	81°C/W
NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



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recommended operating conditions (see Note 3)

		SN54ABT2827		SN74ABT2827		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-12		-12	mA
I _{OL}	Low-level output current		12		12	mA
Δt/Δv	Input transition rise or fall rate		5		5	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT2827		SN74ABT2827		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.5			2.5		2.5		V	
	V _{CC} = 5 V, I _{OH} = -1 mA	3			3		3			
	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.4			2.4		2.4			
				I _{OH} = -12 mA	2		2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA			0.8		0.8		0.8	V	
V _{hys}			100						mV	
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10‡		10		10‡	μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-10‡		-10		-10‡	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50		50		50	μA	
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-140	-225‡		-50	-225‡	-50	-225‡	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		80	250	250		250	μA	
		Outputs low		35	40‡	40‡		40‡	mA	
		Outputs disabled		80	250	250		250	μA	
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled			1.5	1.5		1.5	mA	
		Outputs disabled			50	50		50	μA	
		Control inputs			1.5	1.5		1.5	mA	
C _i	V _I = 2.5 V or 0.5 V			4					pF	
C _o	V _O = 2.5 V or 0.5 V			8.5					pF	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This data sheet limit may vary among suppliers.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54ABT2827, SN74ABT2827
10-BIT BUFFERS/DRIVERS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $T_A = 25^\circ\text{C}$			SN54ABT2827		SN74ABT2827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	3.3	5.1	1.1	5.6	1.1	5.5	ns
t_{PHL}			1.1	2.7	4.5	1.1	5.2	1.1	5.1	
t_{PZH}	\overline{OE}	Y	1	4	5.9	1	6.8	1	6.7	ns
t_{PZL}			1	4.2	6.8	1	8	1	7.8	
t_{PHZ}	\overline{OE}	Y	2	5.3	6.7	2	7.4	2	7.2	ns
t_{PLZ}			1.3	4.8	7.2	1.3	8.5	1.3	7.5	

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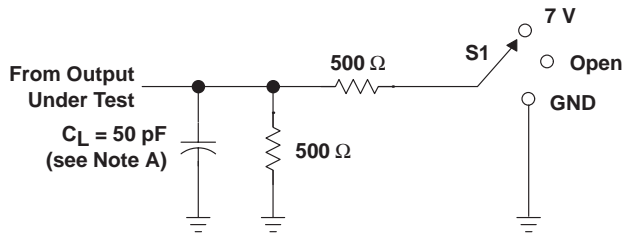


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SN54ABT2827, SN74ABT2827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

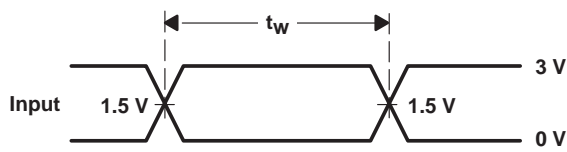
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PARAMETER MEASUREMENT INFORMATION

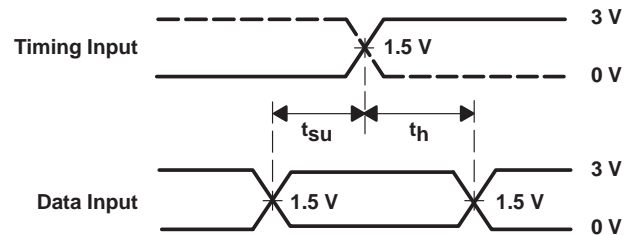


LOAD CIRCUIT

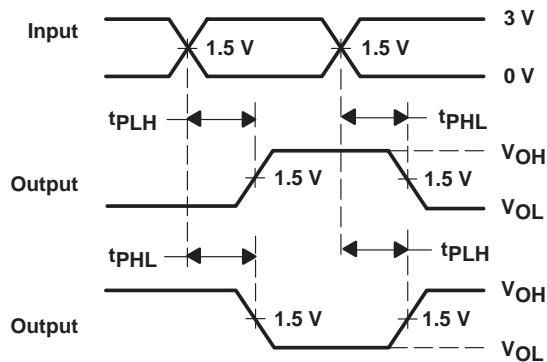
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



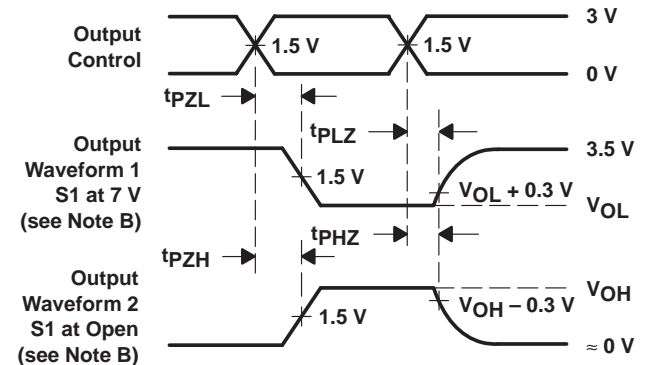
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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