SCBS647C - AUGUST 1995 - REVISED JULY 1997

- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation
- Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot
- Industry Standard '16244 Pinout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

The SN74ALB16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Υ
L	Н	Н
L	L	L
Н	X	Z

DGG OR DL PACKAGE (TOP VIEW)

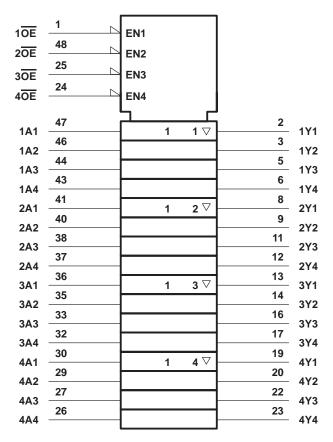
- 1		П		1	
d	1	\cup	48	_	2 <mark>OE</mark>
	2		47		1A1
	3		46	0	1A2
	4		45	0	GND
	5		44	1	1A3
	6		43	1	1A4
	7		42	1	V_{CC}
	8		41		2A1
	9		40	0	2A2
	10		39	0	GND
	11		38	0	2A3
	12		37		2A4
Q	13		36	þ	3A1
	14		35	þ	3A2
	15		34	þ	GND
	16		33	1	3A3
	17		32	1	3A4
	18		31	1	V_{CC}
	19		30	1	4A1
	20		29	1	4A2
	21		28	0	GND
	22		27		4A3
	23		26		4A4
4	24		25	P	3OE
		5 6 7 8 9 10 11 12 13 14 16 17 17 18 19 19 10 20 10 21 22 23	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 19 20 21 22 23	2 47 3 46 4 45 5 44 6 43 7 42 8 41 9 40 10 39 11 38 12 37 13 36 14 35 15 34 16 33 17 32 18 31 17 32 18 31 19 30 20 29 21 28 22 27 23 26	2 47 3 46 4 45 5 44 6 43 7 42 8 41 9 40 10 39 11 38 12 37 13 36 14 35 15 34 16 33 17 32 18 31 19 30 20 29 21 28 22 27 23 26

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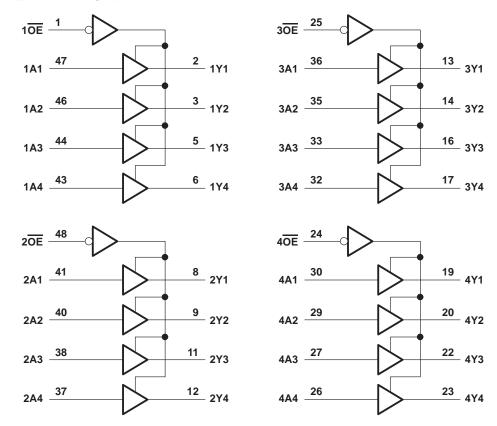
logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V_{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALB16244 **16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS**

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recommended operating conditions

			MIN	MAX	UNIT
VCC	CC Supply voltage		3	3.6	V
I _{OH} †	High-level output current			-25	mA
I _{OL} †	I _{OL} † Low-level output current			25	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5	ns/V
TA	Operating free-air temperature		-40	85	°C

[†] Refer to Figures 1 and 2 for typical I/O ranges.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
Vinc	Data innuta	V _{CC} = 3 V	I _I = 18 mA			3.6	V _{CC} -1.2	V
V _{IK} Data inputs		ACC = 2 A	$I_1 = -18 \text{ mA}$	I _I = -18 mA		-0.9	-1.2	V
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GNI)			±10	μΑ
I _I Data inputs		V _{CC} = 3.6 V	V V.	OE low		0.4	0.6	mA
	Data inpute		$A^{I} = A^{CC}$	OE high			25	μΑ
	Data inputs		V _I = 0	OE low		-0.8	-1	mA
			V = 0	OE high			-60	μΑ
lozh		$V_{CC} = 3.6 \text{ V},$	V _O = 3 V			0.6	20	μΑ
lozL		$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$			-0.1	- 50	μΑ
ICC/bu	ffer	V _{CC} = 3.6 V,	$I_{O} = 0$,	$V_I = V_{CC}$ or GND		3.7	5.6	mA
Iccz Vc		V _{CC} = 3.6 V,	Control inputs = '	Control inputs = V_{CC} or GND			0.8	mA
			V_{CC} = 3 V to 3.6 V, One input at V_{CC} –0.6 V, Other inputs at V_{CC} or GND				600	μΑ
$V_{l} = 3 \text{ V or } 0$		·			4.5	·	pF	
Co		$V_O = 3 \text{ V or } 0$				5.5	·	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	ТО	V_{CC} = 3.3 V \pm 0.3 V			UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP‡	MAX	UNIT
^t pd	А	Y	0.6	1.3	2	ns
t _{en}	ŌĒ	Y	1.3	2.5	4.7	ns
^t dis	ŌĒ	Υ	1.8	2.8	4.2	ns

[‡] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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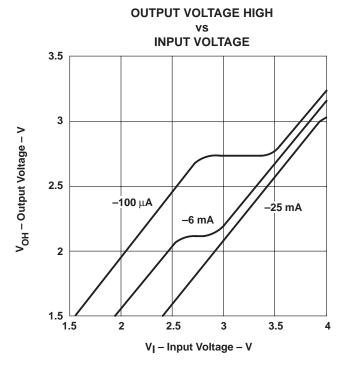


Figure 1. $V_{\mbox{OH}}$ Over Recommended Free-Air Temperature Range

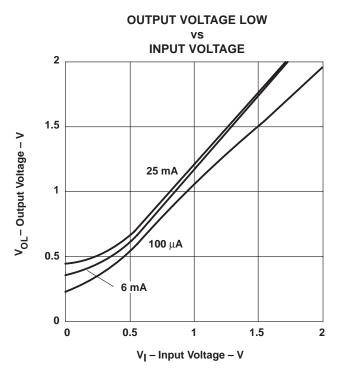
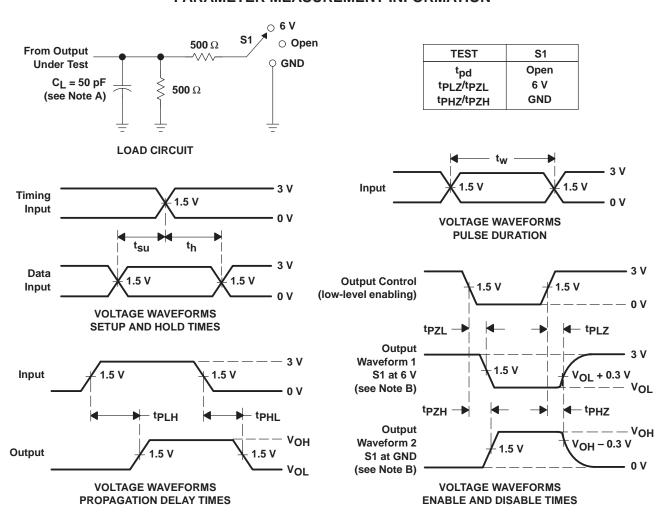


Figure 2. $V_{\mbox{\scriptsize OL}}$ Over Recommended Free-Air Temperature Range



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,$ ns, $t_f \leq 2.5 \,$ ns,
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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