

# SN54HCT125, SN74HCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCLS069C – NOVEMBER 1988 – REVISED MAY 1997

- Inputs Are TTL-Voltage Compatible
- High-Current 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

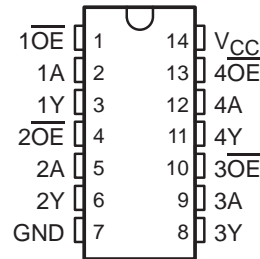
These bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

The SN54HCT125 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HCT125 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

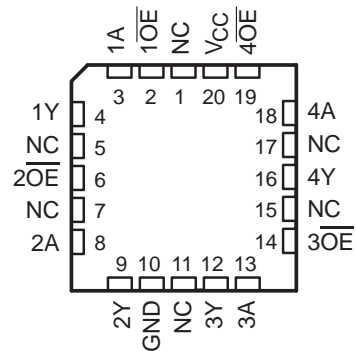
FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

SN54HCT125 . . . J OR W PACKAGE  
SN74HCT125 . . . D OR N PACKAGE  
(TOP VIEW)

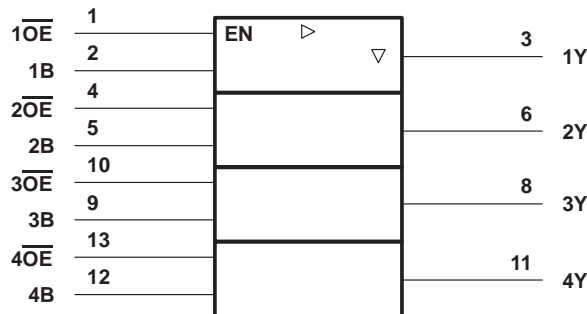


SN54HCT125 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, and W packages.



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**TEXAS  
INSTRUMENTS**

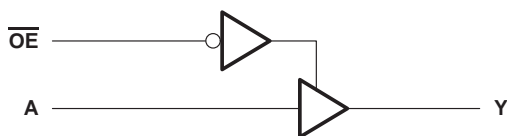
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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	127°C/W
N package .....	78°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

		SN54HCT125			SN74HCT125			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to $5.5$ V			2			V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to $5.5$ V			0			V
$V_I$	Input voltage	0			$V_{CC}$			V
$V_O$	Output voltage	0			$V_{CC}$			V
$t_t$	Input transition (rise and fall) time	0			500			ns
$T_A$	Operating free-air temperature	-55			125			°C

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
		I <sub>OH</sub> = -6 mA		3.98	4.3		3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1		0.1		V	
		I <sub>OL</sub> = 6 mA			0.17	0.26		0.4			0.33
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		5.5 V		±0.01	±0.5		±10		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V			8		160		80	μA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>		5.5 V		1.4	2.4		3		2.9	mA
C <sub>i</sub>			4.5 V to 5.5 V		3	10		10*		10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	4.5 V		15	26		39		33	ns
			5.5 V		12	23		35		30	
t <sub>en</sub>	$\overline{\text{OE}}$	Y	4.5 V		18	28		42		35	ns
			5.5 V		15	25		38		31	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	4.5 V		15	26		39		33	ns
			5.5 V		13	23		35		30	
t <sub>t</sub>		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 150 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	4.5 V		19	36		58		46	ns
			5.5 V		16	32		48		42	
t <sub>en</sub>	$\overline{\text{OE}}$	Y	4.5 V		25	40		60		50	ns
			5.5 V		21	35		53		43	
t <sub>t</sub>		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load	35	pF

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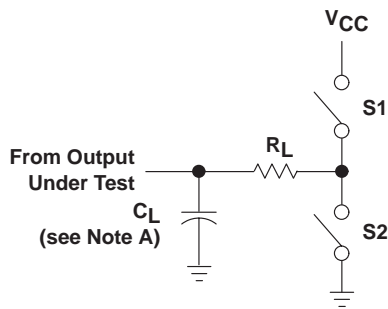


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# SN54HCT125, SN74HCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

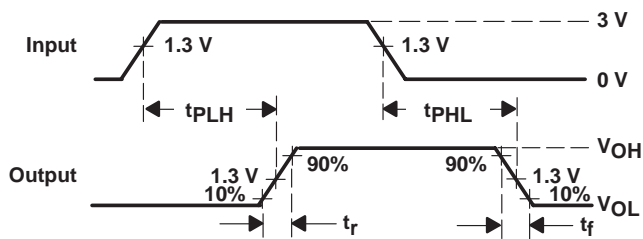
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## PARAMETER MEASUREMENT INFORMATION

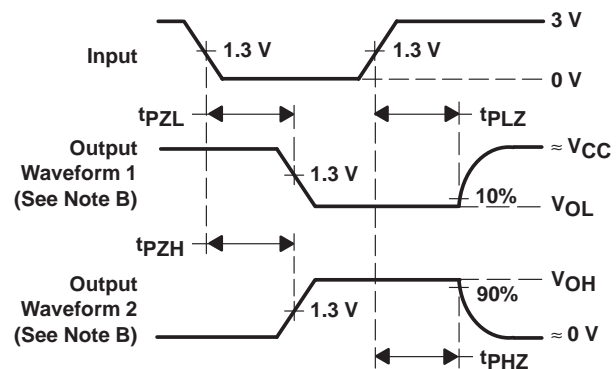


LOAD CIRCUIT

PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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