- Member of the Texas Instruments *Widebus*™ Family

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process

- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C

- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C

- I_{off} and Power-Up 3-State Support Hot Insertion

- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
  – 200-V Machine Model (A115-A)
  – 1000-V Charged-Device Model (C101)

- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	2$\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{OE}$	24	25	3$\overline{OE}$
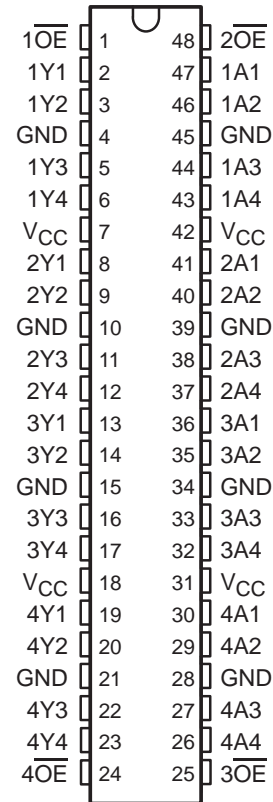
description

This 16-bit buffer/driver is designed for 3-V to 3.6-V V_{CC} operation.

The SN74LVCZ16244A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN74LVCZ16244A is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
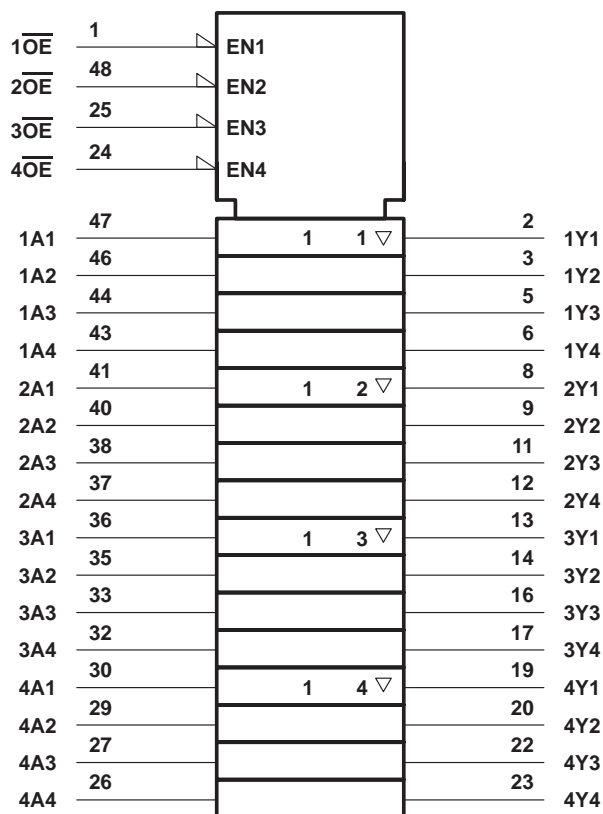
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SN74LVCZ16244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES277B – JUNE 1999 – REVISED MARCH 2000

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)
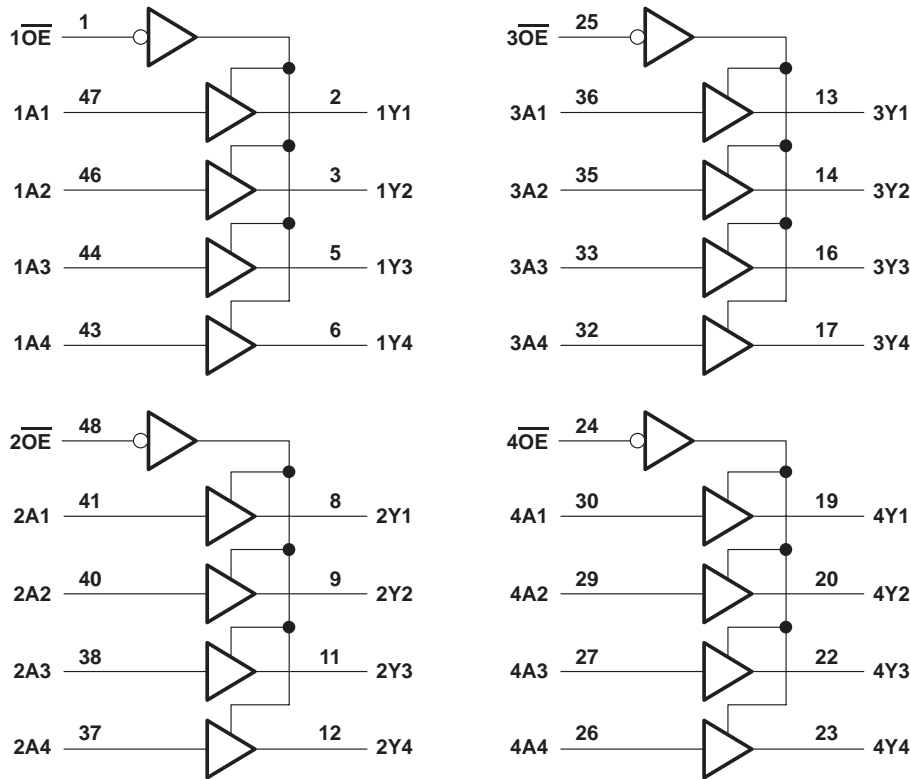
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) .... −0.5 V to 6.5 V

Voltage range applied to any output in the high or low state, V_O
(see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA

Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA

Continuous output current, I_O .... ±50 mA

Continuous current through each V_{CC} or GND .... ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): DGG package .... 70°C/W
DL package .... 63°C/W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 3 V to 3.6 V		0.8	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 3 V		−24	mA
I_{OL}	Low-level output current	V_{CC} = 3 V		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		150		µs/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	I_{OH} = −100 µA		3 V to 3.6 V	V_{CC}−0.2			V
	I_{OH} = −12 mA		3 V	2.4			
	I_{OH} = −24 mA		3 V	2.2			
V_{OL}	I_{OL} = 100 µA		3 V to 3.6 V			0.2	V
	I_{OL} = 12 mA		3 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±5	µA
I_{off}	V_I or V_O = 5.5 V		0			±5	µA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±5	µA
I_{OZPU}	V_O = 0.5 to 2.5 V,	$\overline{OE}$ = don't care	0 to 1.5 V			±5	µA
I_{OZPD}	V_O = 0.5 to 2.5 V,	$\overline{OE}$ = don't care	1.5 V to 0			±5	µA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			100	µA
	3.6 V ≤ V_I ≤ 5.5 V‡					100	
ΔI_{CC}	One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			100	µA
C_i	V_I = V_{CC} or GND		3.3 V		4.5		pF
C_o	V_O = V_{CC} or GND		3.3 V		6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
t_{pd}	A or B	B or A	1.1	4.1	ns
t_{en}	$\overline{OE}$	A or B	1	4.6	ns
t_{dis}	$\overline{OE}$	A or B	1.8	5.8	ns

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operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	32	pF
	Outputs disabled		5.5	

PARAMETER MEASUREMENT INFORMATION
$V_{CC} = 3.3\ V \pm 0.3\ V$
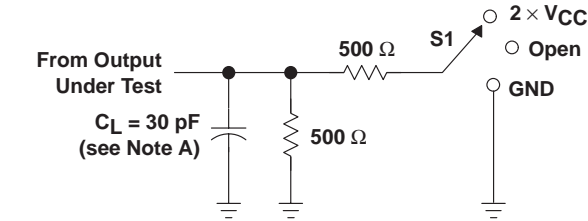
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
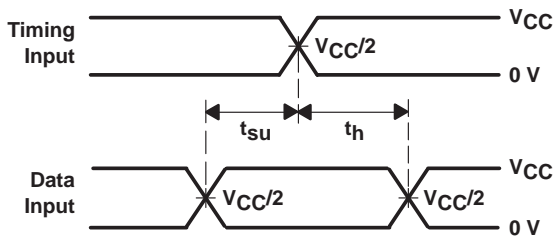
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION
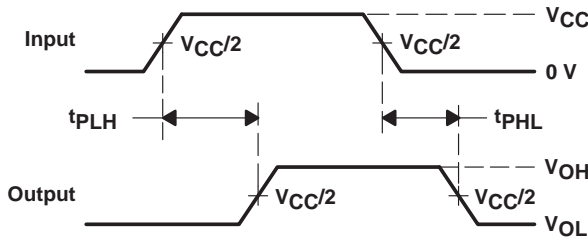
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
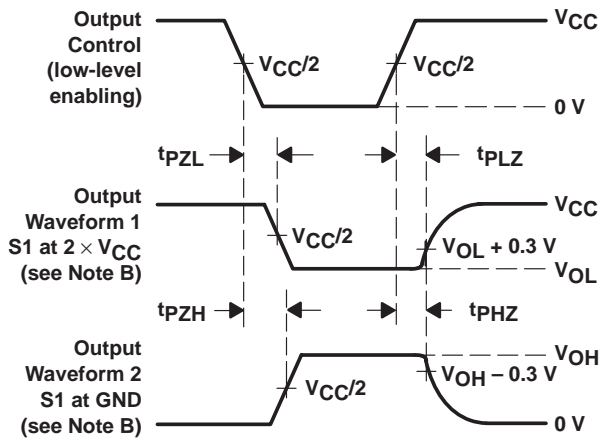
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
   D. The outputs are measured one at a time with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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