- **Low Supply Voltage Range 2.5 V – 5.5 V**
- **Low Operation Current, 400 µA at 1 MHz, 3 V**
- **Ultra-Low Power Consumption**
  Standby Mode: 2 µA
  RAM Retention Off Mode: 0.1 µA
- **Five Power-Saving Modes**
- **Wake Up From Standby Mode in 6 µs**
- **16-Bit RISC Architecture, 300 ns Instruction Cycle Time**
- **Single Common 32 kHz Crystal, Internal System Clock up to 3.8 MHz**
- **Integrated LCD Driver for up to 120 Segments**
- **Integrated Hardware Multiplier Performs Signed, Unsigned, and MAC Operations for Operands Up to 16 X 16 Bits**
- **Serial Communication Interface (USART), Select Asynchronous UART or Synchronous SPI by Software**
- **Slope A/D Converter Using External Components**
- **16-Bit Timer With Five Capture/Compare Registers**
- **Serial On-Board Programming**
- **Programmable Code Protection by Security Fuse**
- **Family Members Include:**
  MSP430C336 – 24 KB ROM, 1 KB RAM
  MSP430C337 – 32 KB ROM, 1 KB RAM
  MSP430P337A – 32 KB OTP, 1 KB RAM
- **EPROM Version Available for Prototyping: PMS430E337A**
- **Available in the following packages:**
  100 Pin Quad Flat-Pack (QFP),
  100 Pin Ceramic Quad Flat-Pack (CFP) (EPROM Version)

description

The Texas Instruments MSP430 is an ultra-low power mixed signal microcontroller family consisting of several devices which features different sets of modules targeted to various applications. The controller is designed to be battery operated for an extended application lifetime. With the 16-bit RISC architecture, 16 integrated registers on the CPU, and a constant generator, the MSP430 achieves maximum code efficiency. The digital-controlled oscillator, together with the frequency lock loop (FLL), provides a wake up from a low-power mode to an active mode in less than 6 µs. The MSP430x33x series micro-controllers have built in hardware multiplication and communication capability using asynchronous (UART) and synchronous protocols.

Typical applications of the MSP430 family include electronic gas, water, and electric meters and other sensor systems that capture analog signals, converts them to digital values, processes, displays, or transmits them to a host system.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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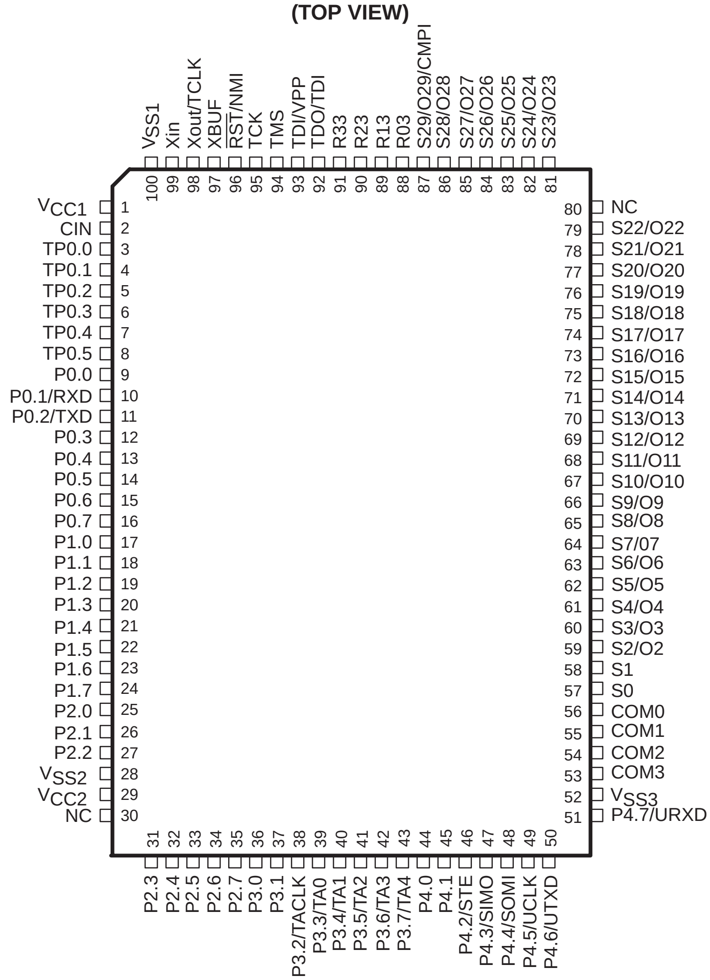
AVAILABLE OPTIONS

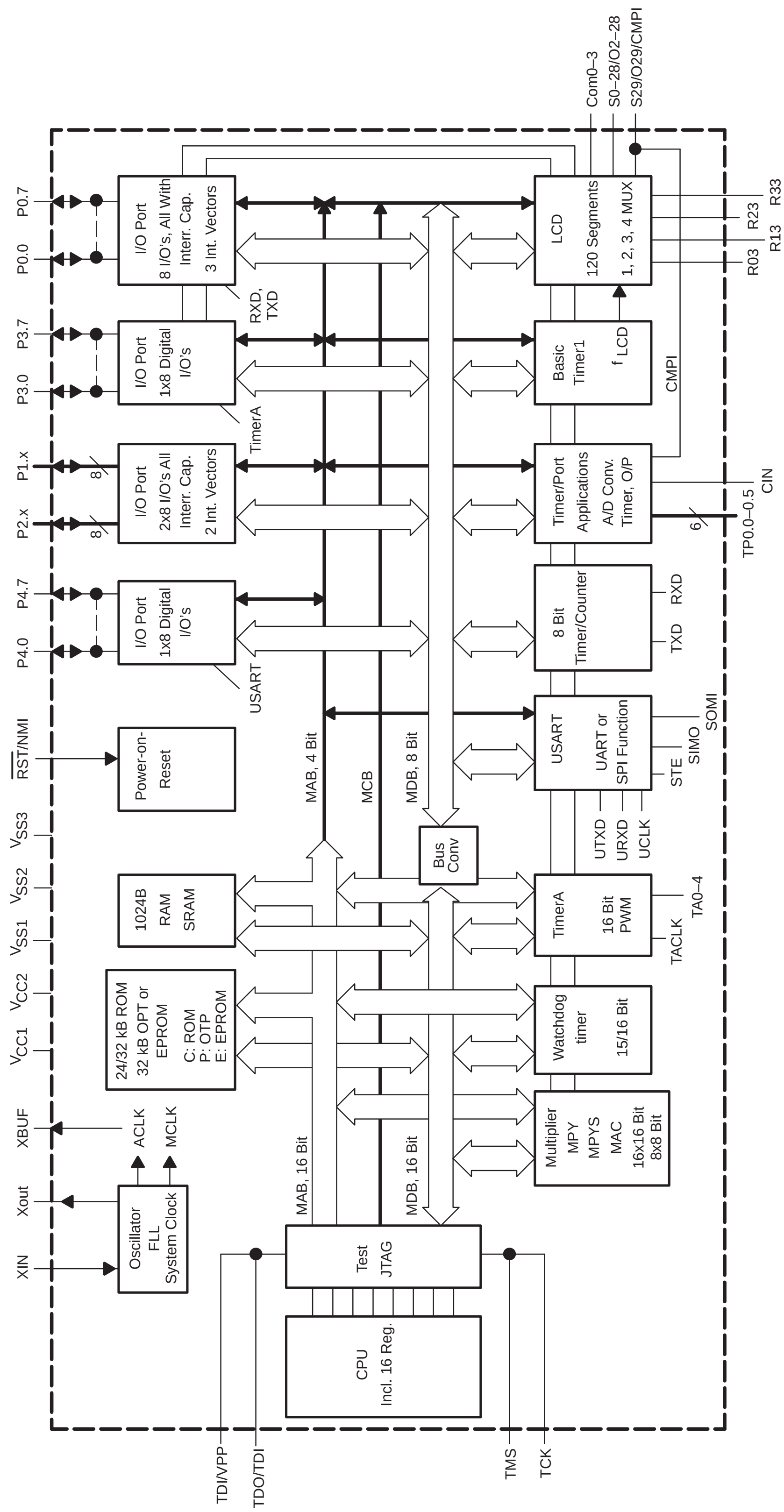
T_A	PACKAGED DEVICES	
	PLASTIC QFP (PJM)	CERAMIC QFP (HFD)
–40°C to 85°C	MSP430C336IPJM MSP430C337IPJM MSP430P337AIPJM	—
25°C	—	PMS430E337AHFD

PJM or HFD PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CIN	2	I	Input port. CIN is used as an enable for counter TPCNT1 – (Timer/Port).
COM0–3	56–53	O	Common outputs. COM0-3 are used for LCD backplanes – LCD
P0.0	9	I/O	General-purpose digital I/O
P0.1/RXD	10	I/O	General-purpose digital I/O, receive digital Input port – 8-bit Timer/Counter
P0.2/TXD	11	I/O	General-purpose digital I/O, transmit data output port – 8-bit Timer/Counter
P0.3–P0.7	12–16	I/O	Five general-purpose digital I/Os, bit 3-7
P1.0–P1.7	17–24	I/O	Eight general-purpose digital I/Os, bit 0-7
P2.0–P2.7	25–27, 31–35	I/O	Eight general-purpose digital I/Os, bit 0-7
P3.0, P3.1	36,37	I/O	Two general-purpose digital I/Os, bit 0 and bit 1
P3.2/TACLK	38	I/O	General-purpose digital I/O, clock input – Timer_A
P3.3/TA0	39	I/O	General-purpose digital I/O, capture I/O, or PWM output port – Timer_A CCR0
P3.4/TA1	40	I/O	General-purpose digital I/O, capture I/O, or PWM output port – Timer_A CCR1
P3.5/TA2	41	I/O	General-purpose digital I/O, capture I/O, or PWM output port – Timer_A CCR2
P3.6/TA3	42	I/O	General-purpose digital I/O, capture I/O, or PWM output port – Timer_A CCR3
P3.7/TA4	43	I/O	General-purpose digital I/O, capture I/O, or PWM output port – Timer_A CCR4
P4.0	44	I/O	General-purpose digital I/O, bit 0
P4.1	45	I/O	General-purpose digital I/O, bit 1
P4.2/STE	46	I/O	General-purpose digital I/O, slave transmit enable – USART/SPI mode
P4.3/SIMO	47	I/O	General-purpose digital I/O, slave in/master out – USART/SPI mode
P4.4/SOMI	48	I/O	General-purpose digital I/O, master in/slave out – USART/SPI mode
P4.5/UCLK	49	I/O	General-purpose digital I/O, external clock input – USART
P4.6/UTXD	50	I/O	General-purpose digital I/O, transmit data out – USART/UART mode
P4.7/URXD	51	I/O	General-purpose digital I/O, receive data in – USART/UART mode
R03	88	I	Input port of fourth positive (lowest) analog LCD level (V5) – LCD
R13	89	I	Input port of third most positive analog LCD level (V3 of V4) – LCD
R23	90	I	Input port of second most positive analog LCD level (V2) – LCD
R33	91	O	Output of most positive analog LCD level (V1) – LCD
$\overline{\text{RST}}$/NMI	96	I	Reset input or non-maskable interrupt input port
S0	57	O	Segment line S0 – LCD
S1	58	O	Segment line S1 – LCD
S2/O2–S5/O5	59–62	O	Segment lines S2 to S5 or digital output ports, O2-O5, group 1 – LCD
S6/O6–S9/O9	63–66	O	Segment lines S6 to S9 or digital output ports O6-O9, group 2 – LCD
S10/O10–S13/O13	67–70	O	Segment lines S10 to S13 or digital output ports O10-O13, group 3 – LCD
S14/O14–S17/O17	71–74	O	Segment lines S14 to S17 or digital output ports O14-O17, group 4 – LCD
S18/O18–S21/O21	75–78	O	Segment lines S18 to S21 or digital output ports O18-O21, group 5 – LCD
S22/O22–S25/O25	79, 81–83	O	Segment line S22 to S25 or digital output ports O22-O25, group 6 – LCD
S26/O26–S29/O29/CMPI	84–87	O	Segment line S26 to S29 or digital output ports O26-O29, group 7 – LCD. Segment line S29 can be used as comparator input port CMPI – Timer/Port
TCK	95	I	Test clock. TCK is the clock input port for device programming and test
TDI/VPP	93	I	Test data input. TDI/VPP is used as a data input port or input for programming voltage

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
TMS	94	I	Test mode select. TMS is used as an input port for device programming and test
TDO/TDI	92	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TP0.0	3	O	General-purpose 3-state digital output port, bit 0 – Timer/Port
TP0.1	4	O	General-purpose 3-state digital output port, bit 1 – Timer/Port
TP0.2	5	O	General-purpose 3-state digital output port, bit 2 – Timer/Port
TP0.3	6	O	General-purpose 3-state digital output port, bit 3 – Timer/Port
TP0.4	7	O	General-purpose 3-state digital output port, bit 4 – Timer/Port
TP0.5	8	I/O	General-purpose 3-state digital input/output port, bit 5 – Timer/Port
VCC1	1		Positive supply voltage
VCC2	29		Positive supply voltage
VSS1	100		Ground reference
VSS2	28		Ground reference
VSS3	52		Ground reference
XBUF	97	O	System clock (MCLK) or crystal clock (ACLK) output
Xin	99	I	Input port for crystal oscillator
Xout/TCLK	98	I/O	Output terminal of crystal oscillator or test clock input

short-form description

processing unit

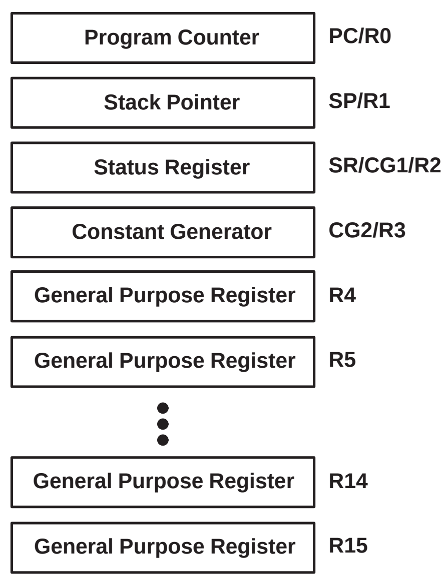
The processing unit is based on a consistent and orthogonal designed CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and is distinguished due to ease of programming. All operations, other than program-flow instructions consequently are performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

CPU registers

Sixteen registers are located inside the CPU, providing reduced instruction execution time. This reduces a register-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as a program counter, a stack pointer, a status register and a constant generator. The remaining registers are available as general purpose registers.

Peripherals are connected to the CPU using a data address and control bus and can be handled easily with all instructions for memory manipulation.



instruction set

The instruction set for this register-register architecture provides a powerful and easy-to-use assembly language. The instruction set consists of 51 instructions, with three formats and seven addressing modes. Table 1 provides a summation and example of the three types of instruction formats; the addressing modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 → R5
Single operands, destination only	e.g. CALL R8	PC → (TOS), R8→ PC
Relative jump, un–/conditional	e.g. JNE	Jump-on equal bit = 0

Instructions that can operate on both word and byte data are differentiated by the suffix .B when a byte operation is required.

Examples:	Instructions for word operation:		Instructions for byte operation:	
	MOV	EDE,TONI	MOV.B	EDE,TONI
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	——	

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	√	√	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	√	√	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	√	√	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	√	√	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	√		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	√		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2→ R10
Immediate	√		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

NOTE 1: S = source, D = destination.

Computed branches (BR) and subroutine calls (CALL) instructions use the same addressing modes as the other instructions. These addressing modes provide *indirect* addressing, ideally suited for computed branches and calls. The full use of this programming capability permits a program structure different from conventional 8- and 16-bit controllers. For example, numerous routines can easily be designed to deal with pointers and stacks instead of using flag type programs for flow control.

operation modes and interrupts

The MSP430 operating modes support various advanced requirements for ultra-low power and ultra-low energy consumption. This is achieved by the intelligent management of the operations during the different module operation modes and CPU states. The requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the RETI instruction to the mode that was selected before the interrupt event. The clocks used are ACLK and MCLK. ACLK is the crystal frequency and MCLK is a multiple of ACLK and is used as the system clock.

The following five operating modes are supported:

- Active mode (AM). The CPU is enabled with different combinations of active peripheral modules.
- Low power mode 0 (LPM0). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is active.
- Low power mode 1 (LPM1). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is inactive.
- Low power mode 2 (LMP2). The CPU is disabled, peripheral operation continues, ACLK signal is active, and MCLK and loop control for MCLK are inactive.
- Low power mode 3 (LMP3). The CPU is disabled, peripheral operation continues, ACLK signal is active, MCLK and loop control for MCLK are inactive, and the dc generator for the digital controlled oscillator (DCO) (→MCLK generator) is switched off.
- Low power mode 4 (LMP4). The CPU is disabled, peripheral operation continues, ACLK signal is inactive (crystal oscillator stopped), MCLK and loop control for MCLK are inactive, and the dc generator for the DCO is switched off.

The special function registers (SFR) include module-enable bits that stop or enable the operation of the specific peripheral module. All registers of the peripherals may be accessed if the operational function is stopped or enabled. However, some peripheral current-saving functions are accessed through the state of local register bits. An example is the enable/disable of the analog voltage generator in the LCD peripheral, which is turned on or off using one register bit.

The most general bits that influence current consumption and support fast turn-on from low power operating modes are located in the status register (SR). Four of these bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.

15 9	8	7							0
Reserved For Future Enhancements	V	SCG1	SCG0	OscOff	CPUOff	GIE	N	Z	C

rw-0

interrupts

Software determines the activation of interrupts through the monitoring of hardware set interrupt flag status bits, the control of specific interrupt enable bits in SRs, the establishment of interrupt vectors, and the programming of interrupt handlers. The interrupt vectors and the power-up starting address are located in ROM address locations 0FFFFh through 0FFE0h. Each vector contains the 16-bit address of the appropriate interrupt handler instruction sequence. Table 3 provides a summation of interrupt functions and addresses.

Table 3. Interrupt Functions and Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up, external reset, Watchdog	WDTIFG	Reset	0FFFEh	15, highest
NMI, Oscillator fault	NMIIFG (see Notes 2 and 4) OFIFG (see Notes 2 and 5)	Non-maskable (Non)-maskable	0FFFCh	14
Dedicated I/O P0.0	P0IFG.0	Mmaskable	0FFFAh	13
Dedicated I/O P0.1 or 8-bit Timer/Counter	P0IFG.1	Maskable	0FFF8h	12
		Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
Timer_A	CCIFG0 (see Note 3)	Maskable	0FFF2h	9
Timer_A	TAIFG (see Note 3)	Maskable	0FFF0h	8
UART receive	URXIFG	Maskable	0FFEEh	7
UART transmit	UTXIFG	Maskable	0FFECh	6
			0FFEAh	5
Timer/Port	RC1FG, RC2FG, EN1FG (see Note 3)	Maskable	0FFE8h	4
I/O port P2	P2IFG.07 (see Note 2)	Maskable	0FFE6h	3
I/O port P1	P1IFG.07 (see Note 2)	Maskable	0FFE4h	2
Basic Timer1	BTIFG	Maskable	0FFE2h	1
I/O port P0.2 – P0.7	P0IFG.27 (see Note 2)	Maskable	0FFE0h	0, lowest

NOTES: 2. Multiple source flags
3. Interrupt flags are located in the individual module registers.
4. Non-maskable : neither the individual or the general interrupt enable bit will disable an interrupt event.
5. (Non)-maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address 0h	7	6	5	4	3	2	1	0
					P0IE.1	P0IE.0	OFIE	WDTIE
					rw-0	rw-0	rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable signal
OFIE: Oscillator fault interrupt enable signal
P0IE.0: Dedicated I/O P0.0 interrupt enable signal
P0IE.1: P0.1 or 8-bit Timer/Counter, RXD interrupt enable signal

Address 01h	7	6	5	4	3	2	1	0
	BTIE				TPIE		UTXIE	URXIE
	rw-0				rw-0		rw-0	rw-0

URXIE: USART receive interrupt enable signal
UTXIE: USART transmit interrupt enable signal
TPIE: Timer/Port interrupt enable signal
BTIE: Basic Timer1 interrupt enable signal

interrupt flag registers 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	P0IFG.1	P0IFG.0	OFIFG	WDTIFG
				rw-0	rw-0	rw-0	rw-1	rw-0

WDTIFG: Set on overflow or security key violation
or
Reset on VCC1 power-on or reset condition at $\overline{\text{RST}}$/NMI-pin
OFIFG: Flag set on oscillator fault
P0IFG.0: Dedicated I/O P0.0
P0IFG.1: P0.1 or 8-bit Timer/Counter, RXD
NMIIFG: Signal at $\overline{\text{RST}}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG						UTXIFG	URXIFG
	rw						rw-1	rw-0

URXIFG: USART receive flag
UTXIFG: USART transmit flag
BTIFG: Basic Timer1 flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h								

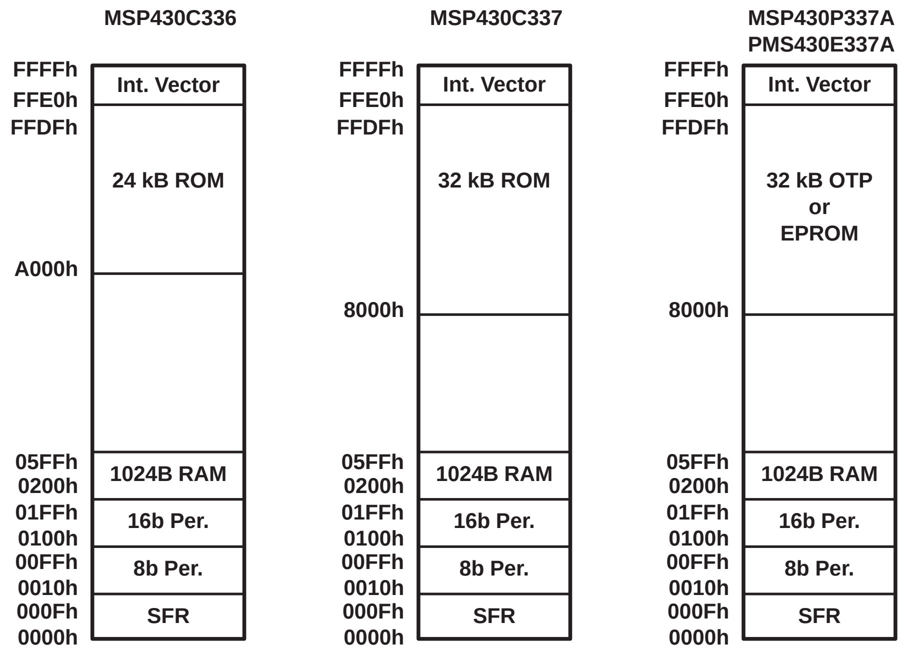
Address	7	6	5	4	3	2	1	0
05h							UTXE	URXE
							rw-0	rw-0

UTXE: USART transmit enable
URXE: USART receive enable

Legend

rw:	Bit can be read and written
rw-0:	Bit can be read and written. It is reset by PUC
(shaded box)	SFR bit not present in device

ROM memory organization



peripherals

Peripherals are connected to the CPU through a data, address, and controls bus and can be handled easily with instructions for memory manipulation.

oscillator and system clock

Two clocks are used in the system: the system (master) clock (MCLK) and the auxiliary clock (ACLK). The MCLK is a multiple of the ACLK. The ACLK runs with the crystal oscillator frequency. The special design of the oscillator supports the feature of low current consumption and the use of a 32 768 Hz crystal. The crystal is connected across two terminals without any other external components being required.

The oscillator starts after applying VCC, due to a reset of the control bit (OscOff) in the status register (SR). It can be stopped by setting the OscOff bit to a 1. The enabled clock signals ACLK, ACLK/2, ACLK/4, or MCLK are accessible for use by external devices at output terminal XBUF .

The controller system clocks have to deal with different requirements according to the application and system condition. Requirements include:

- High frequency in order to react quickly to system hardware requests or events
- Low frequency in order to minimize current consumption, EMI, etc.
- Stable frequency for timer applications e.g. real time clock (RTC)
- Enable start-stop operation with minimum delay to operation function

oscillator and system clock (continued)

These requirements cannot all be met with fast frequency high-Q crystals or with RC-type low-Q oscillators. The compromise selected for the MSP430 uses a low-crystal frequency which is multiplied to achieve the desired nominal operating range:

$$f_{(system)} = (N + 1) \times f_{(crystal)}$$

The crystal frequency multiplication is acheived with a frequency locked loop (FLL) technique. The factor N is set to 31 after a power-up clear condition. The FLL technique, in combination with a digital controlled oscillator (DCO), provides immediate start-up capability together with long term crystal stability. The frequency variation of the DCO with the FLL inactive is typically 330 ppm, which means that with a cycle time of 1 µs the maximum possible variation is 0.33 ns. For more precise timing, the FLL can be used, which forces longer cycle times if the previous cycle time was shorter than the selected one. This switching of cycle times makes it possible to meet the chosen system frequency over a long period of time.

The start-up operation of the system clock depends on the previous machine state. During a PUC, the DCO is reset to its lowest possible frequency. The control logic starts operation immediately after recognition of PUC.

multiplication

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

digital I/O

Five eight-bit I/O ports (P0 thru P4) are implemented. Port P0 has six control registers, P1 and P2 have seven control registers, and P3 and P4 modules have four control registers to give maximum flexibility of digital input/output to the application:

- Individual I/O bits are independently programable.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of the P0, P1, and P2 ports.
- Read/write access is available to all registers by all instructions.

The seven registers are:

- Input register — contains information at the pins
- Output register — contains output information
- Direction register — controls direction
- Interrupt edge select — contains input signal change necessary for interrupt
- Interrupt flags — indicates if interrupt(s) are pending
- Interrupt enable — contains interrupt enable pins
- Function select — determines if pin(s) used by module or port

These registers contain eight bits each with the exception of the interrupt flag register and the interrupt enable register which are 6 bits each. The two least significant bit (LSBs) of the interrupt flag and enable registers are located in the special function register (SFR). Five interrupt vectors are implemented, one for Port P0.0, one for Port P0.1, one commonly used for any interrupt event on Port P0.2 to Port P0.7, one commonly used for any interrupt event on Port P1.0 to Port P1.7, and one commonly used for any interrupt event on Port P2.0 to Port P2.7.

LCD drive

Liquid crystal displays (LCDs) for static, 2-, 3-, and 4-MUX operation can be driven directly. The operation of the controller LCD logic is defined by software through memory-bit manipulation. LCD memory is part of the LCD module, not part of data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily obtained using table programming techniques combined with the proper addressing mode. The segment information is stored into LCD memory using instructions for memory manipulation.

The drive capability is defined by the external resistor divider that supports analog levels for 2-, 3-, and 4-MUX operation. Groups of the LCD segment lines can be selected for digital output signals. The MSP430x33x configuration has four common lines, 30 segment lines, and four terminals for adjusting the analog levels.

Basic Timer1

The Basic Timer1 (BT1) divides the frequency of MCLK or ACLK, as selected with the SSEL bit, to provide low frequency control signals. This is done within the system by one central divider, the Basic Timer1, to support low current applications. The BTCTL control register contains the flags which control or select the different operational functions. When the supply voltage is applied or when a reset of the device ($\overline{RST}$/NMI pin), a watchdog overflow, or a watchdog security key violation occurs, all bits in the register hold undefined or unchanged status. The user software usually configures the operational conditions on the BT during initialization.

The Basic Timer1 has two eight bit timers which can be cascaded to a sixteen bit timer. Both timers can be read and written by software. Two bits in the SFR address range handle the system control interaction according to the function implemented in the Basic Timer1. These two bits are the Basic Timer1 interrupt flag (BTIFG) and the Basic Timer1 interrupt enable (BTIE) bit.

Watchdog Timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The Watchdog Timer counter (WDTCNT) is a 15/16-bit upcounter which is not directly accessible by software. The WDTCNT is controlled using the Watchdog Timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL, in both operating modes (watchdog or timer) is only possible by using the correct password in the high-byte. The low-byte stores data written to the WDTCTL. The high-byte password is 05Ah. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. When the password is read its value is 069h. This minimizes accidental write operations to the WDTCTL register. In addition to the Watchdog Timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

USART

The universal synchronous/asynchronous interface is a dedicated peripheral module which provides serial communications. The USART supports synchronous SPI (3 or 4 pin), and asynchronous UART communications protocols, using double buffered transmit and receive channels. Data streams of 7 or 8 bits in length can be transferred at a rate determined by the program, or by a rate defined by an external clock. Low power applications are optimized by UART mode options which allow for the receipt of only the first byte of a complete frame. The applications software then decides if the succeeding data is to be processed. This option reduces power consumption.

Two dedicated interrupt vectors are assigned to the USART module, one for the receive and one for the transmit channel.

Timer/Port

The Timer/Port module has two 8-bit counters, an input that triggers one counter and six digital outputs with 3-state capability. Both counters have an independent clock selector for selecting an external signal or one of the internal clocks (ACLK or MCLK). One of the counters has an extended control capability to halt, count continuously, or gate the counter by selecting one of two external signals. This gate signal sets the interrupt flag if an external signal is selected and the gate stops the counter.

Both timers can be read to and written from by software. The two 8-bit counters can be cascaded to form a 16-bit counter. A common interrupt vector is implemented. The interrupt flag can be set by three events in the 8-bit counter mode (gate signal or overflow from the counters) or by two events in the 16-bit counter mode (gate signal or overflow from the MSB of the cascaded counter).

slope A/D conversion

Slope A/D conversion is accomplished with the Timer/Port module using external resistor(s) for reference (R_{ref}), external resistor(s) to the measured (R_{meas}), and an external capacitor. The external components are driven by software in such a way that the internal counter measures the time that is needed to charge or discharge the capacitor.The reference resistor’s (R_{ref}) charge or discharge time is represented by N_{ref} counts. The unknown resistors (R_{meas}) charge or discharge time is represented by N_{meas} counts. The unknown resistor’s value R_{meas} is the value of R_{ref} multiplied by the relative number of counts (N_{meas}/N_{ref}). This value determines resistive sensor values that correspond to the physical data, for example temperature, when an NTC or PTC resistor is used.

Timer_A

The Timer_A module offers one sixteen bit counter and five capture/compare registers. The timer clock source can be selected to come from an external source TACLK (SSEL=0), the ACLK (SSEL=1), or MCLK (SSEL=2 or SSEL=3). The clock source can be divided by one, two, four or eight. The timer can be fully controlled (in word mode) since it can be halted, read, and written. It can be stopped, run continuously, count up, or count up/down using one compare block to determine the period. The five capture/compare blocks are configured by the application software to run in either capture or compare mode.

The capture mode is primarily used to measure external or internal events with any combination of positive, negative, or both edges of the clock. The clock can also be stopped in capture mode by software. One external event (CCISx=0) per capture block can be selected. If CCISx=1, the ACLK is the capture signal; and if CCISx=2 or CCISx=3, software capture is chosen.

The compare mode is primarily used to generate timing for the software or application hardware or to generate pulse-width modulated output signals for various purposes like D/A conversion functions or motor control. An individual output module, which can run independently of the compare function or is triggered in several ways, is assigned to each of the five capture/compare registers.

Two interrupt vectors are used by the Timer_A module. One individual vector is assigned to capture/compare block CCR0 and one common interrupt vector is assigned to the timer and the other four capture/compare blocks. The five interrupt events using the common vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter to continue the interrupt handler software at the correct location. This simplifies the interrupt handler and gives each interrupt event the same interrupt handler overhead of 5 cycles.

8-bit Timer/Counter

The 8-bit interval timer supports three major functions for applications:

- Serial communication or data exchange
- Plus counting or plus accumulation
- Timer

8-bit Timer/Counter (continued)

The 8-bit Timer/Counter peripheral includes the following major blocks: an 8-bit up-counter with preload register, an 8-bit control register, an input clock selector, an edge detection (e.g. start bit detection for asynchronous protocols), and an input and output data latch, triggered by the carry-out-signal from the 8-bit counter.

The 8-bit counter counts up with an input clock, which is selected by two control bits from the control register. The four possible clock sources are MCLK, ACLK, the external signal from terminal P0.1, and the signal from the logical AND of MCLK and terminal P0.1.

Two counter inputs (load, enable) control the counter operation. The load input controls load operations. A write-access to the counter results in loading the content of the preload register into the counter. The software writes or reads the preload register with all instructions. The preload register acts as a buffer and can be written immediately after the load of the counter is completed. The enable input enables the count operation. When the enable signal is set to high, the counter will count-up each time a positive clock edge is applied to the clock input of the counter.

peripheral file map

PERIPHERALS WITH BYTE ACCESS		
UART	Transmit buffer, UTXBUF	077h
	Receive buffer, URXBUF	076h
	Baud rate, UBR1	075h
	Baud rate, UBR0	074h
	Modulation control, UMCTL	073h
	Receive control, URCTL	072h
	Transmit control, UTCTL	071h
	UART control, UCTL	070h
EPROM	EPROM control, EPCTL	054h
Crystal Buffer	Crystal buffer control, CBCTL	053h
System Clock	SCG frequency control, SCFQCTL	052h
	SCG frequency integrator, SCFI1	051h
	SCG frequency integrator, SCFI0	050h
Timer/Port	Timer/Port enable, TPE	04Fh
	Timer/Port data, TPD	04Eh
	Timer/Port counter2, TPCNT2	04Dh
	Timer/Port counter1, TPCNT1	04Ch
	Timer/Port control, TPCTL	04Bh
Basic Timer1	Basic timer counter2, BTCNT2	047h
	Basic timer counter1, BTCNT1	046h
	Basic timer control, BTCTL	040h
8-bit T/C	8-bit Timer/Counter data, TCDAT	044h
	8-bit Timer/Counter preload, TCPLD	043h
	8-bit Timer/Counter control, TCCTL	042h
LCD	LCD memory 15, LCDM15	03Fh
	:	
	LCD memory 1, LCDM1	031h
	LCD control & mode, LCDCTL	030h
Port P2	Port P2 selection, P2SEL	02Eh
	Port P2 interrupt enable, P2IE	02Dh
	Port P2 interrupt edge Select, P2IES	02Ch
	Port P2 interrupt flag, P2IFG	02Bh
	Port P2 direction, P2DIR	02Ah
	Port P2 output, P2OUT	029h
	Port P2 input, P2IN	028h
Port P1	Port P1 selection, P1SEL	026h
	Port P1 interrupt enable, P1IE	025h
	Port P1 interrupt edge Select, P1IES	024h
	Port P1 interrupt flag, P1IFG	023h
	Port P1 direction, P1DIR	022h
	Port P1 output, P1OUT	021h
	Port P1 input, P1IN	020h
Port P4	Port P4 selection, P4SEL	01Fh
	Port P4 direction, P4DIR	01Eh
	Port P4 output, P4OUT	01D
	Port P4 input, P4IN	01Ch

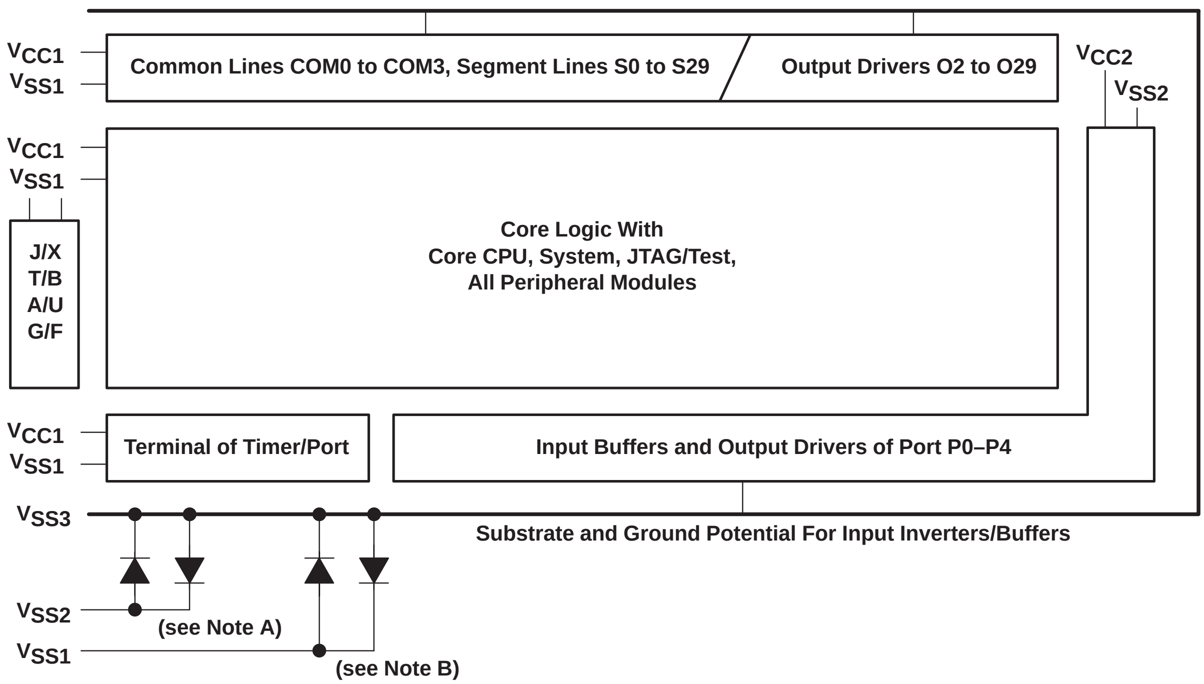
Port P3	Port P3 selection, P3SEL	01Bh
	Port P3 direction, P3DIR	01Ah
	Port P3 output, P3OUT	019h
	Port P3 input, P3IN	018h
Port P0	Port P0 interrupt enable, P0IE	015h
	Port P0 interrupt edge select, P0IES	014h
	Port P0 interrupt flag, P0IFG	013h
	Port P0 direction, P0DIR	012h
	Port P0 output, P0OUT	011h
	Port P0 input, P0IN	010h
Special	SFR interrupt flag2, IFG2	003h
Function	SFR interrupt flag1, IFG1	002h
	SFR interrupt enable2, IE2	001h
	SFR interrupt enable1, IE1	000h
PERIPHERALS WITH WORD ACCESS		
Multiply	Sum extend, SumExt	013Eh
	Result high word, ResHi	013Ch
	Result low word, ResLo	013Ah
	Second operand, OP2	0138h
	Reserved	0136h
	Multiply+accumulate/operand1, MAC	0134h
	Multiply signed/operand1, MPYS	0132h
	Multiply unsigned/operand1, MPY	0130h
Watchdog	Watchdog Timer control, WDTCTL	0120h
Timer_A	Timer_A interrupt vector, TAIV	012Eh
	Timer_A control, TACTL	0160h
	Cap/Com control, CCTL0	0162h
	Cap/Com control, CCTL1	0164h
	Cap/Com control, CCTL2	0166h
	Cap/Com control, CCTL3	0168h
	Cap/Com control, CCTL4	016Ah
	Reserved	016Ch
	Reserved	016Eh
	Timer_A register, TAR	0170h
	Cap/Com register, CCR0	0172h
	Cap/Com register, CCR1	0174h
	Cap/Com register, CCR2	0176h
	Cap/Com register, CCR3	0178h
	Cap/Com register, CCR4	017Ah
	Reserved	017Ch
	Reserved	017Eh

absolute maximum ratings†

Supply voltage range, between V_{CC} terminals	–0.3 V to 0.3 V
Supply voltage range, between V_{SS} terminals	–0.3 V to 0.3 V
Input voltage range, V_{CC1} to any VSS terminal	–0.3 V to 6 V
Input voltage range, V_{CC2} to any VSS terminal	–0.3 V to 6 V
Input voltage range to any terminal (referenced to VSS)	–0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal	±2 mA
Storage temperature range, T_{stg}, (unprogrammed device)	–55°C to 150°C
Storage temperature range, T_{stg}, (programmed device)	–40°C to 85°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to VSS.



NOTES: A. Ground potential for all port output drivers and input terminals, excluding first inverter/buffer

B. Ground potential for entire device core logic and peripheral modules

Figure 1. Supply Voltage Interconnection

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}, (MSP430C33x)		2.5		5.5	V
Supply voltage, V_{CC}, (MSP430E/P33xA)		2.5		5.5	V
Supply voltage, VSS			0		V
Operating free-air temperature range T_A	MSP430C33x, MSP430P33xA	–40		85	°C
	PMS430E33xA		25		
XTAL frequency $f_{(XTAL)}$ (signal ACLK)			32768		HZ
Processor frequency (signal MCLK), f_{system}	V_{CC} = 3 V	DC		1.65	MHz
	V_{CC} = 5 V	DC		3.8	MHz
Low-level input voltage, V_{IL}† (excluding Xin, Xout)	V_{CC} = 3 V/5 V	V_{SS}		V_{SS}+0.8	V
High-level input voltage, V_{IH}† (excluding Xin, Xout)		0.7×V_{CC}		V_{CC}	
Low-level input voltage, $V_{IL(Xin, Xout)}$		V_{SS}		0.2×VCC1	V
High-level input voltage, $V_{IH(Xin, Xout)}$		0.8×V_{CC1}		V_{CC1}	

† A serial resistor of 1 kΩ to the $\overline{RST}$/NMI pin is recommended to enhance latch–up immunity.

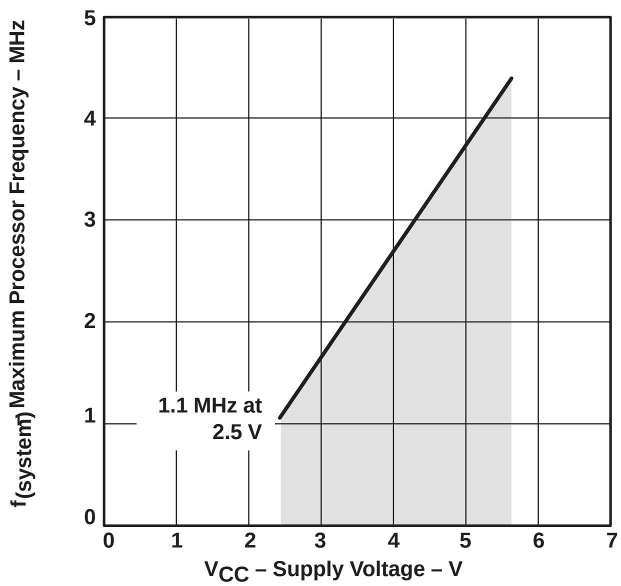


Figure 2. Processor Frequency vs Supply Voltage

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

supply current (into V_{CC}) excluding external current ($f_{(system)}$ = 1 MHz) (see Note 6)

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode	C336/7	T_A= –40°C +85°C,	V_{CC} = 3 V		400	500	μA
			T_A= –40°C +85°C,	V_{CC} = 5 V		800	900	
		P337A	T_A= –40°C +85°C,	V_{CC} = 3 V		570	700	
			T_A= –40°C +85°C,	V_{CC} = 5 V		1170	1250	
$I_{(CPUOff)}$	Low power mode, (LPM0,1)	C336/7	T_A= –40°C +85°C,	V_{CC} = 3 V		50	70	μA
			T_A= –40°C +85°C,	V_{CC} = 5 V		100	130	
		P337A	T_A= –40°C +85°C,	V_{CC} = 3 V		50	70	
			T_A= –40°C +85°C,	V_{CC} = 5 V		100	130	
$I_{(LPM2)}$	Low power mode, (LPM2)		T_A= –40°C +85°C,	V_{CC} = 3 V		7	12	μA
			T_A= –40°C +85°C,	V_{CC} = 5 V		18	25	
$I_{(LPM3)}$	Low power mode, (LPM3)		T_A= –40°C	V_{CC} = 3 V		2.0	3.5	μA
			T_A= 25°C			2.0	3.5	
			T_A= 85°C			1.6	3.5	
			T_A= –40°C	V_{CC} = 5 V		5.2	10	
			T_A= 25°C			4.2	10	
			T_A= 85°C			4.0	10	
$I_{(LPM4)}$	Low power mode, (LPM4)		T_A= –40°C	V_{CC} = 3 V/5 V		0.1	0.8	μA
			T_A= 25°C			0.1	0.8	
			T_A= 85°C			0.4	1.5	

NOTE 6: All inputs are tied to 0 V or VCC2. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with active Basic Timer1 Module (ACLK selected), LCD Module (f_{LCD}=1024Hz, 4MUX) and USART module (UART, ACLK, 2400 Baud selected)

Current Consumption of active mode versus system frequency,

$$I_{AM} = I_{AM[1MHz]} \times f_{system}[MHz]$$

Current Consumption of active mode versus supply voltage,

$$I_{AM} = I_{AM[3V]} + 200\mu A/V \times (V_{CC}-3)$$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

schmitt-trigger inputs Port 0 to P4: P0.x to P4.x, Timer/Port: CIN, TP0.5

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3 V	1.2		2.1	V
		V_{CC} = 5 V	2.3		3.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3 V	0.7		1.5	
		V_{CC} = 5 V	1.4		2.3	
V_{hys}	Input hysteresis (V_{IT+}–V_{IT-})	V_{CC} = 3 V	0.3		1.0	
		V_{CC} = 5 V	0.6		1.4	

outputs Port 0 to P4: P0.x to P4.x, Timer/Port: TP0.0 to TP0.5, LCD: S2/O2 to S29/O29, XBUF: XBUF, JTAG:TDO

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1.2 mA, See Note 7	V_{CC} = 3 V	V_{CC}–0.4		V_{CC}	V
		I_{OH} = – 3.5 mA, See Note 8		V_{CC}–1.0		V_{CC}	
		I_{OH} = – 1.5 mA, See Note 7	V_{CC} = 5 V	V_{CC}–0.4		V_{CC}	
		I_{OH} = – 4.5 mA, See Note 8		V_{CC}–1.0		V_{CC}	
V_{OL}	Low-level output voltage	I_{OL} = + 1.2 mA, See Note 7	V_{CC} = 3 V	V_{SS}		V_{SS}+0.4	V
		I_{OL} = + 3.5 mA, See Note 8		V_{SS}		V_{SS}+1.0	
		I_{OL} = + 1.5 mA, See Note 7	V_{CC} = 5 V	V_{SS}		V_{SS}+0.4	
		I_{OL} = + 4.5 mA, See Note 8		V_{SS}		V_{SS}+1.0	

NOTES: 7. The maximum total current for all outputs combined should not exceed ±9.6 mA to hold the maximum voltage drop specified.
8. The maximum total current for all outputs combined should not exceed ±28 mA to hold the maximum voltage drop specified.

leakage current (see Note 9)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(TP)}$	High-impendance leakage current, Timer/Port	Timer/Port:$V_{TP0.x}$, V_{CC} = 3 V/5 V,	CIN = V_{SS}, V_{CC}, (see Note 10)			± 50	nA
$I_{lkg(S27)}$	High-impendance leakage current, S27	V_{S27} = V_{SS} to V_{CC},	V_{CC} = 3 V/5 V			± 50	nA
$I_{lkg(P0x)}$	Leakage current, port 0	Port P0: P0.x, $0 \le x \le 7$, (see Note 11)	V_{CC} = 3 V/5 V,			± 50	nA

NOTES: 9. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins(s) – unless otherwise noted.
10. All Timer/Port pins (TP0.0 to TP0.5) are Hi-Z. Pins CIN and TP0.0 to TP0.5 are connected together during leakage current measurement. In the leakage measurement mode, the input CIN is included. The input voltage is V_{SS} or V_{CC}.
11. The leakages of the digital port terminals are measured individually. The port terminal must be selected for input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

optional resistors (see Note 12)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$R_{(opt1)}$	Resistors, individually programmable with ROM code, all port pins, values applicable for pull-down and pull-up	V_{CC} = 3 V/5 V	1.4	4.1	6.8	kΩ
$R_{(opt2)}$		V_{CC} = 3 V/5 V	2.1	6.2	11	kΩ
$R_{(opt3)}$		V_{CC} = 3 V/5 V	4.2	12	20	kΩ
$R_{(opt4)}$		V_{CC} = 3 V/5 V	6.6	19	32	kΩ
$R_{(opt5)}$		V_{CC} = 3 V/5 V	12	37	62	kΩ
$R_{(opt6)}$		V_{CC} = 3 V/5 V	26	75	124	kΩ
$R_{(opt7)}$		V_{CC} = 3 V/5 V	39	112	185	kΩ
$R_{(opt8)}$		V_{CC} = 3 V/5 V	65	187	309	kΩ
$R_{(opt9)}$		V_{CC} = 3 V/5 V	91	261	431	kΩ
$R_{(opt10)}$		V_{CC} = 3 V/5 V	117	337	557	kΩ

NOTE 12: Optional resistors $R_{(optx)}$ for pulldown or pullup are not programmed in standard OTP/EPROM devices P/E 337.

inputs and outputs

	PARAMETER	CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$t_{(int)}$	External Interrupt timing	Port P0, P1 to P2: External trigger signal for the interrupt flag (see Notes 13 and 14)	3 V/5 V	1.5			cycle
$t_{(cap)}$	Timer_A, Capture timing	TA0-TA4 External capture signal (see Note 15)	3 V/5 V	250			ns
$f_{(IN)}$	Input frequency	P0.1, CIN, TP 0.5, UCLK, SIMO, SOMI, TACLK, TA0-TA4	3 V/5 V	DC		$f_{(system)}$	MHz
$t_{(H)}$ or $t_{(L)}$			3 V	300		$f_{(system)}$	ns
$t_{(H)}$ or $t_{(L)}$			5 V	300		$f_{(system)}$	
$f_{(XBUF)}$	Output frequency	XBUF, C_L = 20 pF	3 V/5 V			$f_{(system)}$	MHz
$f_{(TAx)}$		TA0-4, C_L = 20 pF	3 V/5 V	DC		$f_{(system)}/2$	
$f_{(UCLK)}$		UCLK, C_L = 20 pF	3 V/5 V	DC		$f_{(system)}$	
$t_{(Xdc)}$	Duty cycle of output	XBUF, C_L = 20 pF $f_{(MCLK)}$= 1.1 MHz $f_{(XBUF)} = f_{(ACLK)}$ $f_{(XBUF)} = f_{(ACLK/n)}$	 3 V/5 V 3 V/5 V 3 V/5 V	 40% 35% 	 50	 60% 65% 	
$\Delta t_{(TA)}$		TA0..4, C_L = 20 pF $t_{(TAH)} = t_{(TAL)}$	3 V/5 V		0	±100	ns
$\Delta t_{(UC)}$		UCLK, $C_{(L)}$ = 15pF $t_{(UCH)} = t_{(UCL)}$	3 V/5 V		0	±100	ns
$t_{(\tau)}$	USART: Deglitch time	See Note16	3 V 5 V	0.6 0.3		2.6 1.4	µs µs

NOTES: 13. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently from this timing constraint. $T_{(int)}$ is defined in MCLK cycles.
14. The external interrupt signal cannot exceed the maximum input frequency ($f_{(in)}$)
15. The external capture signal triggers the capture event every time $t_{(cap)}$ is met. It may be triggered even with capture signals shorter than $t_{(cap)}$. The conditions to set the flag must be met independently from this timing constraint.
16. The signal applied to the USART receive signal/terminal (URXD) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD line.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

LCD

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at R33	V_{CC} = 3 V/5 V	2.5		V_{CC}+0.2	V
$V_{(23)}$		Voltage at R23			$(V_{33}–V_{03}) \times 2/3 + V_{03}$		
$V_{(13)}$		Voltage at R13			$(V_{(33)}–V_{(03)}) \times 1/3 + V_{(03)}$		
$V_{(03)}$		Voltage at R03		$V_{(33)}$ – 2.5		V_{CC}+0.2	
$V_{O(HLCD)}$	Output 1	$I_{(HLCD)}$<= 10 nA	V_{CC} = 3 V/5 V	$V_{(R33)}$ – 0.125		V_{CC}	V
$V_{O(LLCD)}$	Output 0	$I_{(LLCD)}$ <= 10 nA		V_{SS}		V_{SS} + 0.125	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V/5 V			±20	nA
$I_{(R13)}$		R13 = V_{CC}/3				±20	
$I_{(R23)}$		R23 = 2 × V_{CC}/3				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$= – 3 µA,	V_{CC} = 3 V/5 V	$V_{(03)}$		$V_{(03)}$ – 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ – 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ – 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

PUC/POR

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(POR)}$ delay	POR		V_{CC} = 3 V/5 V		150	250	µs
$V_{(POR)}$		T_A = –40°C		1.5		2.4	V
		T_A = 25°C		1.2		2.1	V
		T_A = 85°C		0.9		1.8	V
$V_{(min)}$				0		0.4	V
$t_{(reset)}$	PUC/POR	Reset is accepted internally		2			µs

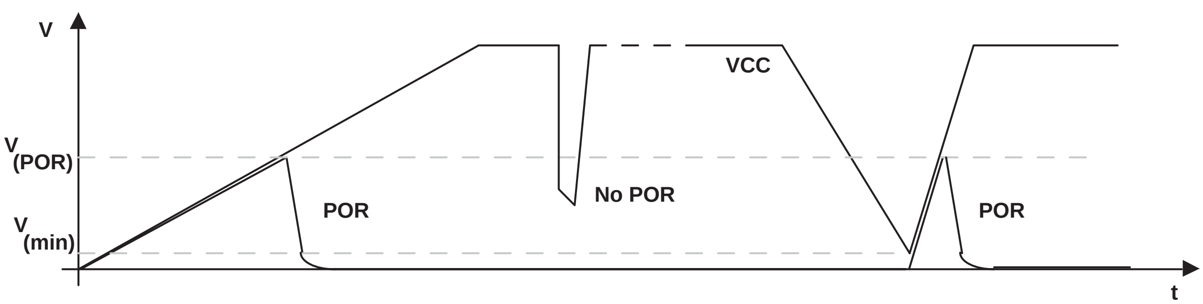


Figure 3. Power-On Reset (POR) vs Supply Voltage

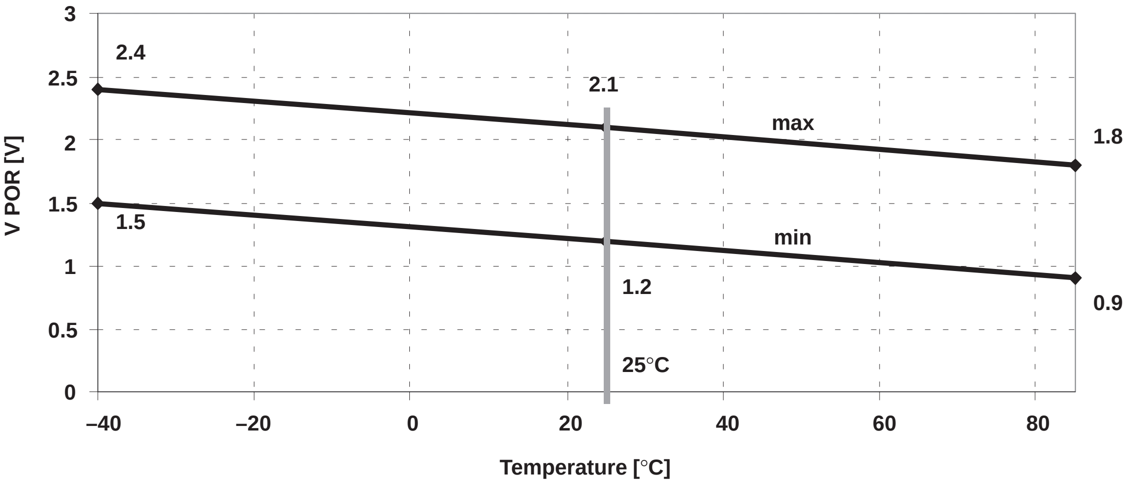


Figure 4. $V_{(POR)}$ vs Temperature

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

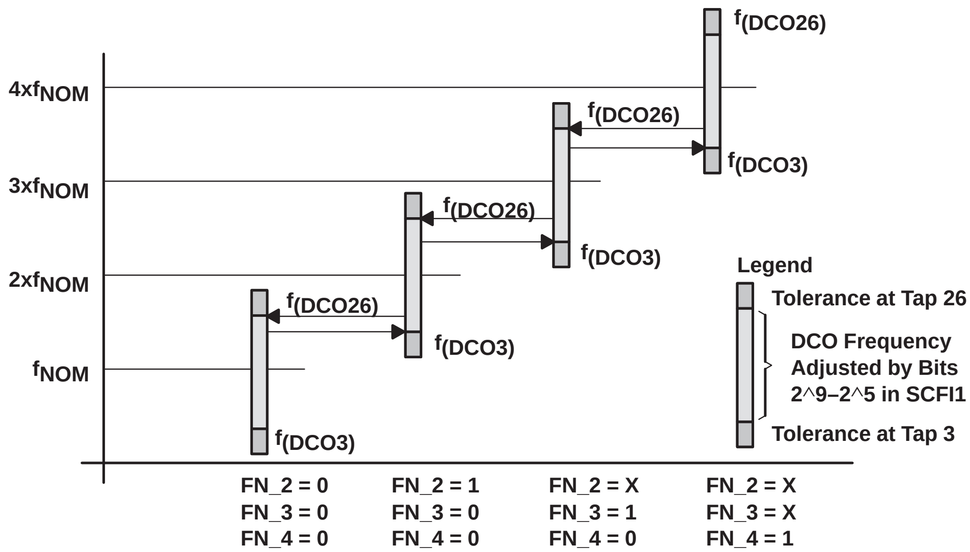
crystal oscillator: Xin, Xout

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$C_{(Xin)}$	Integrated capacitance at input	V_{CC} = 3V/5V		12		pF
$C_{(Xout)}$	Integrated capacitance at output			12		pF

DCO

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(NOM)}$	DCO	$N_{(DCO)}$ = 1 A0h FN_4=FN_3=FN_2 = 0	V_{CC} = 3 V/5 V		1		MHz
$f_{(NOM)}$	$f_{(DCO3)}$	$N_{(DCO)}$ = 00 0110 0000 FN_4=FN_3=FN_2 = 0	V_{CC} = 3 V	0.15		0.6	MHz
			V_{CC} = 5 V	0.18		0.62	
	$f_{(DCO26)}$	$N_{(DCO)}$ = 11 0100 0000 FN_4=FN_3=FN_2 = 0	V_{CC} = 3 V	1.25		4.7	MHz
			V_{CC} = 5 V	1.45		5.5	
$2xf_{(NOM)}$	$f_{(DCO3)}$	$N_{(DCO)}$ = 00 0110 0000 FN_4=FN_3=0, FN_2 = 1	V_{CC} = 3 V	0.36		1.05	MHz
			V_{CC} = 5 V	0.39		1.2	
	$f_{(DCO26)}$	$N_{(DCO)}$ = 11 0100 0000 FN_4=FN_3=0, FN_2 = 1	V_{CC} = 3 V	2.5		8.1	MHz
			V_{CC} = 5 V	3		9.9	
$3xf_{(NOM)}$	$f_{(DCO3)}$	$N_{(DCO)}$ = 00 0110 0000 FN_4=0, FN_3=1, FN_2=X	V_{CC} = 3 V	0.5		1.5	MHz
			V_{CC} = 5 V	0.6		1.8	
	$f_{(DCO26)}$	$N_{(DCO)}$ = 11 0100 0000 FN_4=0,FN_3 =1, FN_2=X	V_{CC} = 3 V	3.7		11	MHz
			V_{CC} = 5 V	4.5		13.8	
$4xf_{(NOM)}$	$f_{(DCO3)}$	$N_{(DCO)}$ = 00 0110 0000 FN_4=1, FN_3 = FN_2=X	V_{CC} = 3 V	0.7		1.85	MHz
			V_{CC} = 5 V	0.8		2.4	
	$f_{(DCO26)}$	$N_{(DCO)}$ = 11 0100 0000 FN_4=1, FN_3 = FN_2=X	V_{CC} = 3 V	4.8		13.3	MHz
			V_{CC} = 5 V	6		17.7	
$N_{(DCO)}$		$f_{(MCLK)} = f_{(NOM)}$ FN_4=FN_3=FN_2 = 0	V_{CC} = 3 V/5 V	A0h	1A0h	340h	
S		$f_{(NDCO)+1} = S \times f_{(NDCO)}$	V_{CC} = 3 V/5 V	1.07		1.13	

electrical characteristics over recommended and operating free-air temperature range (unless otherwise noted) (continued)



RAM

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 17)	1.8			V

NOTE 17: This parameter defines the minimum supply voltage when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

Timer/Port comparator

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(com)}$	Comparator (Timer/Port)	CPON = 1	V_{CC} = 3 V		175	350	µA
			V_{CC} = 5 V			600	
$V_{ref(COM)}$	Internal reference voltage at (–) terminal	CPON = 1	V_{CC} = 3 V/5 V	$0.230 \times V_{CC1}$		$0.260 \times V_{CC1}$	V
$V_{hys(COM)}$	Input hysteresis (comparator)		V_{CC} = 3 V		5	37	mV
		CPON = 1	V_{CC} = 5 V		10	42	mV

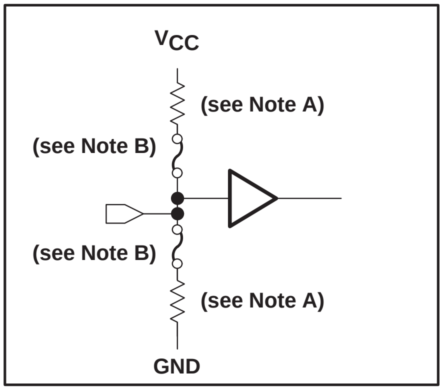
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

JTAG, program memory

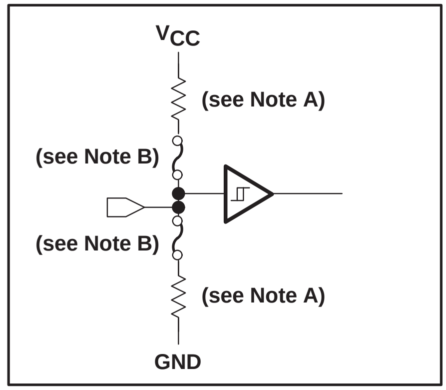
PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/Test	TCK frequency	V_{CC} = 3 V	DC		5	MHz
			V_{CC} = 5 V	DC		10	
$R_{(test)}$		Pullup resistors on TMS, TCK, TDI (see Note 18)	V_{CC} = 3 V/5 V	25	60	90	kΩ
$V_{(FB)}$	JTAG/Fuse (see Note 19)	Fuse blow voltage, C versions (see Note 20)	V_{CC} = 3 V/5 V	5.5		6.0	
		Fuse blow voltage, E/P versions (see Note 20)	V_{CC} = 3 V/5 V	11.0		12.0	
$I_{(FB)}$		Supply current on TDI/VPP to blow fuse				100	mA
$t_{(FB)}$		Time to blow the fuse				1	ms
$V_{(PP)}$	EPROM(E) and OTP(P) versions only	Programming voltage, applied to TDI/VPP	V_{CC} = 5 V	12.0	12.5	13.0	V
$I_{(PP)}$		Current from programming voltage source	V_{CC} = 5 V			70	mA
$t_{(pps)}$		Programming time, single pulse	V_{CC} = 5 V	5			ms
$t_{(ppf)}$		Programming time, fast algorithm	V_{CC} = 5 V		100		µs
P_n		Number of pulses for successful programming	V_{CC} = 5 V	4		100	
		Data retention T_J <55°C		10			Year
$t_{(erase)}$	EPROM(E) version only	Erase time wave length 2537 Å at 15 Ws/cm^2 (UV lamp of 12 mW/ cm^2)		30			min
		Write/erase cycles		1000			

NOTES: 18. The TMS and TCK pullup resistors are implemented in all ROM(C), OTP(P) and EPROM(E) versions. The pullup resistor on TDI is implemented in C versions only.
19. Once the fuse is blown no further access to the MSP430 JTAG/test feature is possible.
20. The voltage supply to blow the fuse is applied to TDI/VPP pin during the fuse blowing procedure.

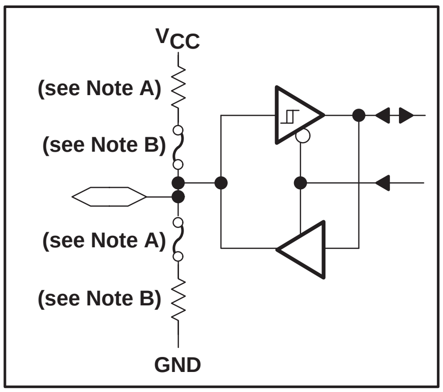
typical input/output schematics



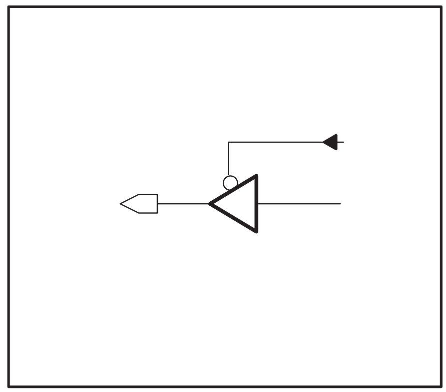
CMOS INPUT



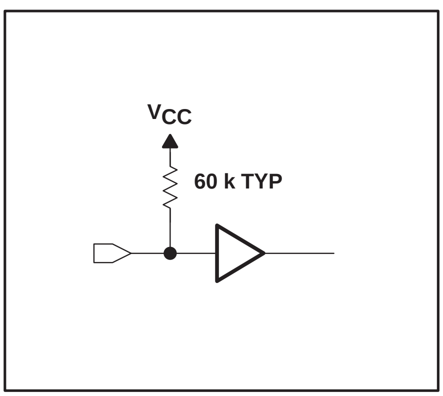
CMOS SCHMITT-TRIGGER INPUT



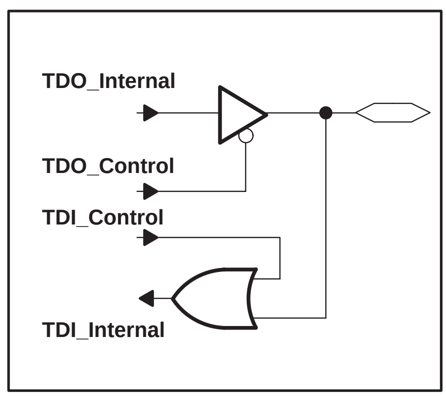
I/O WITH SCHMITT-TRIGGER INPUT



CMOS 3-STATE OUTPUT



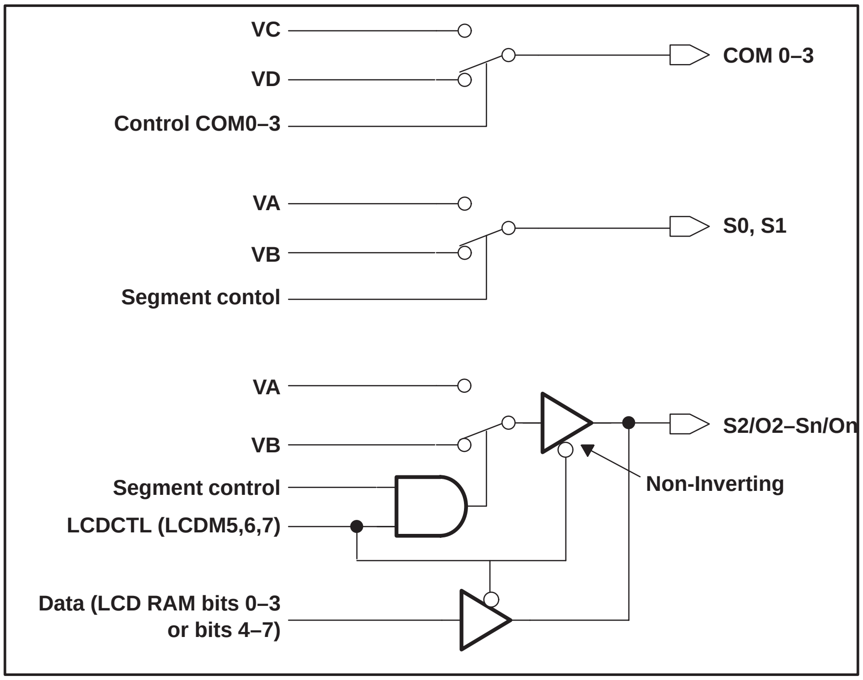
MSP430C336/337: TMS, TCK, TDI
MSP430P/E337A: TMS, TCK



MSP430C33x: TDO/TDI
MSP430P/E337A: TDO/TDI

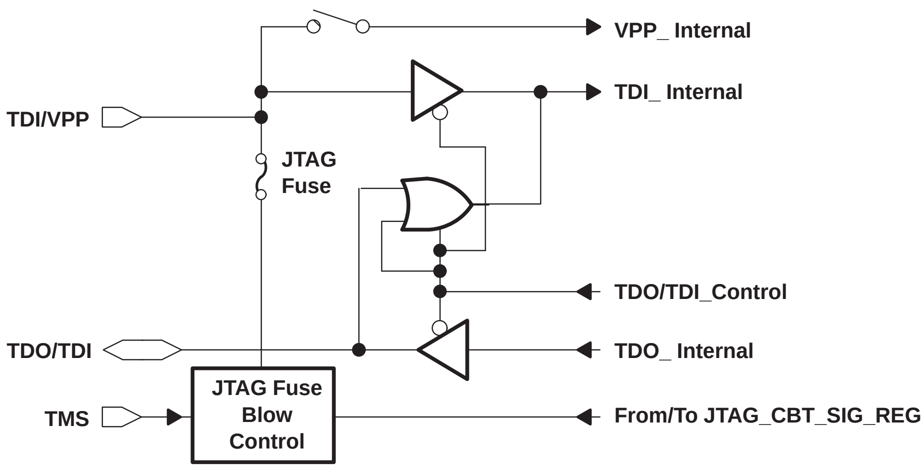
NOTES: A. Optional selection of pullup or pulldown resistors available on ROM (masked) versions.
B. Fuses for the optional pullup and pulldown resistors can only be programmed at the factory.

typical input/output schematics



LCD OUTPUT (COM0–4, Sn, Sn/On)

NOTE A: The signals VA, VB, VC, and VD come from the LCD module analog voltage generator.



NOTES: A. During programming activity and when blowing the JTAG enable fuse, the TDI/VPP terminal is used to apply the correct voltage source. The TDO/TDI terminal is used to apply the test input data for JTAG circuitry.

B. The TDI/VPP terminal of the ’P337A and ’E337A does not have an internal pullup resistor. An external pulldown resistor is recommended to avoid a floating node, which could increase the current consumption of the device. **Remove the external pulldown resistors when switching from P/E337A to C337 devices. Otherwise system power consumption will increase.**

C. The TDO/TDI terminal is in a high-impedance state after POR. The ’P337A and ’E337A need a pullup or a pulldown resistor to avoid floating a node, which could increase the current consumption of the device.

Figure 5. MSP430P/E337A: TDI/VPP, TDO/TDI

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/VPP terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/VPP pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

Fuse check current may or may not flow continuously while the fuse check mode is active, depending on which type of device is in use and the state of the TMS pin.

For the mask ROM or C versions, the fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 6). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

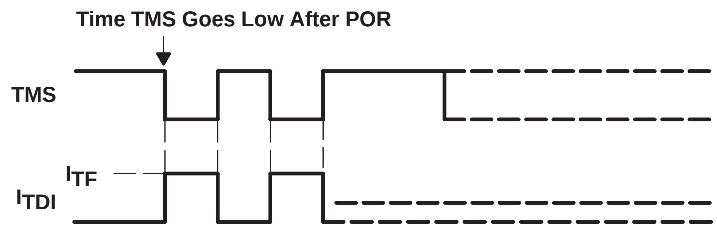


Figure 6. Fuse Check Mode Current, MSP430C33xA

For the OTP or P versions, the fuse check current will flow continuously when fuse check mode is active, regardless of the state of the TMS pin, until the fuse check mode is deactivated with the second positive edge at the TMS pin (see Figure 7).

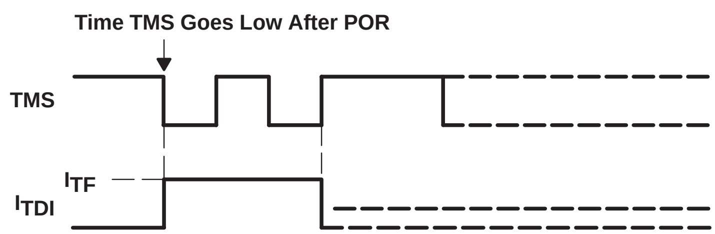


Figure 7. Fuse Check Mode Current, MSP430P337A

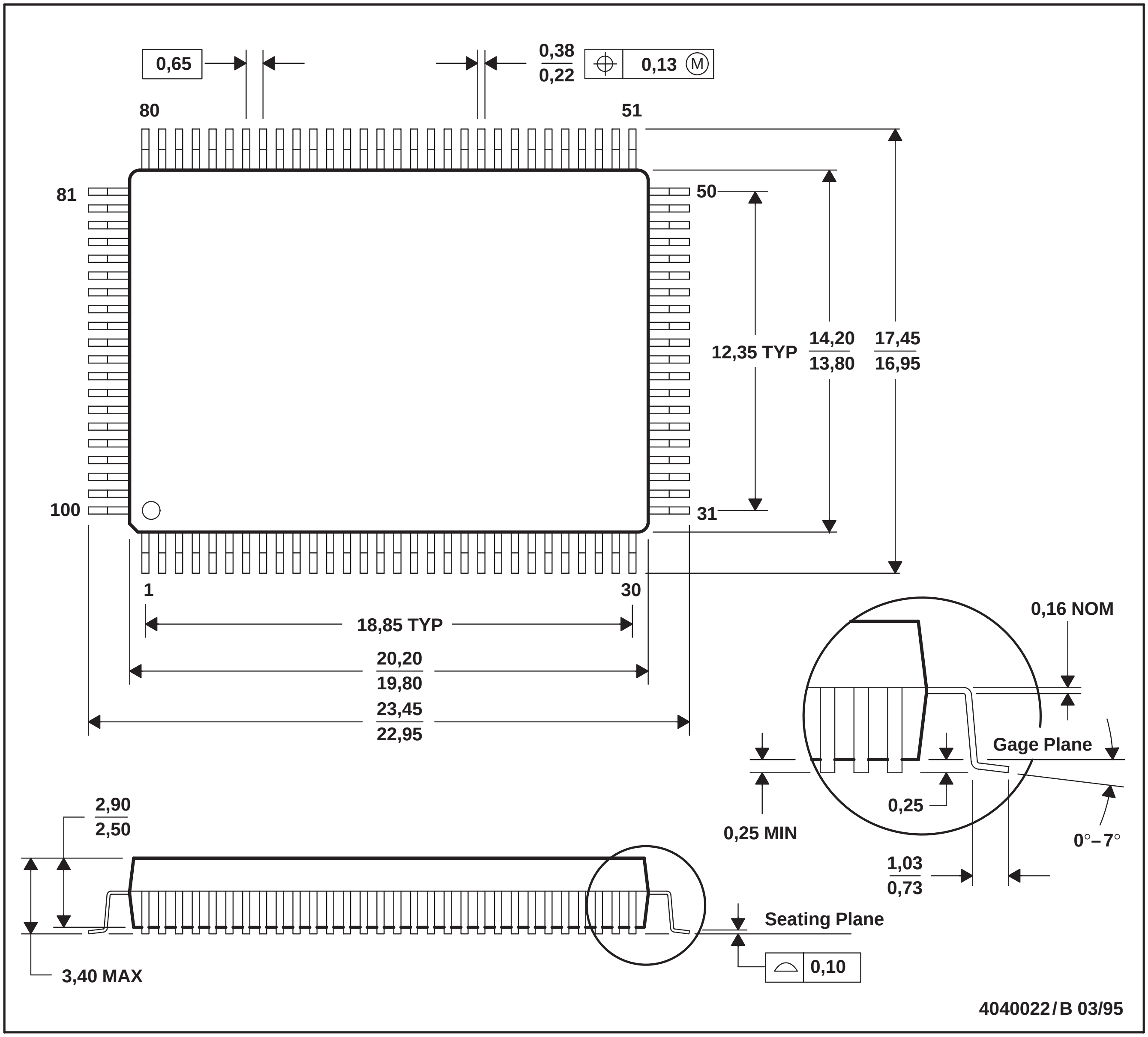
Care must be taken to avoid accidentally activating the fuse check mode, including guarding against EMI/ESD spikes that could cause signal edges on the TMS pin.

Configuration of TMS, TCK, TDI/VPP and TDO/TDI pins in applications.

	C3xx	P/E3xx
TDI	Open	68k, pull down
TDO	Open	68k, pull down
TMS	Open	Open
TCK	Open	Open

MECHANICAL DATA

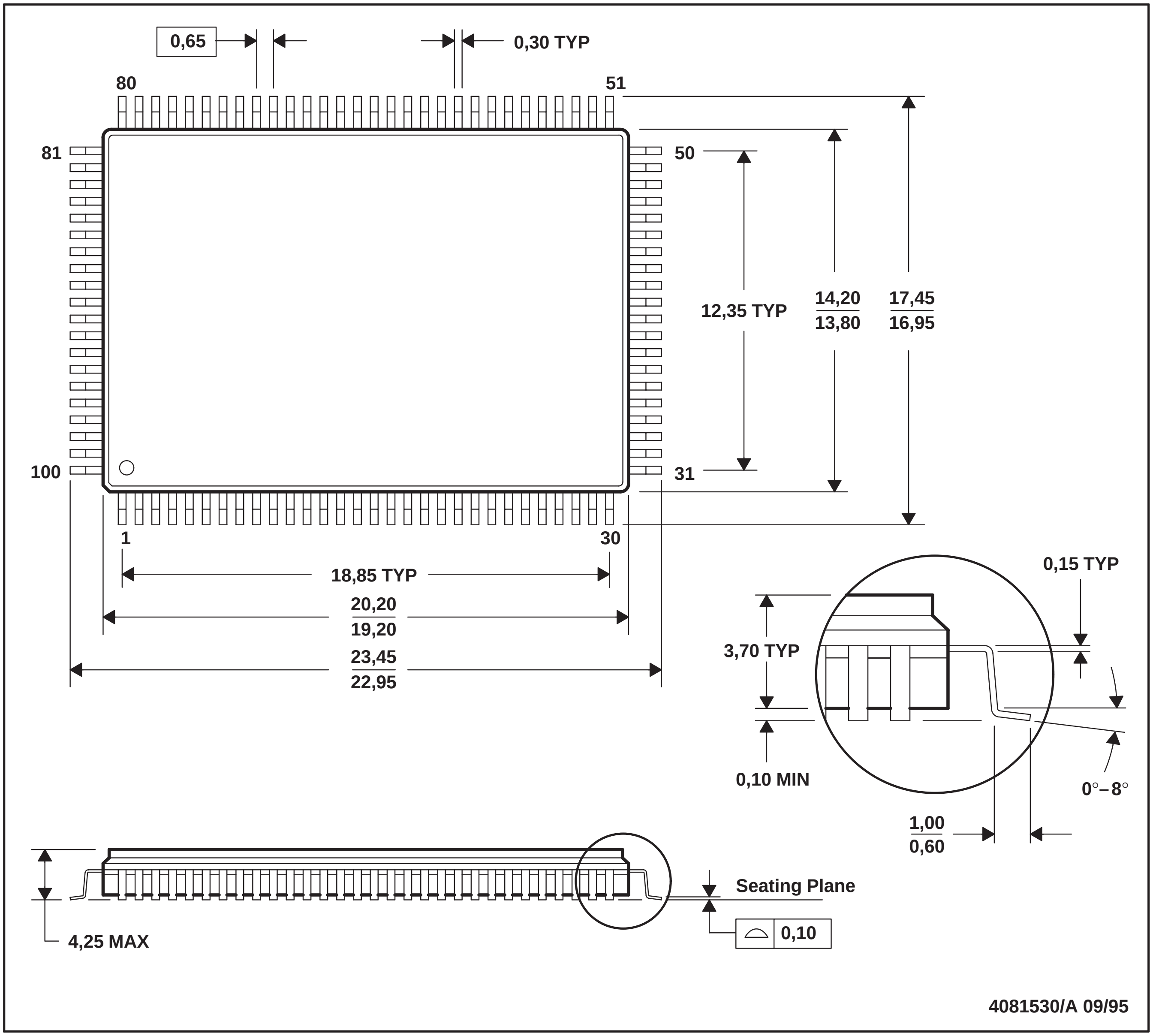
PJM (R-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

MECHANICAL DATA

HFD (S-GQFP-G100) **CERAMIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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