

# SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

SCDS031G – MAY 1996 – REVISED SEPTEMBER 1998

- Standard '16244-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages, and Ceramic Flat (WD) Package

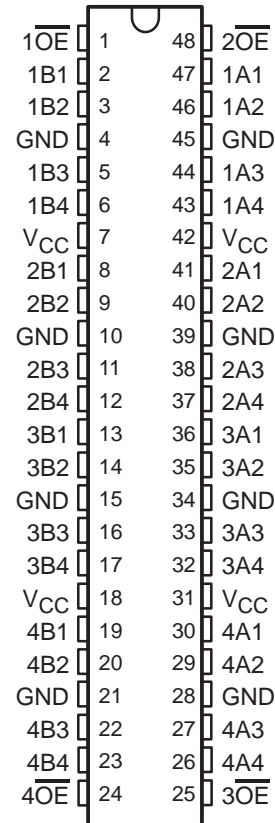
## description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the switch is on and data can flow from port A to port B, or vice versa. When  $\overline{OE}$  is high, the switch is open and a high-impedance state exists between the two ports.

The SN54CBT16244 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74CBT16244 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54CBT16244 . . . WD PACKAGE  
SN74CBT16244 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each 4-bit bus switch)

INPUT $\overline{OE}$	OUTPUTS A, B
L	A port = B port
H	Z



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 **TEXAS  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54CBT16244		SN74CBT16244		UNIT
			MIN	TYP†	MAX	MIN	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V
$I_I$	$V_{CC} = 0$	$V_I = 5.5\text{ V}$	10		10		$\mu\text{A}$
	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V or GND}$	$\pm 1$		$\pm 1$		
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$	$I_O = 0$ ,	3.2		3		$\mu\text{A}$
$\Delta I_{CC}\ddagger$	Control inputs $V_{CC} = 5.5\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$	One input at $3.4\text{ V}$ ,	2.5		2.5		mA
$C_i$	Control inputs $V_I = 3\text{ V or 0}$		2.5		2.5		pF
$C_{io(OFF)}$	$V_O = 3\text{ V or 0}$ ,	$\overline{OE} = V_{CC}$	4.5		4.5		pF
$r_{on}\S$	$V_{CC} = 4\text{ V}$ ,	$V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$	20		20		$\Omega$
		$V_I = 0$ , $I_I = 64\text{ mA}$	5	10	5	7	
	$V_{CC} = 4.5\text{ V}$	$V_I = 0$ , $I_I = 30\text{ mA}$	5	10	5	7	
		$V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$	8	14	8	12	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16244				SN74CBT16244				UNIT
			$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}\parallel$	A or B	B or A			0.8*		0.35		0.25		ns
$t_{en}$	$\overline{OE}$	A or B	10.3		1	9.2	5.5		1	5.1	ns
$t_{dis}$	$\overline{OE}$	A or B	9.7		1	8.2	5.2		1	5.4	ns

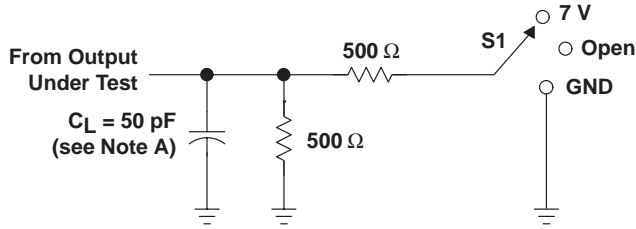
\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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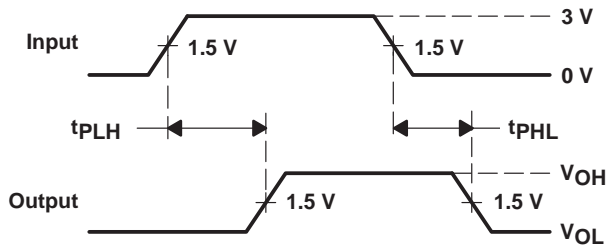
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## PARAMETER MEASUREMENT INFORMATION

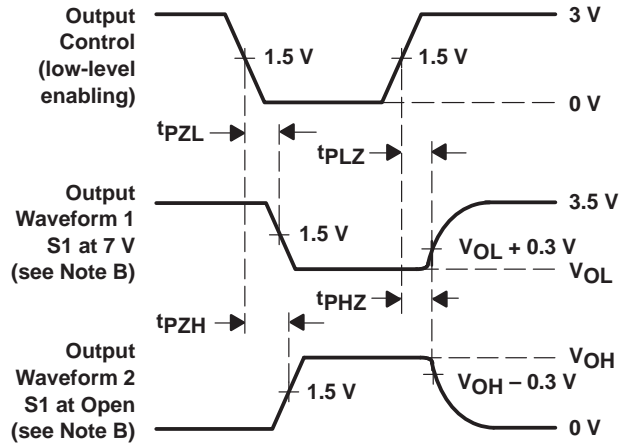


LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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