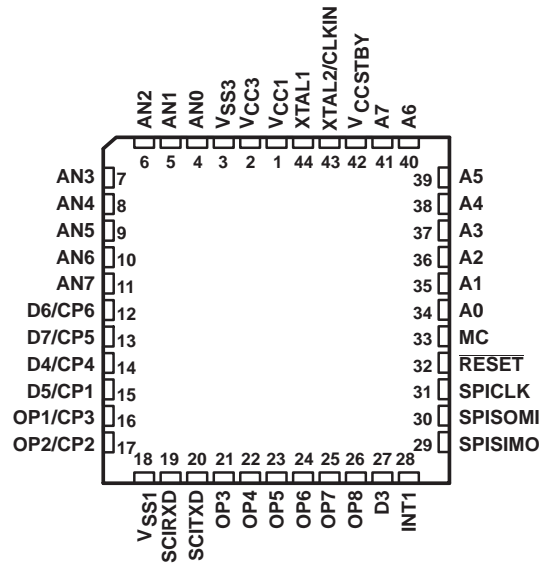


TMS370Cx36 8-BIT MICROCONTROLLER

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- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable-EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 16K Bytes
 - EPROM: 16K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 256 Bytes Usable as Registers
 - Standby RAM With Separate Power Supply Pin: 256 Bytes
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-1 (2 MHz–5 MHz SYSCLK) Phase-Locked Loop (PLL)
 - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
 - Supply Voltage (V_{CC}) 5 V \pm 10%
- **Programmable Acquisition and Control Timer (PACT) Module**
 - Input Capture on up to Six Pins, Four of Which Can Have a Programmable Prescaler
 - One Input Capture Pin Can Drive an 8-Bit Event Counter
 - Up to Eight Timer-Driven Outputs
 - Interaction Between Event Counter and Timer Activity
 - 18 Independent Interrupt Vectors
 - Watchdog With Selectable Time-Out Period
 - Asynchronous Mini Serial Communication Interface (Mini SCI)
- **Flexible Interrupt Handling**
 - Two Software-Programmable Interrupt Levels
 - Global- and Individual-Interrupt Masking
 - Programmable Rising- or Falling-Edge Detect
 - Individual-Interrupt Vectors

FZ AND FN PACKAGES
(TOP VIEW)



- **Serial Peripheral Interface (SPI)**
 - Variable-Length High-Speed Shift Register
 - Synchronous Master/Slave Operation
- **Eight Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With All TMS370 Devices
- **CMOS/TTL Compatible I/O Pins/Packages**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 16 Bidirectional Pins, Nine Input Pins
 - 44-Pin Plastic and Ceramic Leaded Chip Carrier (LCC) Packages
- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Multi-Window User Interface
 - Microcontroller Programmer



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 **TEXAS
INSTRUMENTS**

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Pin Descriptions

| 44 PINS | | I/O† | DESCRIPTION |
|--|--|--------|--|
| NAME | NO. | | |
| A0 A1 A2 A3 A4 A5 A6 A7 | 34 35 36 37 38 39 40 41 | I / O | Port A is a general-purpose bidirectional I/O port. |
| D3 D4/CP4 D5/CP1 D6/CP6 D7/CP5 | 27 14 15 12 13 | I / O | Port D is a general-purpose bidirectional port. Also configurable as SYSCLK (see Note 1) PACT input capture 4 (see Note 2) PACT input capture 1 (see Note 2) PACT input capture 6 (see Note 2) PACT input capture 5 (see Note 2) |
| AN0/E0 AN1/E1 AN2/E2 AN3/E3 AN4/E4 AN5/E5 AN6/E6 AN7/E7 | 4 5 6 7 8 9 10 11 | I | ADC1 analog input pins (AN0–AN7)/port E digital input pins (E0–E7) Port E can be programmed individually as a general-purpose digital input pin if it is not used as ADC1 analog input or positive reference input. |
| INT1 | 28 | I | External interrupt (non-maskable or maskable)/general-purpose input pin |
| OP1/CP3 OP2/CP2 OP3 OP4 OP5 OP6 OP7 OP8 | 16 17 21 22 23 24 25 26 | O | PACT PWM output 1/input capture 3 (see Note 3) PACT output pin 2/input capture 2 (see Note 3) PACT PWM output 3 PACT PWM output 4 PACT PWM output 5 PACT PWM output 6 PACT PWM output 7 PACT PWM output 8 |
| SCIRXD SCITXD | 19 20 | I O | PACT mini SCI data receive input pin PACT mini SCI data transmit output pin |
| SPISOMI SPISIMO SPICLK | 30 29 31 | I / O | SPI slave output pin, master input pin/general-purpose bidirectional pin SPI slave input pin, master output pin/general-purpose bidirectional pin SPI bidirectional serial clock pin/general-purpose bidirectional pin |
| <u>RESET</u> | 32 | I / O | System reset bidirectional pin; as input pin, <u>RESET</u> initializes the microcontroller; as open-drain output, <u>RESET</u> indicates that an internal failure was detected by watchdog or oscillator fault circuit. |
| MC | 33 | I | Mode control input pin; enables EEPROM write protection override (WPO) mode, also EPROM V _{PP} |
| XTAL2/CLKIN XTAL1 | 43 44 | I O | Internal oscillator crystal input/External clock source input Internal oscillator output for crystal |
| VCC1 VSS1 VCC3 VSS3 VCCSTBY | 1 18 2 3 42 | | Positive supply voltage for digital logic and digital I/O pins Ground reference for digital logic and digital I/O pins ADC1 positive supply voltage and optional positive reference input ADC1 ground supply and low reference input pin Positive supply voltage pin for standby RAM |

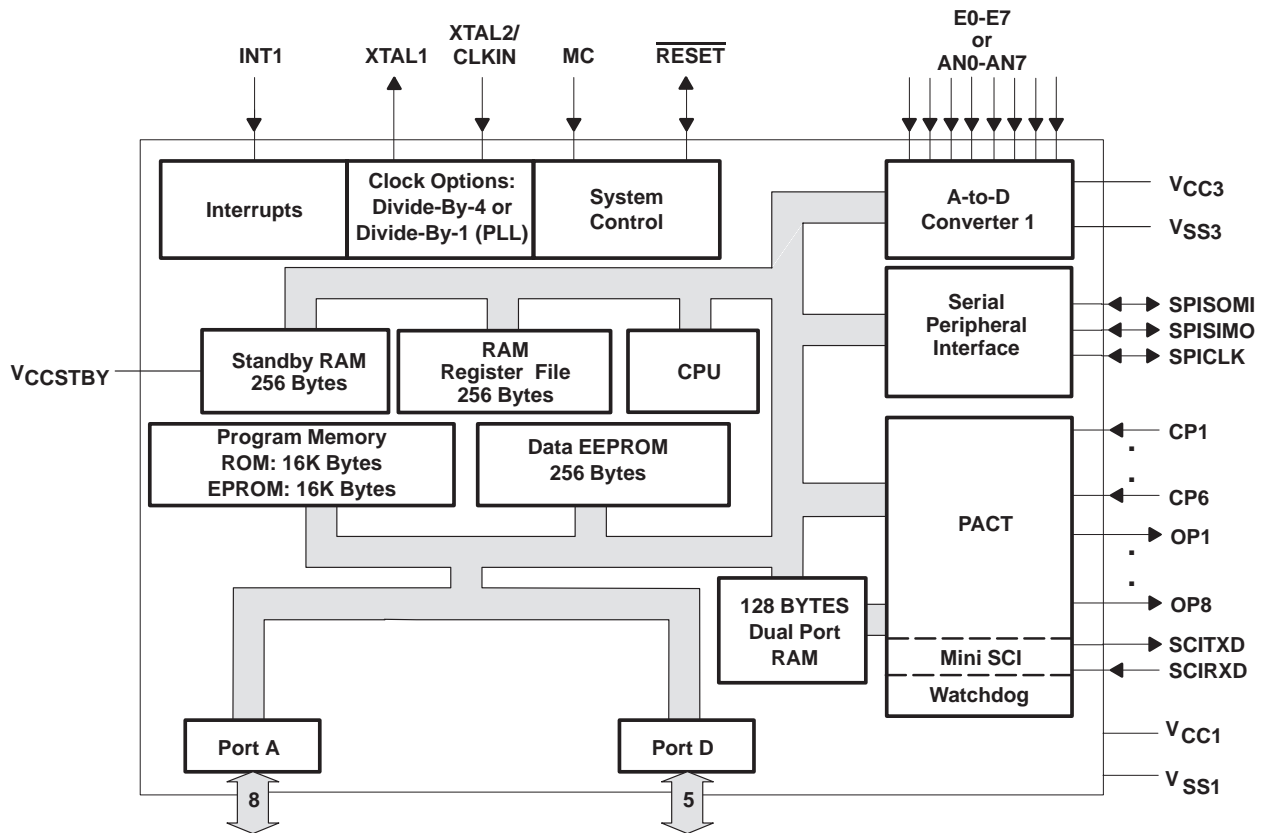
† I = input, O = output

- NOTES:
1. D3 can be configured as SYSCLK by appropriately programming the DPORT1 and DPORT2 registers.
 2. These digital I/O buffers are connected internally to some of the PACT module's input capture pins. This allows the microcontroller to read the level on the input capture pin, or if the port D pin is configured as an output, to generate a capture. Be careful to leave the port D pin configured as an input if the corresponding input capture pin is being driven by external circuitry.
 3. CP2 and CP3 are connected internally to OP2 and OP1. CP2 and CP3 can be used only to capture OP2 and OP1, respectively and not as external capture inputs.



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functional block diagram



description

The TMS370C036, TMS370C736, and SE370C736 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx36 refers to these devices. The TMS370 family provides cost-effective real-time system control through advanced peripheral-function modules and various on-chip memory configurations.

The TMS370Cx36 family of devices uses high-performance silicon-gate CMOS EPROM and EEPROM technologies. Low operating power, wide operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx36 devices attractive for system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx36 devices contain the following on-chip peripheral modules:

- Programmable acquisition and control timer (PACT)
 - Asynchronous mini SCI
 - PACT watchdog timer
- Serial peripheral interface (SPI)
- Eight channel, 8-bit analog-to-digital converter 1 (ADC1)

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description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx36 devices.

Table 1. Memory Configurations

| DEVICE | PROGRAM MEMORY (BYTES) | | DATA MEMORY (BYTES) | | 44 PIN PACKAGES |
|-------------|------------------------|-------|---------------------|--------|-----------------|
| | ROM | EPROM | RAM | EEPROM | |
| TMS370C036A | 16K | — | 512 | 256 | FN – PLCC |
| TMS370C736A | — | 16K | 512 | 256 | FN – PLCC |
| SE370C736A† | — | 16K | 512 | 256 | FZ – CLCC |

† System evaluators and development are for use only in prototype environment, and their reliability has not been characterized.

The suffix letter A appended to the device names in Table 1 indicates the configuration of the devices. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

| DEVICE† | CLOCK | LOW-POWER MODE |
|---------|-----------------------------------|---------------------|
| EPROM A | Divide-by-4 (Standard oscillator) | Enabled |
| ROM A | Divide-by-4 or Divide-by-1 (PLL) | Enabled or disabled |

† Refer to the “device numbering conventions” section for device nomenclature and to the “device part numbers” section for ordering.

The 16K bytes of mask-programmable ROM in the associated TMS370Cx36 devices are replaced in the TMS370C736 with 16K bytes of EPROM. All other available memory and on-chip peripherals are identical. The OTP (TMS370C736) and reprogrammable (SE370C736) devices are available.

The TMS370C736 OTP device is available in a plastic package. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx36 family or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C736 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C736 device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx36 family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator, the PACT counter, and PACT's first command/definition entry remain active. This allows the PACT module to bring the device out of STANDBY mode. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx36 features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx36 family is fully instruction-set-compatible, providing easy transition between members of the family.

The TMS370Cx36 has a PACT module that acts as a timer coprocessor by gathering timing information on input signals and controlling output signals with little or no intervention by the CPU. The coprocessor nature of this module allows for levels of flexibility and power not found in traditional microcontroller timers.



description (continued)

The TMS370Cx36 family provides the system designer with an economical, efficient solution to real-time control applications. The PACT compact development tool (CDT™) meets the challenge of efficiently developing the software and hardware required to design the TMS370Cx36 into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as a reduced time-to-market cycle.

The TMS370Cx36 family together with the TMS370 PACT CDT370, BP programmer, software tools, SE370C736 reprogrammable devices, comprehensive product documentation, and customer support provides a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU on the TMS370Cx36 device is the high-performance 8-bit TMS370 CPU module. The 'x36 implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x36 instruction map is shown in Table 16.

The '370Cx36 CPU architecture provides the following components:

CPU registers:

- A stack pointer (SP) that points to the last entry in the memory stack
- A status register (ST) that monitors the operation of the instructions and contains the global interrupt-enable bits
- A program counter (PC) that points to the memory location of the next instruction to be executed

A memory map that includes:

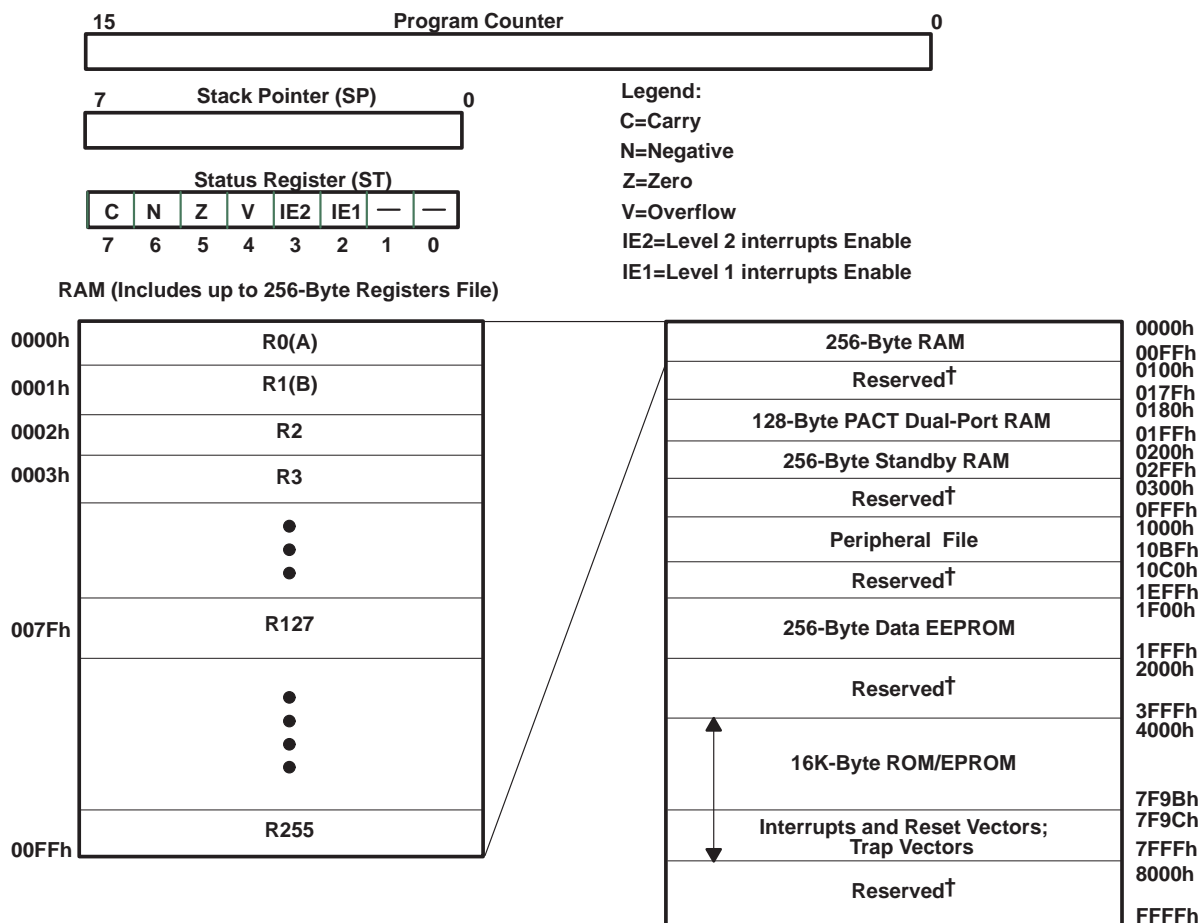
- 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general purpose register, or the stack
- 256-byte general-purpose standby RAM, which is powered through a separate V_{CCSTBY} pin to protect the memory against power failures on the main V_{CC1} pins
- 128-byte dual-port RAM that contains the capture registers, the circular buffer, and a command/definition area
- A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
- 256-byte EEPROM module, that provides in-circuit programmability and data retention in power-off conditions
- 16K-byte ROM or 16K-byte EPROM

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central processing unit (CPU) (continued)

Figure 1 Illustrates the CPU registers and memory blocks.



† Reserved means the address space is reserved for future expansion.

Figure 1. Programmer's Model

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. Typically, the stack is used to store the return address on subroutine calls as well as the ST contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits.

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

central processing unit (CPU) (continued)

The ST, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

| | | | | | | | |
|------|------|------|------|------|------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| C | N | Z | V | IE2 | IE1 | Reserved | Reserved |
| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | | |

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the PC. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 4000h as the contents of the reset vector.

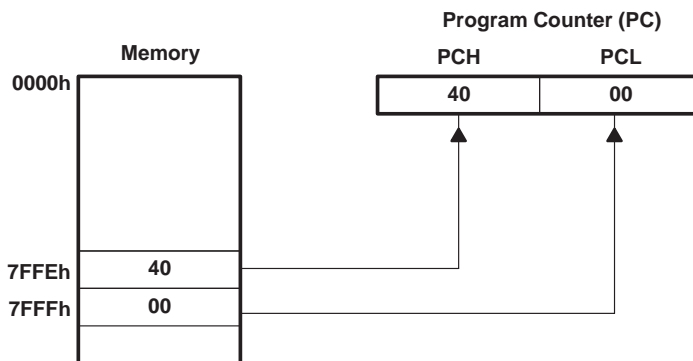


Figure 2. Program Counter After Reset

memory map

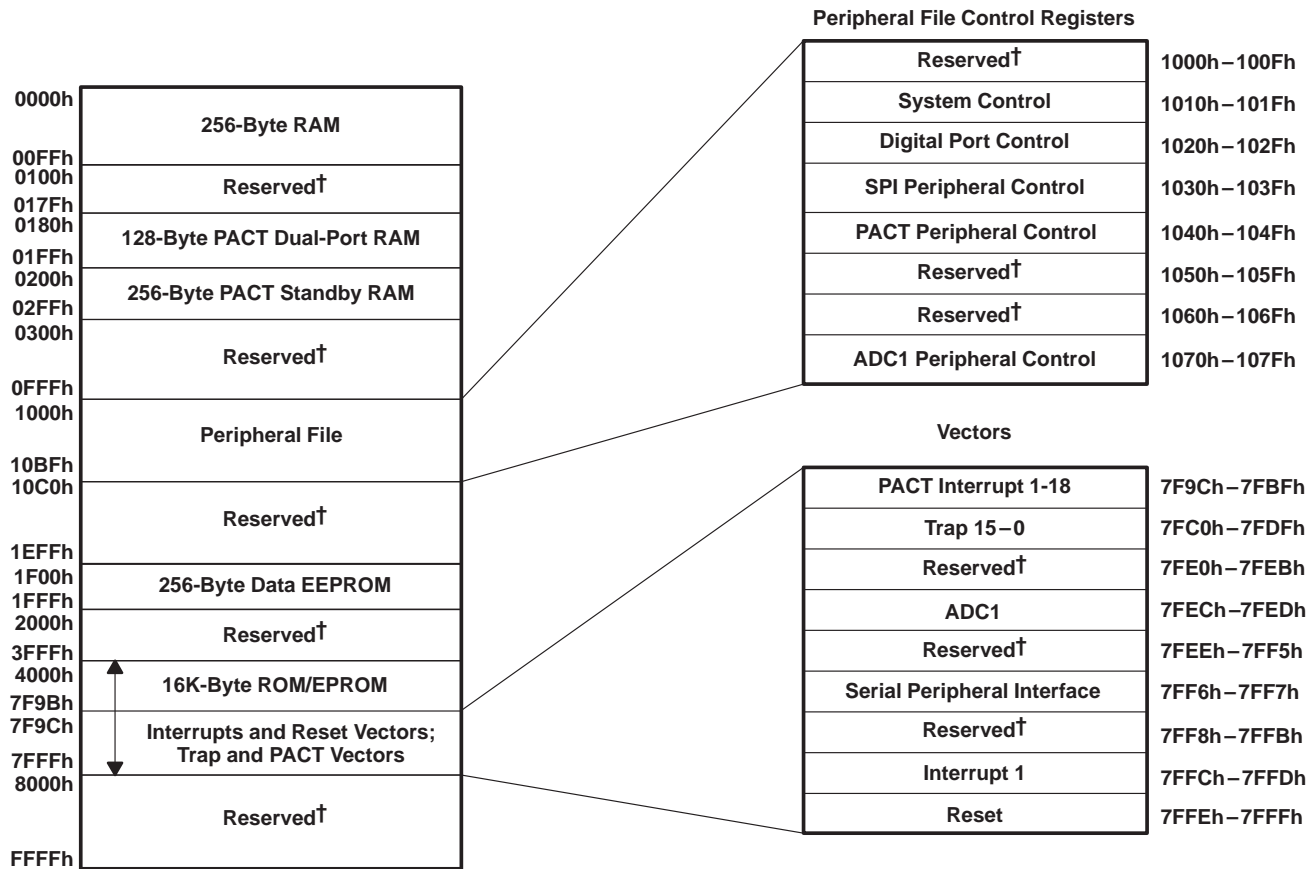
The TMS370Cx36 architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx36 provides memory-mapped RAM, ROM, EPROM, data EEPROM, I/O pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all I/O port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file is located between 1000h to 107Fh and is divided logically into eight peripheral file frames of 16 bytes each. The eight PF frames consist of five control frames and three reserved frames. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information are passed.

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central processing unit (CPU) (continued)



† Reserved means that the address space is reserved for future expansion.

Figure 3. TMS370Cx36 Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx36 devices contain 256 bytes of internal RAM, memory-mapped beginning at location 0000h (R0) and continuing through location 00FFh (R255) which is shown in Figure 1.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

dual-port RAM

The upper 128 bytes of the register files can be used by the PACT module to contain commands and definitions as well as timer values. Any RAM not used by PACT can be used as an additional CPU register or as general-purpose memory.



standby RAM module

The 256 byte standby RAM is general-purpose and powered through a separate V_{CCSTBY} pin. The data stored in this memory is protected against power failures on the main V_{CC1} pins.

The standby RAM data is saved if the power failure on the main V_{CC1} pins is detected externally and an external reset is generated when V_{CC1} falls below 4.3 V (see Figure 4). The external reset must remain low during the entire power failures. The falling edge of the reset signal is internally detected to set the standby RAM in low-power HALT mode. After the next power up, the \overline{RESET} pin must be pulled high to get out of the HALT mode of the standby RAM. In halt mode, the standby RAM consumes only leakage current.

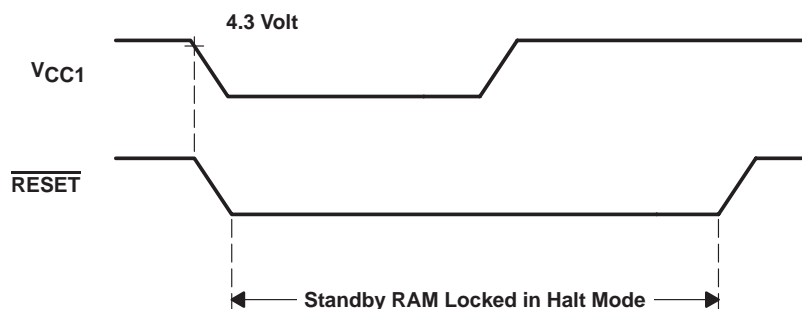


Figure 4. Standby RAM Locked in Halt Mode

peripheral file (PF)

The TMS370Cx36 control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system-control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 lists the TMS370Cx36 PF address map.

Table 4. TMS370Cx36 Peripheral File Address Map

| ADDRESS RANGE | PERIPHERAL FILE DESIGNATOR | DESCRIPTION |
|---------------|----------------------------|---|
| 1000h–100Fh | P000–P00F | Reserved |
| 1010h–101Fh | P010–P01F | System and EPROM/EEPROM control registers |
| 1020h–102Fh | P020–P02F | Digital I/O port control registers |
| 1030h–103Fh | P030–P03F | SPI registers |
| 1040h–104Fh | P040–P04F | PACT registers |
| 1050h–106Fh | P050–P06F | Reserved |
| 1070h–107Fh | P070–P07F | Analog-to-digital converter 1 registers |
| 1080h–10FFh | P080–P0FF | Reserved |

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data EEPROM

The TMS370Cx36 devices, containing 256 bytes of data EEPROM, have a memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes.
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A. See Table 5.
 - In-circuit programming capability. There is no need to remove the device to program.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5. Data EEPROM and PROGRAM EPROM Control Registers Memory Map

| ADDRESS | SYMBOL | NAME |
|---------|--------|--|
| P01A | DEECTL | Data EEPROM Control Register |
| P01B | — | Reserved |
| P01C | EPCTLL | Program EPROM Control Register – Low Array |

program EPROM†

The TMS370Cx36 device contains 16K bytes of EPROM mapped, beginning at location 4000h and continuing through location 7FFFh as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTLL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTLL) located in the peripheral file (PF) frame at location P01C as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted
 - Low-power modes
 - 13 V not applied to MC

† Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™), and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

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program ROM†

The program ROM consists of 16K bytes of mask programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Refer to Figure 3 for ROM memory map.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx36 CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one ($\overline{\text{RESET}}$ pin) is controlled externally. These actions are as follows:

- PACT watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x36 device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4) and the cold-start flag (COLD START, SCCR0.7) to determine the source of the reset. A reset does not clear these flags. Table 6 lists the reset sources. If none of the sources indicated in Table 6 caused the reset, then the $\overline{\text{RESET}}$ pin was pulled low by the external hardware or the PACT module's watchdog.

Table 6. Reset Sources

| REGISTER | ADDRESS | PF | BIT NO. | CONTROL BIT | SOURCE OF RESET |
|----------|---------|------|---------|--------------|-------------------------|
| SCCR0 | 1010h | P010 | 7 | COLD START | Cold (power-up) |
| SCCR0 | 1010h | P010 | 4 | OSC FLT FLAG | Oscillator out of range |

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

† Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments, and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

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interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the ST.

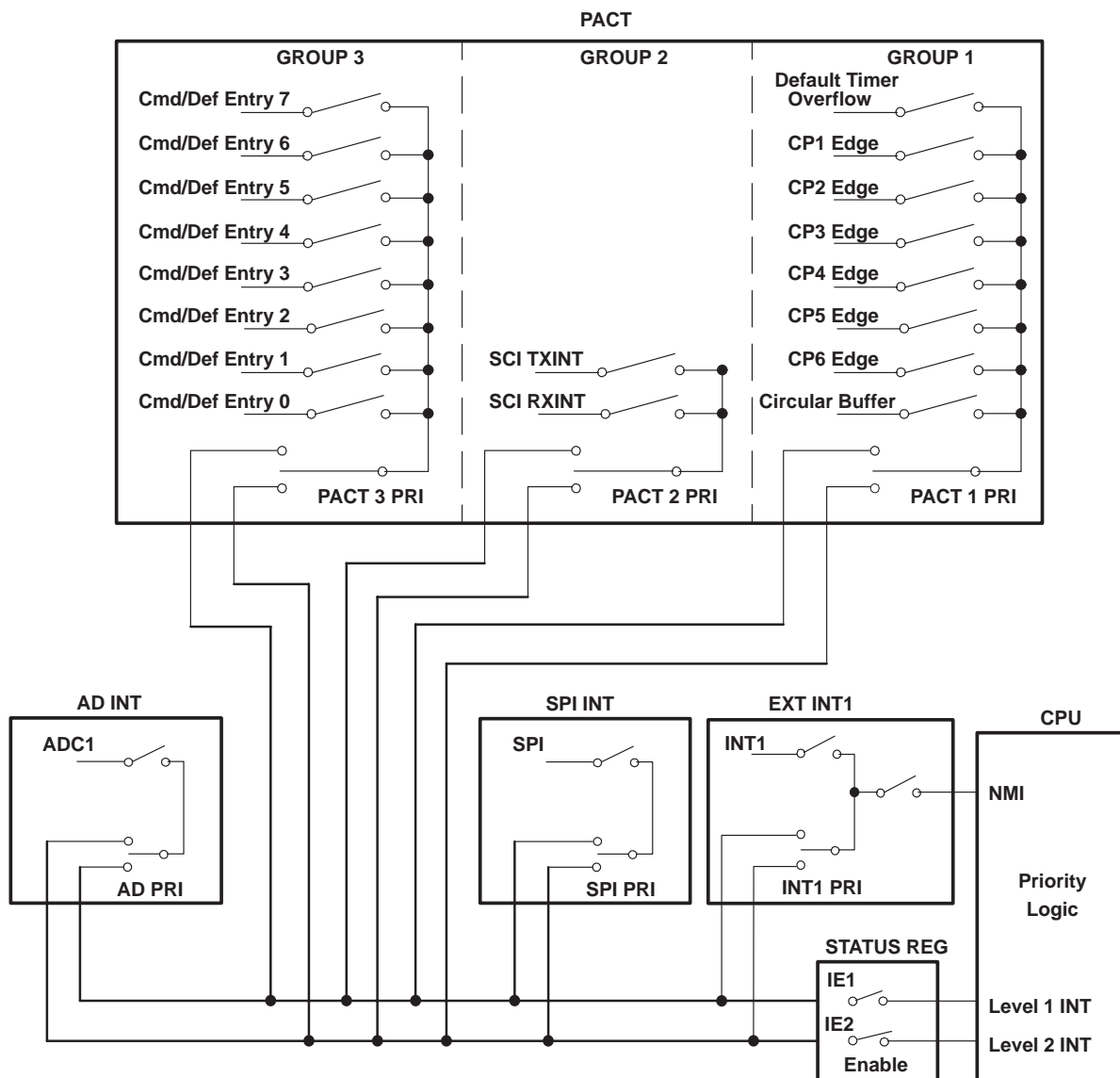


Figure 5. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high- or low-priority-interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx36 has 21 hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Twenty of the system interrupts are generated by on-chip peripheral functions, and one external interrupt is supported. Software configuration of the external interrupts is performed through the INT1 control register in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupt INT1 can be software configured as a general-purpose input pin if the interrupt function is not required.

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interrupts (continued)

Table 7. Hardware System Interrupts

| INTERRUPT SOURCE | INTERRUPT FLAG | OSC FLT FLG | SYSTEM INTERRUPT | VECTOR ADDRESS | MODULE PRIORITY† | PRIORITY IN GROUP |
|------------------|---|---|------------------|----------------|------------------|-------------------|
| RESET | External RESET Watchdog Overflow Oscillator Fault | COLD START (No Flag) OSC FLT FLAG | RESET‡ | 7FFEh, 7FFFh | 1 | |
| INT1 | External Interrupt 1 | INT1 FLAG | INT1‡ | 7FFCh, 7FFDh | 2 | |
| SPI | SPI RX/TX Complete | SPI INT FLAG | SPIINT | 7FF6h, 7FF7h | 3 | |
| PACT (Group 1) | PACT Circular Buffer | Buffer Half/Full Interrupt Flag | BUFINT | 7FB0h, 7FB1h | 4 | 1 |
| | PACT CP6 Event | CP6 INT FLAG | CP6INT | 7FB2h, 7FB3h | | 2 |
| | PACT CP5 Event | CP5 INT FLAG | CP5INT | 7FB4h, 7FB5h | | 3 |
| | PACT CP4 Event | CP4 INT FLAG | CP4INT | 7FB6h, 7FB7h | | 4 |
| | PACT CP3 Event | CP3 INT FLAG | CP3INT | 7FB8h, 7FB9h | | 5 |
| | PACT CP2 Event | CP2 INT FLAG | CP2INT | 7FBAh, 7FBBh | | 6 |
| | PACT CP1 Event | CP1 INT FLAG | CP1INT | 7FBCh, 7FBDh | | 7 |
| | Default Timer Overflow | DEFTIM OVRFL INT FLAG | POVRL INT | 7FBEh, 7FBFh | | 8 |
| PACT (Group 2) | PACT SCI Rx Int | PACT RX RDY | PRXINT | 7F9Eh, 7F9Fh | 5 | 1 |
| | PACT SCI Tx Int | PACT TX RDY | PTXINT | 7F9Ch, 7F9Dh | | 2 |
| PACT (Group 3) | PACT Cmd/Def Entry 0 | CMD/DEF INT 0 FLAG | CDINT 0 | 7FA0h, 7FA1h | 6 | 1 |
| | PACT Cmd/Def Entry 1 | CMD/DEF INT 1 FLAG | CDINT 1 | 7FA2h, 7FA3h | | 2 |
| | PACT Cmd/Def Entry 2 | CMD/DEF INT 2 FLAG | CDINT 2 | 7FA4h, 7FA5h | | 3 |
| | PACT Cmd/Def Entry 3 | CMD/DEF INT 3 FLAG | CDINT 3 | 7FA6h, 7FA7h | | 4 |
| | PACT Cmd/Def Entry 4 | CMD/DEF INT 4 FLAG | CDINT 4 | 7FA8h, 7FA9h | | 5 |
| | PACT Cmd/Def Entry 5 | CMD/DEF INT 5 FLAG | CDINT 5 | 7FAAh, 7FABh | | 6 |
| | PACT Cmd/Def Entry 6 | CMD/DEF INT 6 FLAG | CDINT 6 | 7FACH, 7FADh | | 7 |
| | PACT Cmd/Def Entry 7 | CMD/DEF INT 7 FLAG | CDINT 7 | 7FAEh, 7FAFh | | 8 |
| ADC1 | ADC1 Conversion Complete | AD INT FLAG | ADINT | 7FECh, 7FEDh | 7 | |

† Relative priority within an interrupt level

‡ Release microcontroller from STANDBY and HALT low-power modes

privileged operation and EEPROM write protection override

The TMS370Cx36 family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx36 operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1 to enter the nonprivileged mode, disabling write operations to specific configuration-control bits within the PF. Table 8 lists the control bits shown in the table which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.



privileged operation and EEPROM write protection override (continued)

Table 8. Privilege Bits

| REGISTER† | | CONTROL BIT |
|-----------|--|---|
| NAME | LOCATION | |
| SCCRO | P010.5 P010.6 | PF AUTO WAIT OSC POWER |
| SCCR1 | P011.2 P011.4 | MEMORY DISABLE AUTOWAIT DISABLE |
| SCCR2 | P012.0 P012.1 P012.3 P012.4 P012.6 P012.7 | PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY |
| SPIPRI | P03F.5 P03F.6 P03F.7 | SPI ESPEN SPI PRIORITY SPI STEST |
| PACTSCR | P040.0 P040.1 P040.2 P040.3 P040.4 | PACT PRESCALE SELECT 0 PACT PRESCALE SELECT 1 PACT PRESCALE SELECT 2 PACT PRESCALE SELECT 3 FAST MODE SELECT |
| PACTPRI | P04F.0 P04F.1 P04F.2 P04F.3 P04F.4 P04F.5 P04F.7 | PACT WD PRESCALE SELECT 0 PACT WD PRESCALE SELECT 1 PACT MODE SELECT PACT GROUP 3 PRIORITY PACT GROUP 2 PRIORITY PACT GROUP 1 PRIORITY PACT STEST |
| ADPRI | P07F.5 P07F.6 P07F.7 | AD ESPEN AD PRIORITY AD STEST |

† The privilege bits are shown in a bold typeface and shaded areas in the system configuration registers section of Table 10.

low-power and IDLE modes

The TMS370Cx36 devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, the PACT counter, and the first PACT command entry remain active in all modules. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$ or external interrupt on INT1) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx36 is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$ or external interrupt on the INT1) is detected. The power-down mode-selection bits are summarized in Table 9.



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low-power and IDLE modes (continued)

Table 9. Low-Power/Idle Control Bits

| POWER-DOWN CONTROL BITS | | MODE SELECTED |
|-------------------------|------------------------|---------------|
| PWRDWN/IDLE (SCCR2.6) | HALT/STANDBY (SCCR2.7) | |
| 1 | 0 | STANDBY |
| 1 | 1 | HALT |
| 0 | X † | IDLE |

† X = Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method for always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (SP, PC, and ST), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x36 family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x36 masked-ROM devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '736A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. These are formulated as follows:

$$\text{Divide-by-4 option : } \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : } \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the reduced EMI. The harmonics of low-speed resonators extend through fewer of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.



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system configuration registers

Table 10 contains system-configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded areas.

Table 10. Peripheral File Frame 1: System-Configuration Registers

| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REG |
|--------------|---------------------|--------------------|---------------------|--------------------------|------------------|-----------------------|-----------------|--------------------------|--------|
| P010 | COLD START | OSC POWER | PF AUTO WAIT | OSC FLT FLAG | MC PIN WPO | MC PIN DATA | — | μP/μC MODE | SCCR0 |
| P011 | — | — | — | AUTO WAIT DISABLE | — | MEMORY DISABLE | — | — | SCCR1 |
| P012 | HALT/STANDBY | PWRDWN/IDLE | — | BUS STEST | CPU STEST | — | INT1 NMI | PRIVILEGE DISABLE | SCCR2 |
| P013 to P016 | Reserved | | | | | | | | |
| P017 | INT1 FLAG | INT1 PIN DATA | — | — | — | INT1 POLARITY | INT1 PRIORITY | INT1 ENABLE | INT1 |
| P018 | Reserved | | | | | | | | |
| P019 | Reserved | | | | | | | | |
| P01A | BUSY | — | — | — | — | AP | W1W0 | EXE | DEECTL |
| P01B | Reserved | | | | | | | | |
| P01C | BUSY | VPPS | — | — | — | — | W0 | EXE | EPCTL |
| P01D to P01F | Reserved | | | | | | | | |

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digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 shows the specific addresses, registers, and control bits within this peripheral file frame. Table 12 shows the port configuration register setup.

Table 11. Peripheral File Frame 2: Digital Port-Control Registers

| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
|--------------------|--|-------|-------|-------|-------|-------|-------|-------|--------|
| P020 | Reserved | | | | | | | | APORT1 |
| P021 | Port A Control Register 2 (must be 0) | | | | | | | | APORT2 |
| P022 | Port A Data | | | | | | | | ADATA |
| P023 | Port A Direction | | | | | | | | ADIR |
| P024 to P02B | Reserved | | | | | | | | |
| P02C | Port D Control Register 1 (must be 0) | | | | | — | — | — | DPORT1 |
| P02D | Port D Control Register 2 (must be 0) [†] | | | | | — | — | — | DPORT2 |
| P02E | Port D Data | | | | | — | — | — | DDATA |
| P02F | Port D Direction | | | | | — | — | — | DDIR |

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

| PORT | PIN | abcd 00q1 | abcd 00y0 |
|---|-------|--------------|--------------|
| A | 0 – 7 | Data out q | Data In y |
| D | 3 – 7 | Data out q | Data In y |
| a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction | | | |

serial peripheral interface

The SPI is a high-speed synchronous serial I/O port that allows a serial bit stream of programmed length (one to eight bits) to be shifted into and out of the device at a programmable bit transfer rate. The SPI normally is used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion by way of devices such as shift registers, display drivers, and A/D converters. Multi-device communications are supported by the master/slave operation of the SPI. The SPI module features include the following:

- Three external pins
 - SPISOMI: SPI slave output/master input pin or general-purpose bidirectional I/O pin
 - SPISIMO: SPI slave input/master output pin or general-purpose bidirectional I/O pin
 - SPICLK: SPI serial clock pin or general-purpose bidirectional I/O pin
- Two operational modes: Master and slave



serial peripheral interface (continued)

- Baud rate: Eight different programmable rates
 - Maximum baud rate in master mode: 2.5M bps at 5-MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^b}$$

where b=bit rate in SPICCR.5-3 (range 0–7)

- Maximum baud rate in slave mode: 625K bps at 5-MHz SYSCLK
for maximum slave SPI BAUD RATE < SYSCLK/8
- Data word format: one to eight data bits
- Simultaneous receiver and transmitter operations (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Seven SPI module control registers located in control register frame beginning at address P030h

The SPI module-control registers are listed in Table 13.

Table 13. SPI Module-Control Register Memory Map

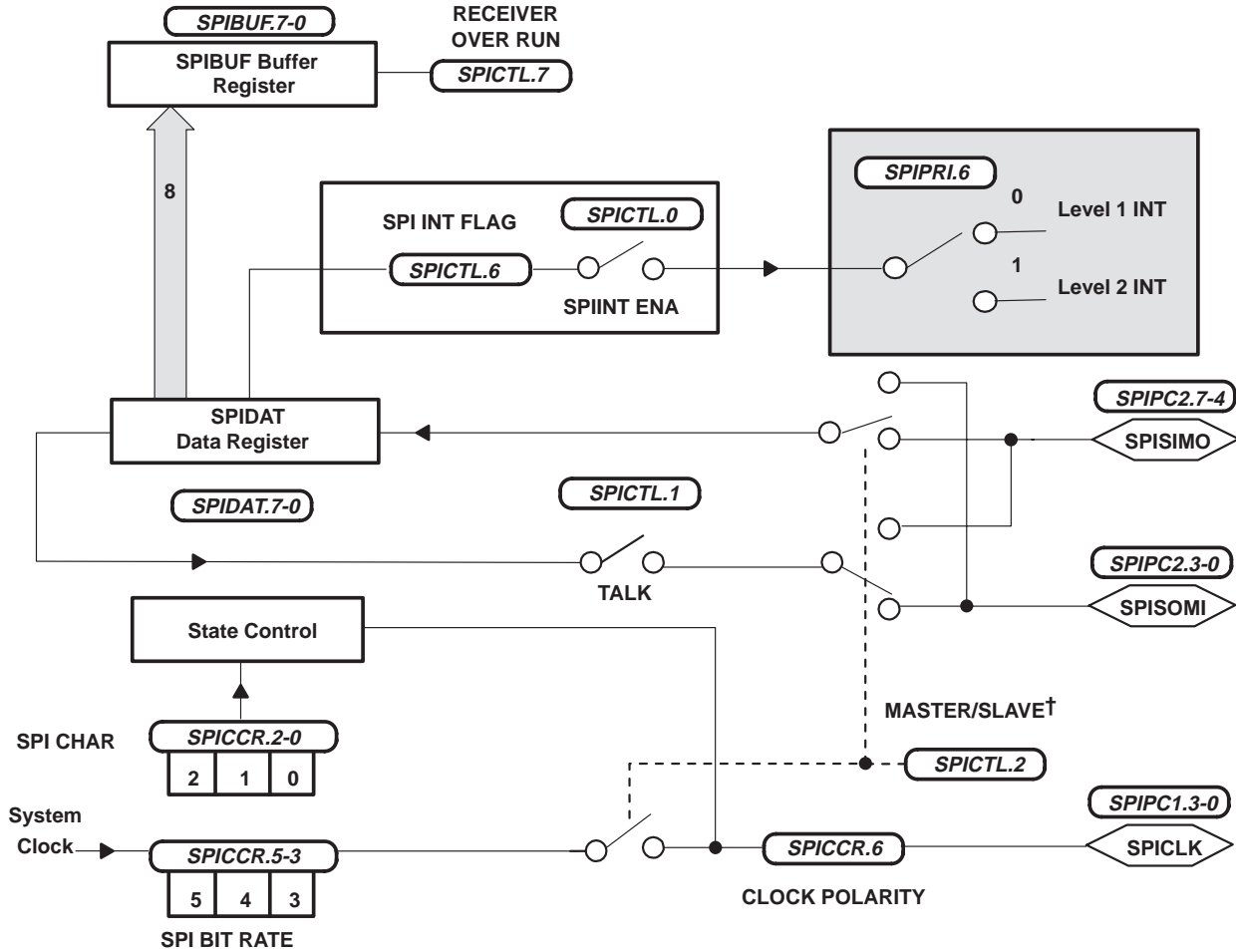
| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REG |
|--------------|------------------|---------------------|------------------|------------------|-----------------|------------------|------------------|------------------|--------|
| P030 | SPI SW RESET | CLOCK POLARITY | SPI BIT RATE2 | SPI BIT RATE1 | SPI BIT RATE0 | SPI CHAR2 | SPI CHAR1 | SPI CHAR0 | SPICCR |
| P031 | RECEIVER OVERRUN | SPI INT FLAG | — | — | — | MASTER/SLAVE | TALK | SPI INT ENA | SPICTL |
| P032 to P036 | Reserved | | | | | | | | |
| P037 | RCVD7 | RCVD6 | RCVD5 | RCVD4 | RCVD3 | RCVD2 | RCVD1 | RCVD0 | SPIBUF |
| P038 | RESERVED | | | | | | | | |
| P039 | SDAT7 | SDAT6 | SDAT5 | SDAT4 | SDAT3 | SDAT2 | SDAT1 | SDAT0 | SPIDAT |
| P03A to P03C | Reserved | | | | | | | | |
| P03D | — | — | — | — | SPICLK DATA IN | SPICLK DATA OUT | SPICLK FUNCTION | SPICLK DATA DIR | SPIPC1 |
| P03E | SPISIMO DATA IN | SPISIMO DATA OUT | SPISIMO FUNCTION | SPISIMO DATA DIR | SPISOMI DATA IN | SPISOMI DATA OUT | SPISOMI FUNCTION | SPISOMI DATA DIR | SPIPC2 |
| P03F | SPI STEST | SPI PRIORITY | SPI ESPEN | — | — | — | — | — | SPIPRI |

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serial peripheral interface (continued)

The SPI block diagram is illustrated in Figure 6.



† The block diagram is shown in slave mode.

Figure 6. SPI Block Diagram

programmable acquisition and control timer (PACT) module

Traditionally, timers in microcontrollers provide limited capture and compare functions consuming significant CPU processing power and leading to inaccurate timings due to interrupt latencies. The programmable acquisition and control timer (PACT) acts as a coprocessor combining configurable capture and compare features, within a flexible dual-port RAM, able to run real-time tasks with little or no CPU intervention. The PACT structure allows concatenation of tasks, thus enabling the CPU to perform data manipulation while the PACT module both captures and outputs real-time-related information. Since all the PACT control information is held within the dual-port Ram, the CPU can access these parameters quickly.

To use the PACT, the user must set up three distinct areas of memory. The first is the dual-port RAM, which contains the capture area, the commands, and the timer definitions. The second is the peripheral frame. The third is an area near the end of the program memory which holds the interrupt vectors of PACT.

programmable acquisition and control timer (PACT) module (continued)

The PACT module features include the following:

- Input-capture functions on up to six input pins (CP1 to CP6), depending on the mode selected:
 - Mode A: CP1–2 are dedicated capture, CP3–6 are circular buffer capture, and CP6 is also an event pin.
 - Mode B: CP1–4 are dedicated capture, CP5–6 are circular buffer capture, and CP6 is also an event pin.
- Multiple timer-driven outputs on eight pins (OP1 to OP8)
 - Standard compare command: set or clear an output pin whenever the timer/counter is equal to a certain value
 - Virtual timers: enable variations of the PWM's period and provides periodic interrupts to the processor.
 - Double event-compare command: comparisons of the 8-bit event counter with two event-compare values and the actions that can be performed are based on each value:
 - Event-compare 1 matching the event counter: sets or resets the selected output pin (OP1–OP8), generates interrupt, and generates a 32-bit capture into the circular buffer.
 - Event-compare 2 matching the event counter: sets or resets the selected output pin (OP1–OP8), generates interrupt, generates a 32-bit capture into the circular buffer, and resets the 20-bit default timer.
 - Offset timer definition-time from last event:
 - Generates an interrupt when the maximum event count is reached
 - Stores the 16-bit virtual timer in the circular buffer on each event
 - Stores the 20-bit default timer and 8-bit event counter in the circular buffer when the maximum event count is reached
 - Resets the 20-bit hardware default timer when the maximum event count is reached.
 - Conditional-compare command has a timer-compare value and an event-compare value.
 - Generates an interrupt when the event-compare value equals the event counter and the timer-compare value equals the last defined timer
 - Sets or clears one of the seven output pins (OP1–OP7) when the event compare value equals the event counter and the timer-compare value equals the last defined timer
 - Baud rate timer definition: runs the mini-serial communications port built into the PACT module.
- Configurable timer overflow rates
- One 8-bit event counter driven by CP6
- Up to 20-bit timer capability
- Interaction between event counter and timer activity
- Register-based organization allowing direct access to timer parameters by the CPU
- 18 independent interrupt vectors with two priority levels
- Integrated, configurable watchdog with selectable time-out period

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programmable acquisition and control timer (PACT) module (continued)

- Mini-serial communications interface works as a simplified full duplex universal asynchronous receiver/transmitter (UART) with independent setup of baud rate for receive and transmit lines.

- Asynchronous communications mode

$$\text{Asynchronous Baud} = \frac{1}{(\text{Max Virtual Timer Value}) \times (4) \times (\text{PACT Resolution})} - 2$$

where PACT Resolution = SYSCLK × Prescale Value

PACT block diagram

The PACT module block diagram is illustrated in Figure 7.

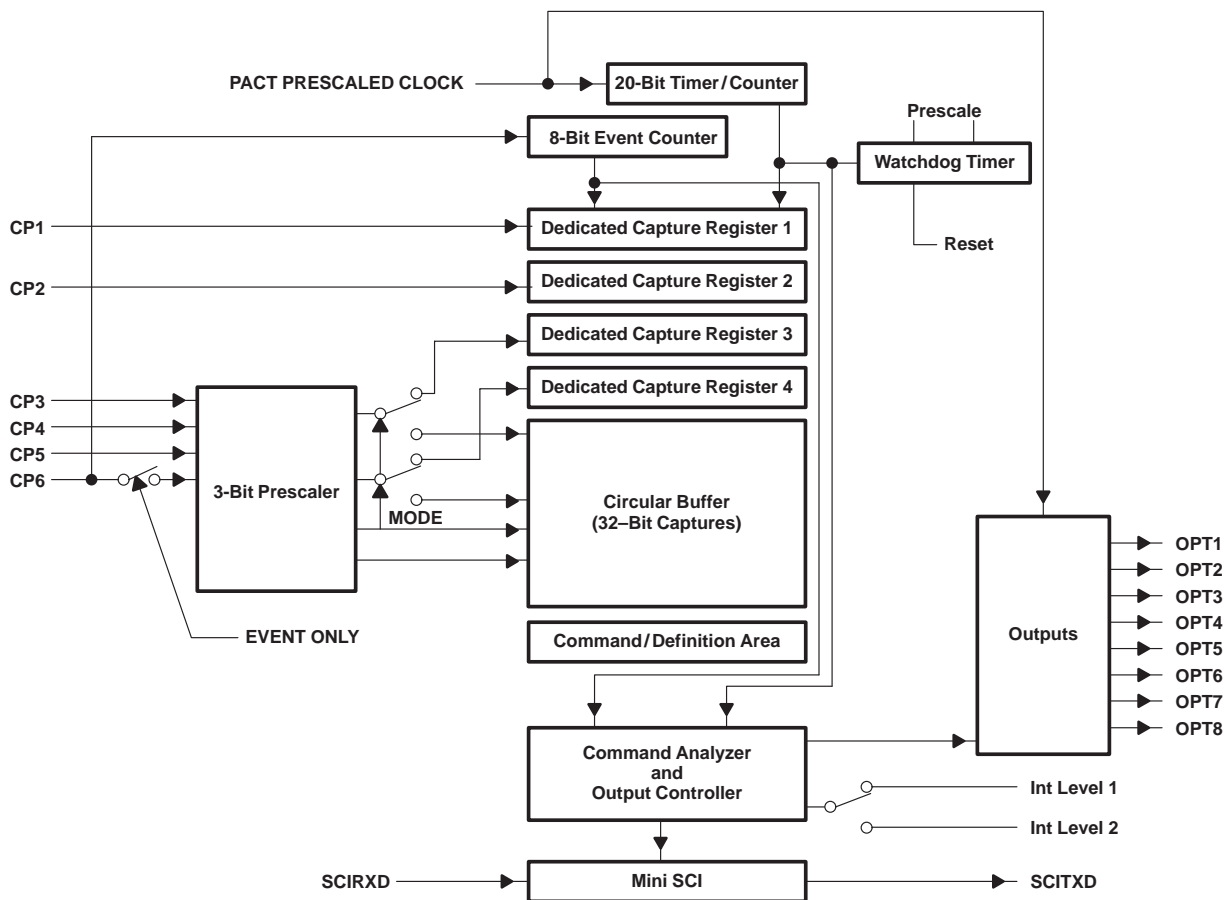


Figure 7. PACT Block diagram

PACT control registers

The PACT module is controlled and accessed through registers in peripheral frame 4. These registers are listed in Table 14. The bits in shaded boxes are privileged mode bits; that is, they can be written to only in the privileged mode.

Table 14. PACT Control Registers

| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REG |
|------|--------------------------|---------------------------|------------------------------|------------------------------|------------------------------|------------------------------|----------------------------------|----------------------------------|---------|
| P040 | DEFTIM OVRFL INT ENA | DEFTIM OVRFL INT FLAG | CMD/DEF AREA ENA | FAST MODE SELECT | PACT PRESCALE SELECT3 | PACT PRESCALE SELECT2 | PACT PRESCALE SELECT1 | PACT PRESCALE SELECT0 | PACTSCR |
| P041 | CMD/DEF AREA INT ENA | — | CMD/DEF AREA START BIT 5 | CMD/DEF AREA START BIT 4 | CMD/DEF AREA START BIT 3 | CMD/DEF AREA START BIT 2 | — | — | CDSTART |
| P042 | — | CMD/DEF AREA END BIT 6 | CMD/DEF AREA END BIT 5 | CMD/DEF AREA END BIT 4 | CMD/DEF AREA END BIT 3 | CMD/DEF AREA END BIT 2 | — | — | CDEND |
| P043 | 1 | 1 | BUFFER POINTER BIT 5 | BUFFER POINTER BIT 4 | BUFFER POINTER BIT 3 | BUFFER POINTER BIT 2 | BUFFER POINTER BIT 1 | — | BUFPTR |
| P044 | Reserved | | | | | | | | |
| P045 | PACT RXRDY | PACT TXRDY | PACT PARITY | PACT FE | PACT SCI RX INT ENA | PACT SCI TX INT ENA | — | PACT SCI SW RESET | SCICTLP |
| P046 | PACT RXDT7 | PACT RXDT6 | PACT RXDT5 | PACT RXDT4 | PACT RXDT3 | PACT RXDT2 | PACT RXDT1 | PACT RXDT0 | RXBUFP |
| P047 | PACT TXDT7 | PACT TXDT6 | PACT TXDT5 | PACT TXDT4 | PACT TXDT3 | PACT TXDT2 | PACT TXDT1 | PACT TXDT0 | TXBUFP |
| P048 | PACT OP8 STATE | PACT OP7 STATE | PACT OP6 STATE | PACT OP5 STATE | PACT OP4 STATE | PACT OP3 STATE | PACT OP2 STATE | PACT OP1 STATE | PSTATE |
| P049 | CMD/DEF INT 7 FLAG | CMD/DEF INT 6 FLAG | CMD/DEF INT 5 FLAG | CMD/DEF INT 4 FLAG | CMD/DEF INT 3 FLAG | CMD/DEF INT 2 FLAG | CMD/DEF INT 1 FLAG | CMD/DEF INT 0 FLAG | CDFLAGS |
| P04A | CP2 INT ENA | CP2 INT FLAG | CP2 CAPT RISING EDGE | CP2 CAPT FALLING EDGE | CP1 INT ENA | CP1 INT FLAG | CP1 CAPT RISING EDGE | CP1 CAPT FALLING EDGE | CPCTL1 |
| P04B | CP4 INT ENA | CP4 INT FLAG | CP4 CAPT RISING EDGE | CP4 CAPT FALLING EDGE | CP3 INT ENA | CP3 INT FLAG | CP3 CAPT RISING EDGE | CP3 CAPT FALLING EDGE | CPCTL2 |
| P04C | CP6 INT ENA | CP6 INT FLAG | CP6 CAPT RISING EDGE | CP6 CAPT FALLING EDGE | CP5 INT ENA | CP5 INT FLAG | CP5 CAPT RISING EDGE | CP5 CAPT FALLING EDGE | CPCTL3 |
| P04D | BUFFER HALF/FULL INT ENA | BUFFER HALF/FULL INT FLAG | INPUT CAPT PRESCALE SELECT 3 | INPUT CAPT PRESCALE SELECT 2 | INPUT CAPT PRESCALE SELECT 1 | CP6 EVENT ONLY | EVENT COUNTER SW RESET | OP/ SET/CLR SELECT | CPPRE |
| P04E | WATCHDOG REST KEY | | | | | | | | WDRST |
| P04F | PACT STEST | PACT SUSPEND | PACT GROUP 1 PRIORITY | PACT GROUP 2 PRIORITY | PACT GROUP 3 PRIORITY | PACT MODE SELECT | PACT WD PRESCALE SELECT 1 | PACT WD PRESCALE SELECT 0 | PACTPRI |

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analog-to-digital converter 1 module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has four multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Ten external pins:
 - Eight analog-input channels (AN0–AN7), any of which can be software-configured as digital inputs (E0–E7) when not needed as analog channels
 - AN1–AN7 also can be configured as positive-input voltage reference.
 - V_{CC3}: ADC1 module high-voltage reference input
 - V_{SS3}: ADC1 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last ADC1 conversion.
- ADC1 operations can be accomplished through either interrupt-driven or polled algorithms.
- Six ADC1 module control registers located in the control-register frame beginning at address 1070h

The ADC1 module control registers are listed in Table 15.

Table 15. ADC1 Module Control Register Memory Map

| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REG |
|--------------------|------------------------------|--------------|------------------|------------------|------------------|------------------|------------------|------------------|--------|
| P070 | CONVERT START | SAMPLE START | REF VOLT SELECT2 | REF VOLT SELECT1 | REF VOLT SELECT0 | AD INPUT SELECT2 | AD INPUT SELECT1 | AD INPUT SELECT0 | ADCTL |
| P071 | — | — | — | — | — | AD READY | AD INT FLAG | AD INT ENA | ADSTAT |
| P072 | A/D Conversion Data Register | | | | | | | | ADDATA |
| P073 to P07C | RESERVED | | | | | | | | |
| P07D | Port E Data Input Register | | | | | | | | ADIN |
| P07E | Port E Input Enable Register | | | | | | | | ADENA |
| P07F | AD STEST | AD PRIORITY | AD ESPEN | — | — | — | — | — | ADPRI |

analog-to-digital converter 1 module (continued)

The ADC1 module block diagram is illustrated in Figure 8.

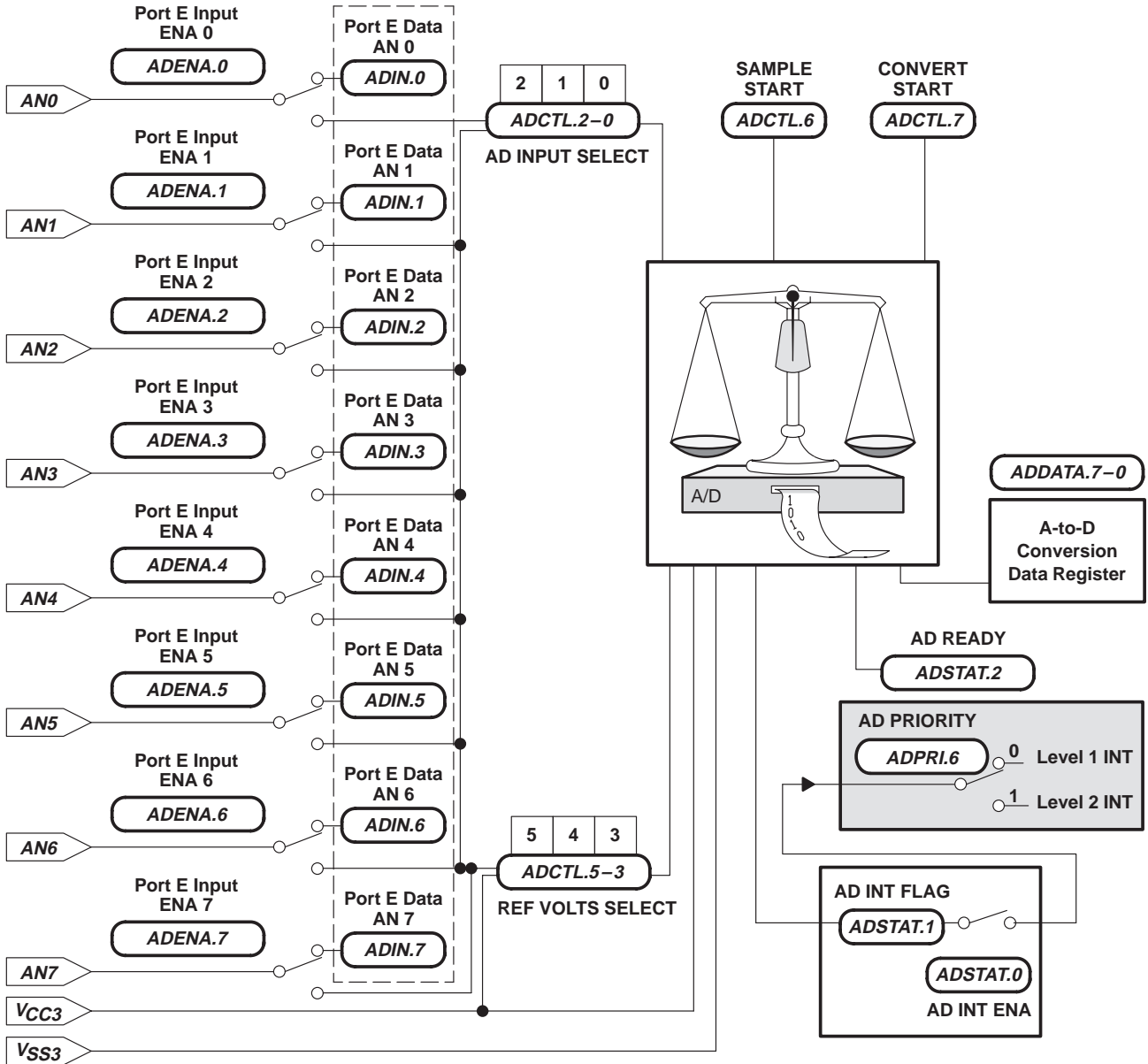


Figure 8. ADC1 Block Diagram

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instruction set overview

Table 16 provides an opcode to instruction cross reference of all 73 instructions and 274 opcodes of the '370Cx36 instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.



Table 16. TMS370 Family Opcode/Instruction Map†

| | | MSN | | | | | | | | | | | | | | | | |
|---|------------------|------------------------|------------------------|------------------------|------------------------|--------------------------|------------------------|------------------------|--------------------------|-------------------------|-------------------------|----------------------------|-----------------------|------------------------------|-----------------------|--------------------|-----------------------------|-------------------------|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | |
| 0 | JMP ra 2/7 | | | | | | | | INCW #ra,Rd 3/11 | MOV Ps,A 2/8 | | | | | MOV A,B 1/9 | MOV A,Rd 2/7 | TRAP 15 1/14 | LDST n 2/6 |
| 1 | JN ra 2/5 | | MOV A,Pd 2/8 | | | | MOV B,Pd 2/8 | | MOV Rs,Pd 3/10 | | MOV Ps,B 2/7 | | | | | MOV B,Rd 2/7 | TRAP 14 1/14 | MOV #ra[SP],A 2/7 |
| 2 | JZ ra 2/5 | MOV Rs,A 2/7 | MOV #n,A 2/6 | MOV Rs,B 2/7 | MOV Rs,B 2/7 | MOV Rs,Rd 3/9 | MOV #n,B 2/6 | MOV B,A 1/8 | MOV #n,Rd 3/8 | | | MOV Ps,Rd 3/10 | DEC A 1/8 | DEC B 1/8 | DEC Rd 2/6 | TRAP 13 1/14 | MOV A,*ra[SP] 2/7 | |
| 3 | JC ra 2/5 | AND Rs,A 2/7 | AND #n,A 2/6 | AND Rs,B 2/7 | AND Rs,B 2/7 | AND Rs,Rd 3/9 | AND #n,B 2/6 | AND B,A 1/8 | AND #n,Rd 3/8 | AND A,Pd 2/9 | AND B,Pd 2/9 | AND #n,Pd 3/10 | INC A 1/8 | INC B 1/8 | INC Rd 2/6 | TRAP 12 1/14 | CMP *n[SP],A 2/8 | |
| 4 | JP ra 2/5 | OR Rs,A 2/7 | OR #n,A 2/6 | OR Rs,B 2/7 | OR Rs,B 2/7 | OR Rs,Rd 3/9 | OR #n,B 2/6 | OR B,A 1/8 | OR #n,Rd 3/8 | OR A,Pd 2/9 | OR B,Pd 2/9 | OR #n,Pd 3/10 | INV A 1/8 | INV B 1/8 | INV Rd 2/6 | TRAP 11 1/14 | extend inst.2 opcodes | |
| 5 | JPZ ra 2/5 | XOR Rs,A 2/7 | XOR #n,A 2/6 | XOR Rs,B 2/7 | XOR Rs,B 2/7 | XOR Rs,Rd 3/9 | XOR #n,B 2/6 | XOR B,A 1/8 | XOR #n,Rd 3/8 | XOR A,Pd 2/9 | XOR B,Pd 2/9 | XOR #n,Pd 3/10 | CLR A 1/8 | CLR B 1/8 | CLR Rn 2/6 | TRAP 10 1/14 | | |
| 6 | JNZ ra 2/5 | BTJO Rs,A,ra 3/9 | BTJO #n,A,ra 3/8 | BTJO Rs,B,ra 3/9 | BTJO Rs,B,ra 3/9 | BTJO Rs,Rd,ra 4/11 | BTJO #n,B,ra 3/8 | BTJO B,A,ra 2/10 | BTJO #n,Rd,ra 4/10 | BTJO A,Pd,ra 3/11 | BTJO B,Pd,ra 3/10 | BTJO #n,Pd,ra 4/11 | XCHB A 1/10 | XCHB A / TST B 1/10 | XCHB Rn 2/8 | TRAP 9 1/14 | IDLE 1/6 | |
| 7 | JNC ra 2/5 | BTJZ Rs,A,ra 3/9 | BTJZ #n,A,ra 3/8 | BTJZ Rs,B,ra 3/9 | BTJZ Rs,B,ra 3/9 | BTJZ Rs,Rd,ra 4/11 | BTJZ #n,B,ra 3/8 | BTJZ B,A,ra 2/10 | BTJZ #n,Rd,ra 4/10 | BTJZ A,Pd,ra 3/10 | BTJZ B,Pd,ra 3/10 | BTJZ #n,Pd,ra 4/11 | SWAP A 1/11 | SWAP B 1/11 | SWAP Rn 2/9 | TRAP 8 1/14 | MOV #n,Pd 3/10 | |
| 8 | JV ra 2/5 | ADD Rs,A 2/7 | ADD #n,A 2/6 | ADD Rs,B 2/7 | ADD Rs,B 2/7 | ADD Rs,Rd 3/9 | ADD #n,B 2/6 | ADD B,A 1/8 | ADD #n,Rd 3/8 | MOVW #16,Rd 4/13 | MOVW Rs,Rd 3/12 | MOVW #16[B],Rpd 4/15 | PUSH A 1/9 | PUSH B 1/9 | PUSH Rd 2/7 | TRAP 7 1/14 | SETC 1/7 | |
| 9 | JL ra 2/5 | ADC Rs,A 2/7 | ADC #n,A 2/6 | ADC Rs,B 2/7 | ADC Rs,B 2/7 | ADC Rs,Rd 3/9 | ADC #n,B 2/6 | ADC B,A 1/8 | ADC #n,Rd 3/8 | JMPL lab 3/9 | JMPL *Rp 2/8 | JMPL *lab[B] 3/11 | POP A 1/9 | POP B 1/9 | POP Rd 2/7 | TRAP 6 1/14 | RTS 1/9 | |
| A | JLE ra 2/5 | SUB Rs,A 2/7 | SUB #n,A 2/6 | SUB Rs,B 2/7 | SUB Rs,B 2/7 | SUB Rs,Rd 3/9 | SUB #n,B 2/6 | SUB B,A 1/8 | SUB #n,Rd 3/8 | MOV &lab,A 3/10 | MOV *Rp,A 2/9 | MOV *lab[B],A 3/12 | DJNZ A,#ra 2/10 | DJNZ B,#ra 2/10 | DJNZ Rd,#ra 3/8 | TRAP 5 1/14 | RTI 1/12 | |
| B | JHS ra 2/5 | SBB Rs,A 2/7 | SBB #n,A 2/6 | SBB Rs,B 2/7 | SBB Rs,B 2/7 | SBB Rs,Rd 3/9 | SBB #n,B 2/6 | SBB B,A 1/8 | SBB #n,Rd 3/8 | MOV A, &lab 3/10 | MOV A, *Rp 2/9 | MOV A, *lab[B] 3/12 | COMPL A 1/8 | COMPL B 1/8 | COMPL Rd 2/6 | TRAP 4 1/14 | PUSH ST 1/8 | |

† All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 16. TMS370 Family Opcode/Instruction Map† (Continued)

| | | MSN | | | | | | | | | | | | | | | |
|---|------------------|---------------------|---------------------|---------------------|----------------------|----------------------|--------------------|----------------------|----------------------|------------------------|-------------------------|--------------------------|-----------------|-----------------|-------------------|-------------------|-------------|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| C | JNV ra 2/5 | MPY Rs,A 2/46 | MPY #n,A 2/45 | MPY Rs,B 2/46 | MPY Rs,Rd 3/48 | MPY #n,B 2/45 | MPY B,A 1/47 | MPY #n,Rs 3/47 | BR lab 3/9 | BR *Rp 2/8 | BR *lab[B] 3/11 | RR A 1/8 | RR B 1/8 | RR Rd 2/6 | TRAP 3 1/14 | POP ST 1/8 | |
| | D | JGE ra 2/5 | CMP Rs,A 2/7 | CMP #n,A 2/6 | CMP Rs,B 2/7 | CMP Rs,Rd 3/9 | CMP #n,B 2/6 | CMP B,A 1/8 | CMP #n,Rd 3/8 | CMP & lab,A 3/11 | CMP *Rp,A 2/10 | CMP *lab[B],A 3/13 | RRC A 1/8 | RRC B 1/8 | RRC Rd 2/6 | TRAP 2 1/14 | LDSP 1/7 |
| E | JG ra 2/5 | DAC Rs,A 2/9 | DAC #n,A 2/8 | DAC Rs,B 2/9 | DAC Rs,Rd 3/11 | DAC #n,B 2/8 | DAC B,A 1/10 | DAC #n,Rd 3/10 | CALL lab 3/13 | CALL *Rp 2/12 | CALL *lab[B] 3/15 | RL A 1/8 | RL B 1/8 | RL Rd 2/6 | TRAP 1 1/14 | STSP 1/8 | |
| | F | JLO ra 2/5 | DSB Rs,A 2/9 | DSB #n,A 2/8 | DSB Rs,B 2/9 | DSB Rs,Rd 3/11 | DSB #n,B 2/8 | DSB B,A 1/10 | DSB #n,Rd 3/10 | CALLR lab 3/15 | CALLR *Rp 2/14 | CALLR *lab[B] 3/17 | RLC A 1/8 | RLC B 1/8 | RLC Rd 2/6 | TRAP 0 1/14 | NOP 1/7 |

Second byte of two-byte instructions (F4xx):

| | | | |
|----|---|-------------------------|------------------------|
| F4 | 8 | MOVW *n[Rn] 4/15 | DIV Rn,A 3/14-63 |
| F4 | 9 | JMPL *n[Rn] 4/16 | |
| F4 | A | MOV *n[Rn],A 4/17 | |
| F4 | B | MOV A,*n[Rn] 4/16 | |
| F4 | C | BR *n[Rn] 4/16 | |
| F4 | D | CMP *n[Rn],A 4/18 | |
| F4 | E | CALL *n[Rn] 4/20 | |
| F4 | F | CALLR *n[Rn] 4/22 | |

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = Register file
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

† All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C-compiler, a linker, CDT and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
 - Generate assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (Compact Development Tool) PACT real-time in-circuit emulation
 - Base (Part Number EDSCDT37P – for PC, requires cable)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCC36)
 - EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Includes compatibility to upload/download program and data memory
 - Execute programs and software routines
 - Includes 1 024-sample trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 44-pin PLCC (Part No. TMDS3780512A)
 - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment

HP700 is a trademark of Hewlett Packard, Incorporated.
Sun-3 and Sun-4 are trademarks of Sun Microsystems, Incorporated.



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device numbering conventions

Figure 9 illustrates the numbering and symbol nomenclature for the TMS370Cx36 family.

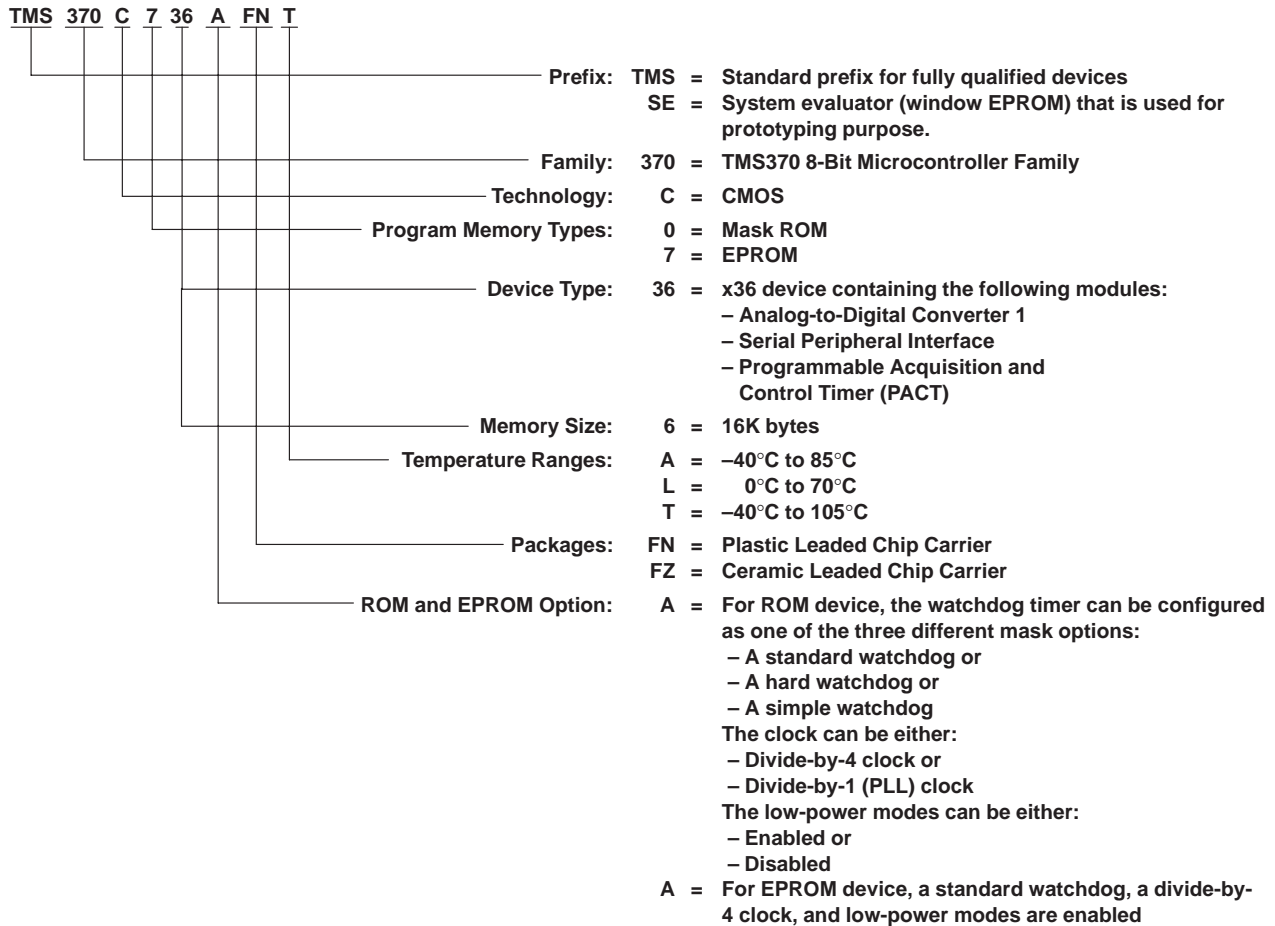


Figure 9. TMS370Cx36 Family Nomenclature

device part numbers

Table 17 provides a listing of all the 'x36 devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 17. Device Part Numbers

| DEVICE PART NUMBERS FOR 44 PINS (LCC) |
|--|
| TMS370C036AFNA |
| TMS370C036AFNL |
| TMS370C036AFNT |
| TMS370C736AFNT |
| SE370C736AFZT† |

† System evaluators are for use in prototype environment, and their reliability has not been characterized.

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new code release form

Figure 10 shows a sample of the new code release form.

NEW CODE RELEASE FORM
TEXAS INSTRUMENTS
TMS370 MICROCONTROLLER PRODUCTS

DATE: _____

To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:

1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media)
2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.

Company Name: _____
 Street Address: _____
 Street Address: _____
 City: _____ State _____ Zip _____

Contact Mr./Ms.: _____
 Phone: (_____) _____ Ext.: _____

Customer Purchase Order Number: _____
 Customer Print Number *Yes: _____ # _____
 No: _____ (Std. spec to be followed)

*If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.

TMS370 Device: _____
 TI Customer ROM Number: _____
 (provided by Texas Instruments)

OSCILLATOR FREQUENCY

| | MIN | TYP | MAX |
|---|-------|-------|-------|
| <input type="checkbox"/> External Drive (CLKIN) | _____ | _____ | _____ |
| <input type="checkbox"/> Crystal | _____ | _____ | _____ |
| <input type="checkbox"/> Ceramic Resonator | _____ | _____ | _____ |

Supply Voltage MIN: _____ MAX: _____
 (std range: 4.5V to 5.5V)

TEMPERATURE RANGE

'L': 0° to 70°C (standard)
 'A': -40° to 85°C
 'T': -40° to 105°C

SYMBOLIZATION

TI standard symbolization
 TI standard w/customer part number
 Customer symbolization
 (per attached spec, subject to approval)

NON-STANDARD SPECIFICATIONS:
 ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.

RELEASE AUTHORIZATION:
 This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cyclotime commences when this document is signed off and the verification code is approved by the customer.

1. Customer: _____ Date: _____

2. TI: Field Sales: _____
 Marketing: _____
 Prod. Eng.: _____
 Proto. Release: _____

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

| | | |
|-----------------------------------|---|--|
| Low Power Modes | Watchdog counter | Clock Type |
| <input type="checkbox"/> Enabled | <input type="checkbox"/> Standard | <input type="checkbox"/> Standard (/4) |
| <input type="checkbox"/> Disabled | <input type="checkbox"/> Hard Enabled | <input type="checkbox"/> PLL (/1) |
| | <input type="checkbox"/> Simple Counter | |

NOTE:
 Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE

| | |
|---|--|
| <input type="checkbox"/> 'N' 28-pin PDIP | <input type="checkbox"/> "FN" 44-pin PLCC |
| <input type="checkbox"/> "FN" 28-pin PLCC | <input type="checkbox"/> "FN" 68-pin PLCC |
| <input type="checkbox"/> "N" 40-pin PDIP | <input type="checkbox"/> "NM" 64-pin PSDIP |
| <input type="checkbox"/> "NJ" 40-pin PSDIP (formerly known as N2) | |

BUS EXPANSION

YES NO

Figure 10. Sample New Code Release Form



POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Table 18. Peripheral File Frame Compilation

Table 18 is a collection of all the peripheral file frames used in the 'Cx36 (provided for a quick reference).

| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REG |
|---|--|----------------|---------------|-------------------|---------------|----------------|---------------|-------------------|--------|
| System Configuration Registers | | | | | | | | | |
| P010 | COLD START | OSC POWER | PF AUTO WAIT | OSC FLT FLAG | MC PIN WPO | MC PIN DATA | — | μP/μC MODE | SCCR0 |
| P011 | — | — | — | AUTO WAIT DISABLE | — | MEMORY DISABLE | — | — | SCCR1 |
| P012 | HALT/STANDBY | PWRDWN/IDLE | — | BUS STEST | CPU STEST | — | INT1 NMI | PRIVILEGE DISABLE | SCCR2 |
| P013 to P016 | Reserved | | | | | | | | |
| P017 | INT1 FLAG | INT1 PIN DATA | — | — | — | INT1 POLARITY | INT1 PRIORITY | INT1 ENABLE | INT1 |
| P018 to P019 | Reserved | | | | | | | | |
| P01A | BUSY | — | — | — | — | AP | W1W0 | EXE | DEECTL |
| P01B | Reserved | | | | | | | | |
| P01C | BUSY | VPPS | — | — | — | — | W0 | EXE | EPCTLL |
| P01D to P01F | Reserved | | | | | | | | |
| Digital Port Control Registers | | | | | | | | | |
| P020 | Reserved | | | | | | | | APORT1 |
| P021 | Port A Control Register 2 (must be 0) | | | | | | | | APORT2 |
| P022 | Port A Data | | | | | | | | ADATA |
| P023 | Port A Direction | | | | | | | | ADIR |
| P024 to P02B | Reserved | | | | | | | | |
| P02C | Port D Control Register 1 (must be 0) | | | | | — | — | — | DPORT1 |
| P02D | Port D Control Register 2 (must be 0) [†] | | | | | — | — | — | DPORT2 |
| P02E | Port D Data | | | | | — | — | — | DDATA |
| P02F | Port D Direction | | | | | — | — | — | DDIR |
| SPI Module Control Register Memory Map | | | | | | | | | |
| P030 | SPI SW RESET | CLOCK POLARITY | SPI BIT RATE2 | SPI BIT RATE1 | SPI BIT RATE0 | SPI CHAR2 | SPI CHAR1 | SPI CHAR0 | SPICCR |
| P031 | RECEIVER OVERRUN | SPI INT FLAG | — | — | — | MASTER/SLAVE | TALK | SPI INT ENA | SPICTL |
| P032 to P036 | Reserved | | | | | | | | |
| P037 | RCVD7 | RCVD6 | RCVD5 | RCVD4 | RCVD3 | RCVD2 | RCVD1 | RCVD0 | SPIBUF |
| P038 | Reserved | | | | | | | | |
| P039 | SDAT7 | SDAT6 | SDAT5 | SDAT4 | SDAT3 | SDAT2 | SDAT1 | SDAT0 | SPIDAT |

[†] To configure D3 as SYSCLK, set port D register 2 = 08h.

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Table 18. Peripheral File Frame Compilation (Continued)

| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REG |
|---|--------------------------|---------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|---------|
| SPI Module Control Register Memory Map (Continued) | | | | | | | | | |
| P03A to P03C | Reserved | | | | | | | | |
| P03D | — | — | — | — | SPICLK DATA IN | SPICLK DATA OUT | SPICLK FUNCTION | SPICLK DATA DIR | SPIPC1 |
| P03E | SPISIMO DATA IN | SPISIMO DATA OUT | SPISIMO FUNCTION | SPISIMO DATA DIR | SPISOMI DATA IN | SPISOMI DATA OUT | SPISOMI FUNCTION | SPISOMI DATA DIR | SPIPC2 |
| P03F | SPI STEST | SPI PRIORITY | SPI ESPEN | — | — | — | — | — | SPIPRI |
| PACT Module Register Memory Map | | | | | | | | | |
| P040 | DEFTIM OVRFL INT ENA | DEFTIM OVRFL INT FLAG | CMD/DEF AREA ENA | FAST MODE SELECT | PACT PRESCALE SELECT3 | PACT PRESCALE SELECT2 | PACT PRESCALE SELECT1 | PACT PRESCALE SELECT0 | PACTSCR |
| P041 | CMD/DEF AREA INT ENA | — | CMD/DEF AREA START BIT 5 | CMD/DEF AREA START BIT 4 | CMD/DEF AREA START BIT 3 | CMD/DEF AREA START BIT 2 | — | — | CDSTART |
| P042 | — | CMD/DEF AREA END BIT 6 | CMD/DEF AREA END BIT 5 | CMD/DEF AREA END BIT 4 | CMD/DEF AREA END BIT 3 | CMD/DEF AREA END BIT 2 | — | — | CDEND |
| P043 | 1 | 1 | BUFFER POINTER BIT 5 | BUFFER POINTER BIT 4 | BUFFER POINTER BIT 3 | BUFFER POINTER BIT 2 | BUFFER POINTER BIT 1 | — | BUFPTR |
| P044 | Reserved | | | | | | | | |
| P045 | PACT RXRDY | PACT TXRDY | PACT PARITY | PACT FE | PACT SCI RX INT ENA | PACT SCI TX INT ENA | — | PACT SCI SW RESET | SCICTLP |
| P046 | PACT RXDT7 | PACT RXDT6 | PACT RXDT5 | PACT RXDT4 | PACT RXDT3 | PACT RXDT2 | PACT RXDT1 | PACT RXDT0 | RXBUFP |
| P047 | PACT TXDT7 | PACT TXDT6 | PACT TXDT5 | PACT TXDT4 | PACT TXDT3 | PACT TXDT2 | PACT TXDT1 | PACT TXDT0 | TXBUFP |
| P048 | PACT OP8 STATE | PACT OP7 STATE | PACT OP6 STATE | PACT OP5 STATE | PACT OP4 STATE | PACT OP3 STATE | PACT OP2 STATE | PACT OP1 STATE | PSTATE |
| P049 | CMD/DEF INT 7 FLAG | CMD/DEF INT 6 FLAG | CMD/DEF INT 5 FLAG | CMD/DEF INT 4 FLAG | CMD/DEF INT 3 FLAG | CMD/DEF INT 2 FLAG | CMD/DEF INT 1 FLAG | CMD/DEF INT 0 FLAG | CDFLAGS |
| P04A | CP2 INT ENA | CP2 INT FLAG | CP2 CAPT RISING EDGE | CP2 CAPT FALLING EDGE | CP1 INT ENA | CP1 INT FLAG | CP1 CAPT RISING EDGE | CP1 CAPT FALLING EDGE | CPCTL1 |
| P04B | CP4 INT ENA | CP4 INT FLAG | CP4 CAPT RISING EDGE | CP4 CAPT FALLING EDGE | CP3 INT ENA | CP3 INT FLAG | CP3 CAPT RISING EDGE | CP3 CAPT FALLING EDGE | CPCTL2 |
| P04C | CP6 INT ENA | CP6 INT FLAG | CP6 CAPT RISING EDGE | CP6 CAPT FALLING EDGE | CP5 INT ENA | CP5 INT FLAG | CP5 CAPT RISING EDGE | CP5 CAPT FALLING EDGE | CPCTL3 |
| P04D | BUFFER HALF/FULL INT ENA | BUFFER HALF/FULL INT FLAG | INPUT CAPT PRESCALE SELECT 3 | INPUT CAPT PRESCALE SELECT 2 | INPUT CAPT PRESCALE SELECT 1 | CP6 EVENT ONLY | EVENT COUNTER SW RESET | OP/ SET/CLR SELECT | CPPRE |



Table 18. Peripheral File Frame Compilation (Continued)

| PF | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REG |
|--------------------|--|------------------------|--------------------------------------|--------------------------------------|--------------------------------------|---------------------------------|--|--|---------|
| | PACT Module Register Memory Map (Continued) | | | | | | | | |
| P04E | WATCHDOG RESET KEY | | | | | | | | WDRST |
| P04F | PACT STEST | PACT SUSPEND | PACT GROUP 1 PRIORITY | PACT GROUP 2 PRIORITY | PACT GROUP 3 PRIORITY | PACT MODE SELECT | PACT WD PRESCALE SELECT 1 | PACT WD PRESCALE SELECT 0 | PACTPRI |
| | ADC1 Module Control Register Memory Map | | | | | | | | |
| P070 | CONVERT START | SAMPLE START | REF VOLT SELECT2 | REF VOLT SELECT1 | REF VOLT SELECT0 | AD INPUT SELECT2 | AD INPUT SELECT1 | AD INPUT SELECT0 | ADCTL |
| P071 | — | — | — | — | — | AD READY | AD INT FLAG | AD INT ENA | ADSTAT |
| P072 | ADC1 Conversion Data Register | | | | | | | | ADDATA |
| P073 to P07C | RESERVED | | | | | | | | |
| P07D | Port E Data Input Register | | | | | | | | ADIN |
| P07E | Port E Input Enable Register | | | | | | | | ADENA |
| P07F | AD STEST | AD PRIORITY | AD ESPEN | — | — | — | — | — | ADPRI |

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | | |
|--|-------|----------------|
| Supply voltage range, V_{CC1} (see Note 4) | | -0.6 V to 7 V |
| Input voltage range, All pins except MC | | -0.6 V to 7 V |
| MC | | -0.6 V to 14 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | | ± 20 mA |
| Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 5) | | ± 10 mA |
| Maximum I_{CC} current | | 170 mA |
| Maximum I_{SS} current | | -170 mA |
| Continuous power dissipation | | 1 W |
| Operating free-air temperature, T_A : L version | | 0°C to 70°C |
| A version | | -40°C to 85°C |
| T version | | -40°C to 105°C |
| Storage temperature range, T_{stg} | | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 4. Unless otherwise noted, all voltage values are with respect to V_{SS1} .
 5. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT | |
|--------------|--|--|---------------|-----------|------|----|
| V_{CC1} | Supply voltage (see Note 4) | 4.5 | 5 | 5.5 | V | |
| | RAM data-retention supply voltage (see Note 6) | 3 | | 5.5 | V | |
| V_{CCSTBY} | Standby RAM supply voltage | 4.5 | 5 | 5.5 | V | |
| | Standby RAM data retention supply voltage (see Note 6) | 3 | | 5.5 | V | |
| V_{CC3} | Analog supply voltage (see Note 4) | 4.5 | 5 | 5.5 | V | |
| V_{SS3} | Analog supply ground | -0.3 | 0 | 0.3 | V | |
| V_{IL} | Low-level input voltage | All pins except MC | | V_{SS1} | 0.8 | V |
| | | MC, normal operation | | V_{SS1} | 0.3 | V |
| V_{IH} | High-level input voltage | All pins except MC, XTAL2/CLKIN, and RESET | 2 | V_{CC1} | | V |
| | | XTAL2/CLKIN | $0.8 V_{CC1}$ | V_{CC1} | | |
| | | RESET | $0.7 V_{CC1}$ | V_{CC1} | | |
| V_{MC} | MC (mode control) voltage | EEPROM write protect override (WPO) | 11.7 | 12 | 13 | V |
| | | EEPROM programming voltage (V_{PP}) | 13 | 13.2 | 13.5 | |
| | | Microcomputer | V_{SS1} | | 0.3 | |
| T_A | Operating free-air temperature | L version | 0 | 70 | | °C |
| | | A version | -40 | 85 | | |
| | | T version | -40 | 105 | | |

- NOTES: 4. Unless otherwise noted, all voltage values are with respect to V_{SS1} .
 6. RESET must be externally activated when V_{CC1} or SYSCLOCK is not within the recommended operating range.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

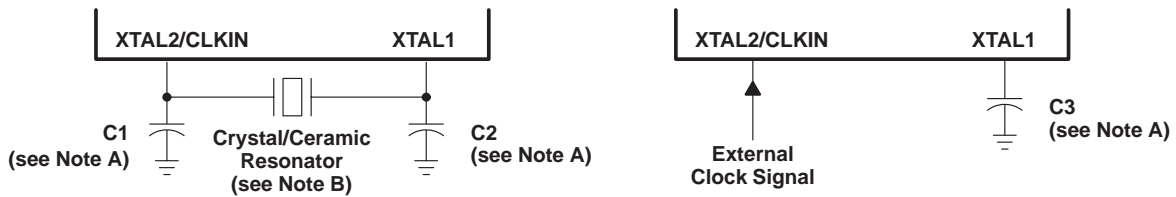
| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|---------------------------------|--|------|-----|----------------------|------|
| V _{OL} | Low-level output voltage | All outputs | I _{OL} = 1.4 mA | | | 0.4 | V |
| V _{OH} | High-level output voltage | All outputs except PACT outputs | I _{OH} = -50 μA | | | 0.9 V _{CC1} | V |
| | | PACT outputs | I _{OH} = -50 μA | | | 0.7 V _{CC1} | |
| | | All outputs | I _{OH} = -2 mA | | | 2.4 | |
| I _I | Input current | MC | 0 V ≤ V _I ≤ 0.3 V | | | 10 | μA |
| | | | 0.3 V < V _I < V _{CC1} - 0.3 V | | | 50 | μA |
| | | | V _{CC1} - 0.3 < V _I < V _{CC1} + 0.3 V | | | 10 | μA |
| | | | V _{CC1} + 0.3 V < V _I < 13 V | | | 650 | μA |
| | | I/O pins | 0 V < V _I < V _{CC1} | | | ± 10 | μA |
| I _{OL} | Low-level output current | All outputs | V _{OL} = 0.4 V | 1.4 | | | mA |
| I _{OH} | High-level output current | All outputs | V _{OH} = 0.9 V _{CC1} | - 50 | | | μA |
| | | | V _{OH} = 2.4 V | - 2 | | | mA |
| I _{CC1} | Supply current (operating mode) OSC POWER bit = 0 | | See Notes 7 and 8 SYSCLK = 5 MHz | | 36 | 45 | mA |
| | Supply current (STANDBY mode) OSC POWER bit = 0 | | See Notes 7 and 8 SYSCLK = 5 MHz | | 7 | 12 | mA |
| | Supply current (HALT mode) | | See Notes 7 and 8 XTAL2/CLKIN < 0.2 V | | 5 | 30 | μA |
| I _{CCSTBY} | Standby RAM supply current (operating mode OSC POWER bit = 0) | | SYSCLK = 5 MHz V _{CCSTBY} = 4.5 V | | 1 | 1.5 | mA |

- NOTES: 7. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} - 0.2V.
8. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).



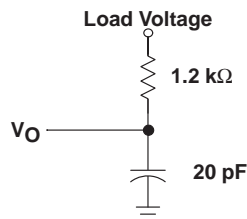
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NOTES: A. The values of C1 and C2 are typically 15 pF and C3 value is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.
B. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.

Figure 11. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4\text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4\text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 12. Typical Output Load Circuit (See Note A)

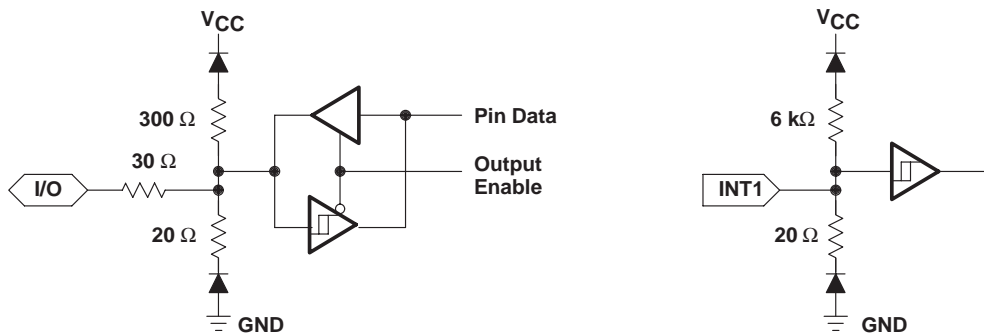


Figure 13. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

| | | | |
|----|-------------|------|---------|
| AR | Array | SC | SYSCLK |
| B | Byte | SIMO | SPISIMO |
| CI | XTAL2/CLKIN | SOMI | SPISOMI |
| M | Master mode | SPC | SPICLK |
| S | Slave mode | | |

Lowercase subscripts and their meanings are:

| | | | |
|---|---------------------|----|------------------------|
| c | cycle time (period) | su | setup time |
| d | delay time | v | valid time |
| f | fall time | w | pulse duration (width) |
| r | rise time | | |

The following additional letters are used with these meanings:

| | |
|---|-------|
| H | High |
| L | Low |
| V | Valid |

All timings are measured between high and low measurement points as indicated in Figure 14 and Figure 15.



Figure 14. XTAL2/CLKIN Measurement Points



Figure 15. General Measurement Points

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external clocking requirements for clock divided by 4 (see Note 9 and Figure 16)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1 | $t_w(C)$ Pulse duration, XTAL2/CLKIN (see Note 10) | 20 | | ns |
| 2 | $t_r(C)$ Rise time, XTAL2/CLKIN | | 30 | ns |
| 3 | $t_f(C)$ Fall time, XTAL2/CLKIN | | 30 | ns |
| 4 | $t_d(CIH-SCL)$ Delay time, XTAL2/CLKIN rise to SYSCLK fall | | 100 | ns |
| | CLKIN Crystal operating frequency | 2 | 20 | MHz |
| | SYSCLK Internal system clock operating frequency [†] | 0.5 | 5 | MHz |

[†] SYSCLK = CLKIN/4

NOTES: 9. For V_{IL} and V_{IH} , refer to recommended operating conditions.

10. This pulse may be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

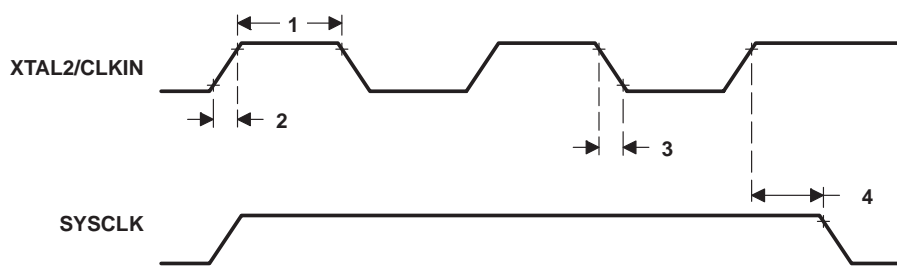


Figure 16. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL) (see Note 9 and Figure 17)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1 | $t_w(C)$ Pulse duration, XTAL2/CLKIN (see Note 10) | 20 | | ns |
| 2 | $t_r(C)$ Rise time, XTAL2/CLKIN | | 30 | ns |
| 3 | $t_f(C)$ Fall time, XTAL2/CLKIN | | 30 | ns |
| 4 | $t_d(CIH-SCH)$ Delay time, XTAL2/CLKIN rise to SYSCLK rise | | 100 | ns |
| | CLKIN Crystal operating frequency | 2 | 5 | MHz |
| | SYSCLK Internal system clock operating frequency [‡] | 2 | 5 | MHz |

[‡] SYSCLK = CLKIN/1

NOTES: 9. For V_{IL} and V_{IH} , refer to recommended operating conditions.

10. This pulse can be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

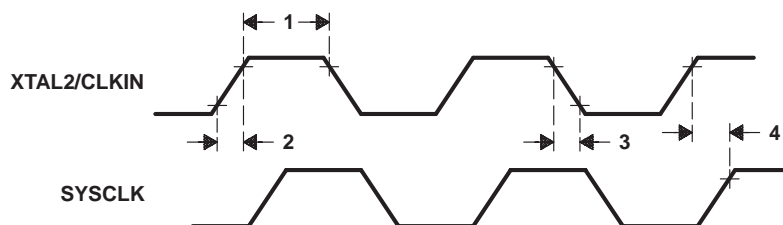


Figure 17. External Clock Timing for Divide-by-1

switching characteristics and timing requirements (see Note 11 and Figure 18)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|---|-------------|----------------|----------------|------|
| 5 | t_c Cycle time, SYSCLK (system clock) | Divide by 4 | 200 | 2000 | ns |
| | | Divide by 1 | 200 | 500 | |
| 6 | $t_w(SCL)$ Pulse duration, SYSCLK low | | $0.5 t_c - 20$ | $0.5 t_c$ | ns |
| 7 | $t_w(SCH)$ Pulse duration, SYSCLK high | | $0.5 t_c$ | $0.5 t_c + 20$ | ns |

NOTE 11: t_c = system clock cycle time = 1/SYSCLK

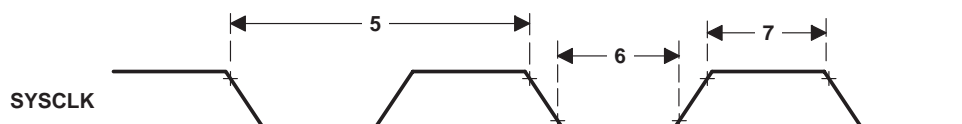


Figure 18. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 19)

| | MIN | TYP | MAX | UNIT |
|-----------------|-----|-----|-----|------|
| t_r Rise time | | 30 | | ns |
| t_f Fall time | | 30 | | ns |

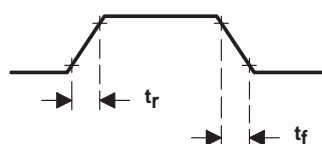


Figure 19. Signal Switching Timing

recommended EEPROM timing requirements for programming

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_w(PGM)B$ Pulse duration, programming signal to ensure valid data is stored (byte mode) | 10 | | ms |
| $t_w(PGM)AR$ Pulse duration, programming signal to ensure valid data is stored (array mode) | 20 | | ms |

recommended EPROM operating conditions for programming

| | MIN | TYP | MAX | UNIT |
|--|-------------|------|------|------|
| V_{CC} Supply voltage | 4.75 | 5.5 | 6 | V |
| V_{PP} Supply voltage at MC pin | 13 | 13.2 | 13.5 | V |
| I_{PP} Supply current at MC pin during programming ($V_{PP} = 13 V$) | | 30 | 50 | mA |
| SYSCLK System clock | Divide by 4 | 0.5 | 5 | MHz |
| | Divide by 1 | 2 | 5 | |

recommended EPROM timing requirements for programming

| | MIN | TYP | MAX | UNIT |
|--|------|------|-----|------|
| $t_w(EPGM)$ Pulse duration, programming signal (see Note 12) | 0.40 | 0.50 | 3 | ms |

NOTE 12: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

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SPI master mode external timing characteristics and requirements (see Note 11 and Figure 20)

| NO. | | MIN | MAX | UNIT |
|-----|---|-------------------------|---------------------------|------|
| 38 | $t_c(\text{SPC})_M$ Cycle time, SPICLK | $2t_c$ | $256t_c$ | ns |
| 39 | $t_w(\text{SPCL})_M$ Pulse duration, SPICLK low | $t_c - 45$ | $0.5t_c(\text{SPC}) + 45$ | ns |
| 40 | $t_w(\text{SPCH})_M$ Pulse duration, SPICLK high | $t_c - 55$ | $0.5t_c(\text{SPC}) + 45$ | ns |
| 41 | $t_d(\text{SPCL-SIMOV})_M$ Delay time, SPISIMO valid after SPICLK low (polarity = 1) | - 65 | 50 | ns |
| 42 | $t_v(\text{SPCH-SIMO})_M$ Valid time, SPISIMO data valid after SPICLK high (polarity = 1) | $t_w(\text{SPCH}) - 50$ | | ns |
| 43 | $t_{su}(\text{SOMI-SPCH})_M$ Setup time, SPISOMI to SPICLK high (polarity = 1) | $0.25 t_c + 150$ | | ns |
| 44 | $t_v(\text{SPCH-SOMI})_M$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1) | 0 | | ns |

NOTE 11: t_c = system clock cycle time = 1/SYSCLK

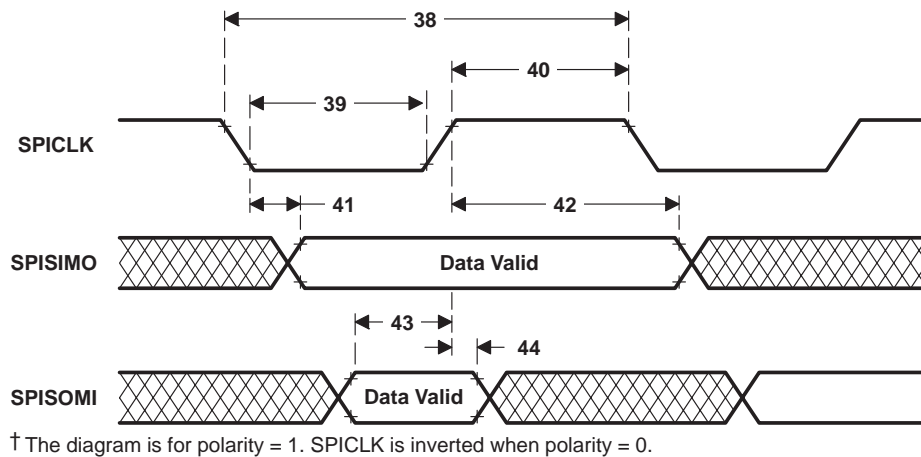
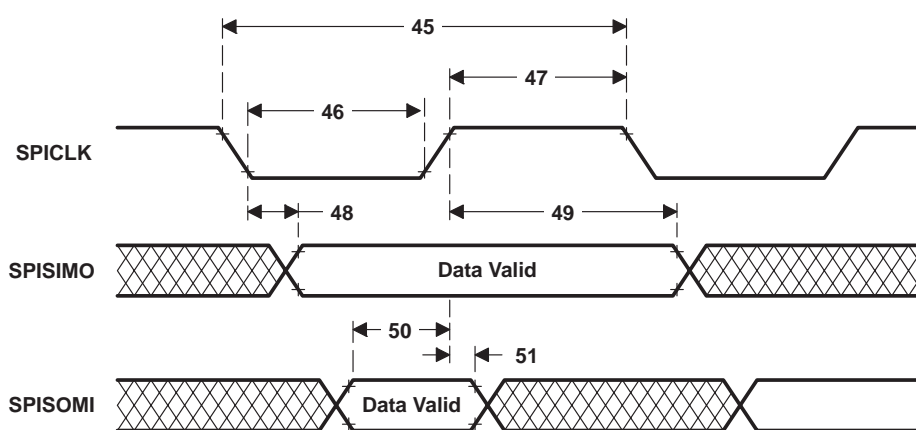


Figure 20. SPI Master External Timing†

SPI slave mode external timing characteristics and requirements (see Note 11 and Figure 21)

| NO. | | MIN | MAX | UNIT |
|-----|---|--------------|---------------------|------|
| 45 | $t_{c(SPC)S}$ Cycle time, SPICLK | $8t_c$ | | ns |
| 46 | $t_w(SPCL)S$ Pulse duration, SPICLK low | $4t_c - 45$ | $0.5t_c(SPC)S + 45$ | ns |
| 47 | $t_w(SPCH)S$ Pulse duration, SPICLK high | $4t_c - 45$ | $0.5t_c(SPC)S + 45$ | ns |
| 48 | $t_d(SPCL-SOMIV)S$ Delay time, SPISOMI valid after SPICLK low (polarity = 1) | | $3.25t_c + 130$ | ns |
| 49 | $t_v(SPCH-SOMI)S$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1) | $t_w(SPCH)S$ | | ns |
| 50 | $t_{su}(SIMO-SPCH)S$ Setup time, SPISIMO to SPICLK high (polarity = 1) | 0 | | ns |
| 51 | $t_v(SPCH-SIMO)S$ Valid time, SPISIMO data after SPICLK high (polarity = 1) | $3t_c + 100$ | | ns |

NOTE 11: t_c = system clock cycle time = 1/SYSCLK



† The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 21. SPI Slave External Timing†

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ADC1 converter

The ADC1 converter has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|-------------------------------------|---------------|-----------|-----------------|------|
| V_{CC3} Analog supply voltage | 4.5 | 5 | 5.5 | V |
| | $V_{CC1}-0.3$ | | $V_{CC1}+0.3$ | |
| V_{SS3} Analog ground | $V_{SS1}-0.3$ | | $V_{SS1}+0.3$ | V |
| V_{ref} Non- V_{CC3} reference† | 2.5 | V_{CC3} | $V_{CC3} + 0.1$ | V |
| Analog input for conversion | V_{SS3} | | V_{ref} | V |

† V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

| PARAMETER | | MIN | MAX | UNIT |
|---|-------------------------------------|-----|-----------|-----------|
| Absolute accuracy‡ | $V_{CC3} = 5.5 V$ $V_{ref} = 5.1 V$ | | ± 1.5 | LSB |
| Differential/integral linearity error‡§ | $V_{CC3} = 5.5 V$ $V_{ref} = 5.1 V$ | | ± 0.9 | LSB |
| I_{CC3} Analog supply current | Converting | | 2 | mA |
| | Nonconverting | | 5 | μA |
| I_I Input current, AN0–AN7 | $0 V \leq V_I \leq 5.5 V$ | | 2 | μA |
| I_{ref} Input charge current | | | 1 | mA |
| Z_{ref} Source impedance of V_{ref} | $SYSCLK \leq 3 MHz$ | | 24 | $k\Omega$ |
| | $3 MHz < SYSCLK \leq 5 MHz$ | | 10 | $k\Omega$ |

‡ Absolute resolution = 20 mV. At $V_{ref} = 5 V$, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

§ Excluding quantization error of 1/2 LSB



ADC1 converter (continued)

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements (see Figure 22)

| | MIN | MAX | UNIT |
|--|---------|-----|------------------------------|
| $t_{su(S)}$ Setup time, analog to sample command | 0 | | ns |
| $t_{h(AN)}$ Hold time, analog input from start of conversion | $18t_C$ | | ns |
| $t_w(S)$ Pulse duration, sample time per kilo- Ω of source impedance [†] | 1 | | $\mu\text{s}/\text{k}\Omega$ |

[†] The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

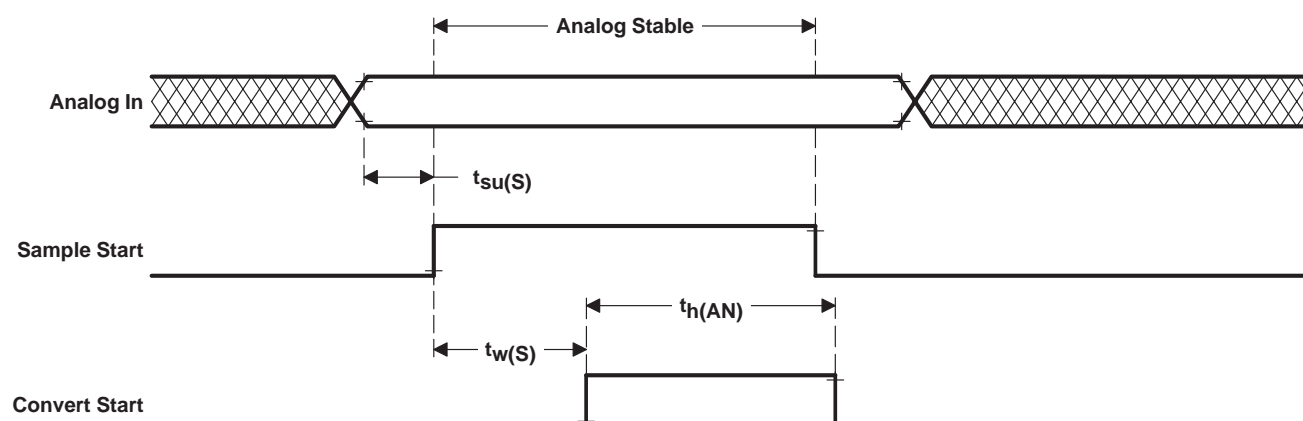


Figure 22. Analog Timing

Table 19 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 19. TMS370Cx36 Family Package Type and Mechanical Cross-Reference

| PKG TYPE (mil pin spacing) | TMS370 GENERIC NAME | PKG TYPE NO. AND MECHANICAL NAME | DEVICE PART NUMBERS |
|-------------------------------------|---------------------------------------|---|--|
| FN – 44 pin (50-mil pin spacing) | PLASTIC LEADED CHIP CARRIER (PLCC) | FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER | TMS370C036AFNA TMS370C036AFNL TMS370C036AFNT TMS370C736AFNT |
| FZ – 44 pin (50-mil pin spacing) | CERAMIC LEADED CHIP CARRIER (CLCC) | FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER | SE370C736AFZT [†] |

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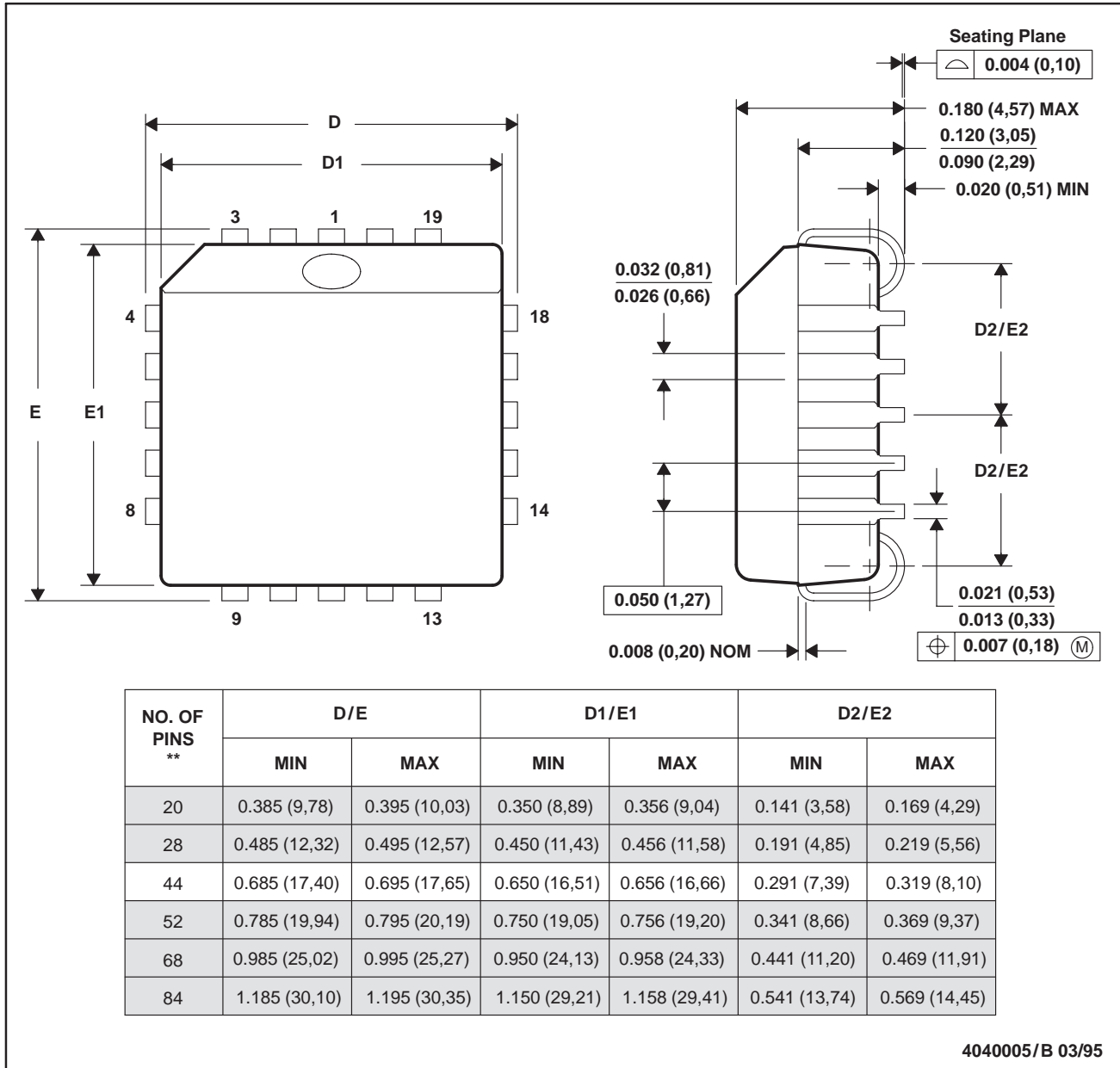
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MECHANICAL DATA

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018



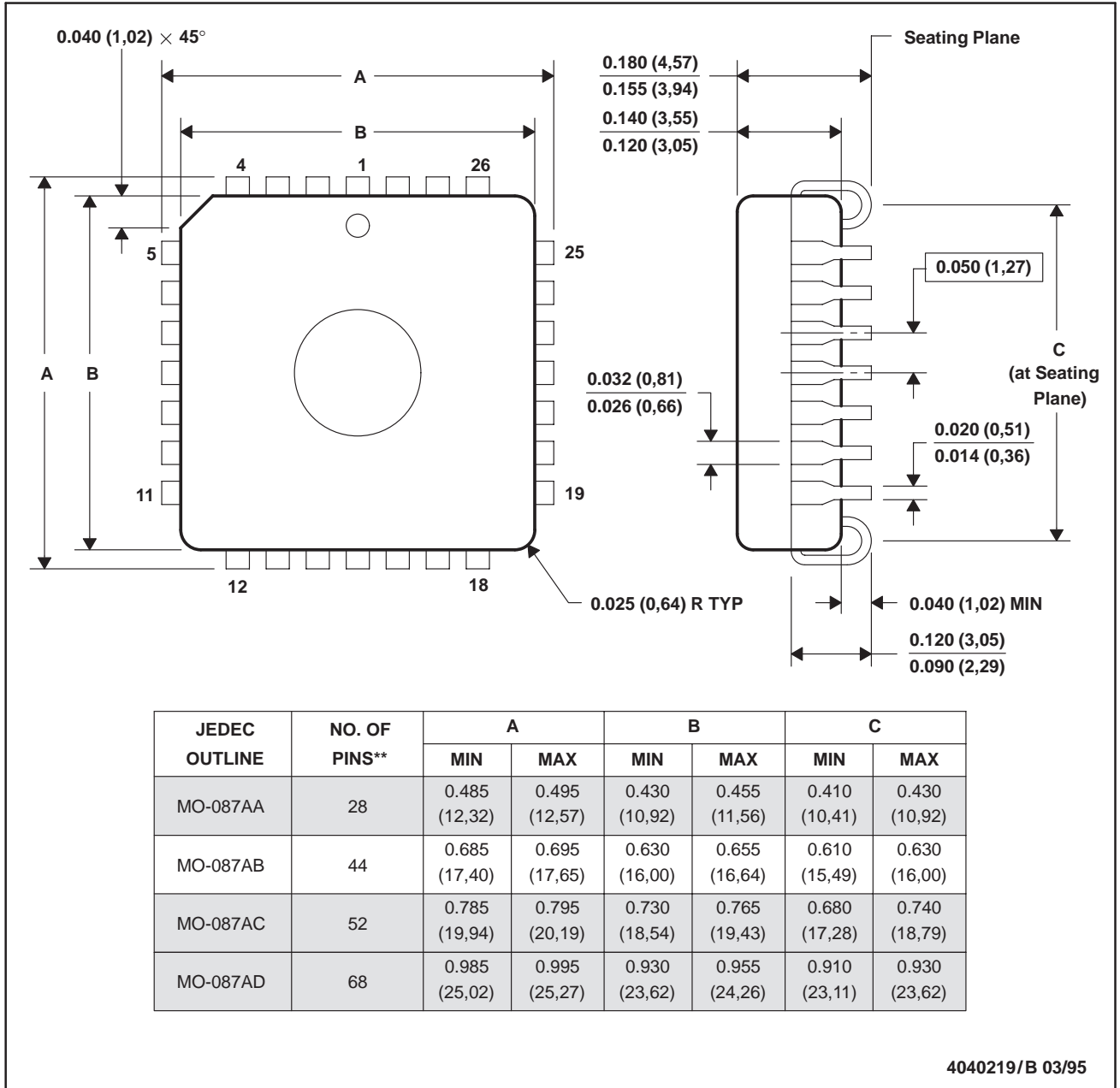
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

MECHANICAL DATA

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.

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