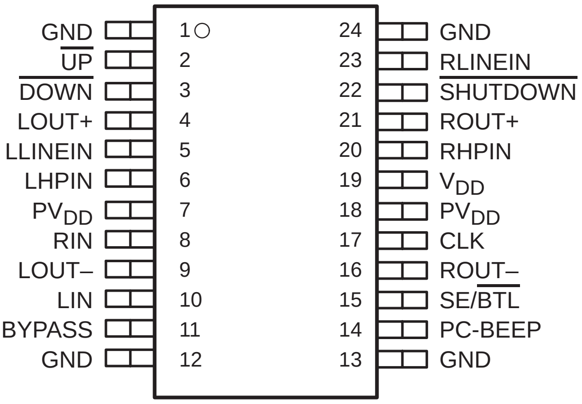
TPA0162
2-W STEREO AUDIO POWER AMPLIFIER WITH DIGITAL VOLUME CONTROL

SLOS249B – JUNE 1999 – REVISED MARCH 2000

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **Digital Volume Control From 20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0162 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0162 has less than 0.22% THD+N across its specified frequency range.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

The overall gain of the amplifier is controlled digitally by the UP and DOWN terminals. At power up, the gain is set at the lowest level, –85 dB. It can then be adjusted to any of 31 discrete steps by pulling the voltage down at the desired pin to logic low. The gain is adjusted in the initial stage of the amplifier as opposed to the power output stage. As a result, the THD changes very little over all volume levels.

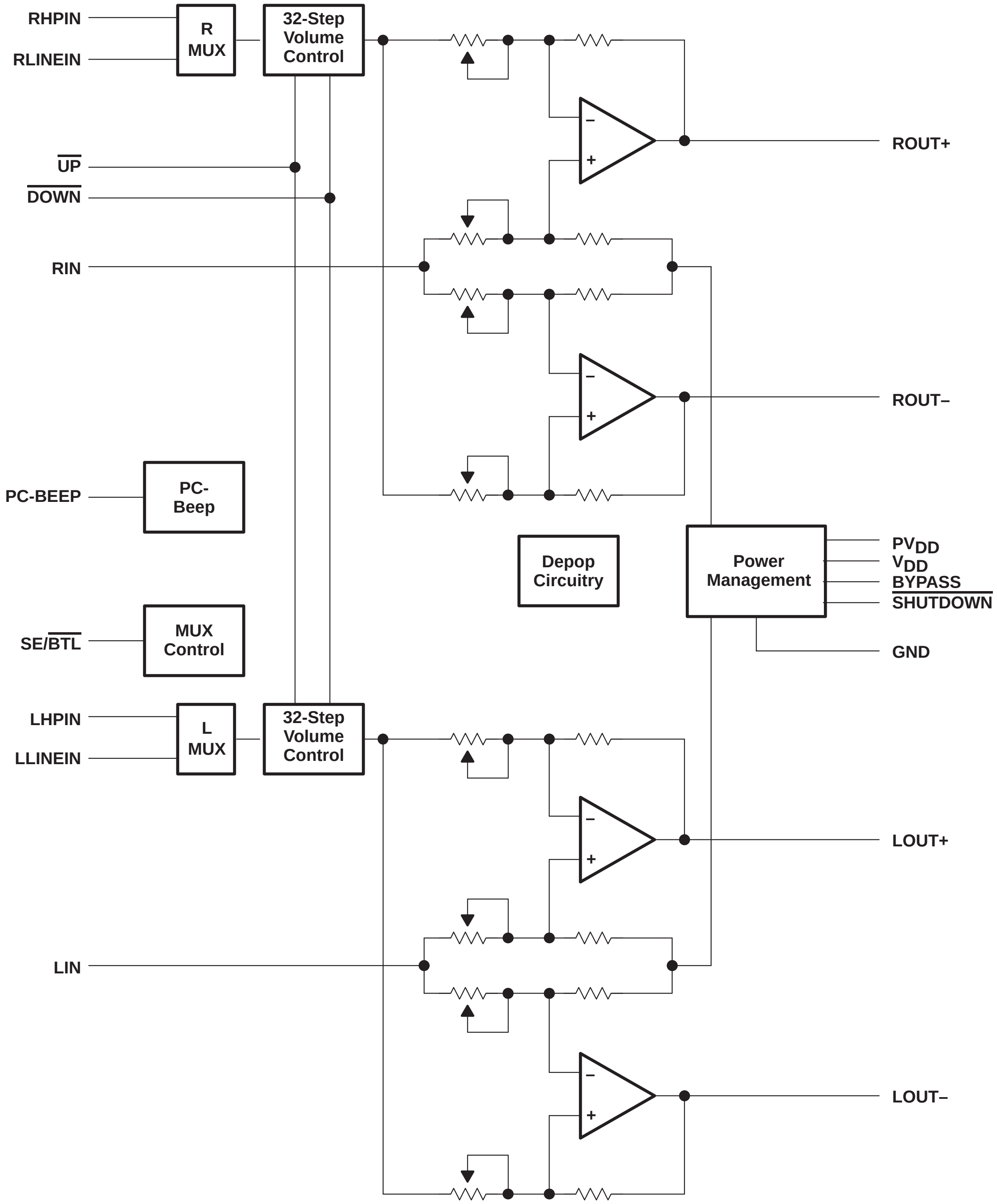
An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0162 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. This effectively reduces the gain by 6 dB.

The TPA0162 consumes only 20 mA of supply current during normal operation. A miserly shutdown mode is included that reduces the supply current to less than 150 µA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0162 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

PowerPAD is a trademark of Texas Instruments Incorporated.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP[†] (PWP)
–40°C to 85°C	TPA0162PWP

[†] The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0162PWPR).

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0162 generates an internal clock. An external clock can override the internal clock input to this terminal.
$\overline{\text{DOWN}}$	3	I	A momentary pulse on this terminal decreases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
GND	1, 12 13, 24		Ground connection for circuitry. Connected to thermal pad
LHPIN	6	I	Left-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left-channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
LOUT–	9	O	Left-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low.
ROUT+	21	O	Right-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
ROUT–	16	O	Right-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
$\overline{\text{UP}}$	2	I	A momentary pulse on this terminal increases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} . . . . 6 V
Input voltage, V_I . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W[‡]	21.8 mW/°C	1.7 W	1.4 W

[‡] Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$	4		V
	$\overline{\text{SHUTDOWN}}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$		3	V
	$\overline{\text{SHUTDOWN}}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	$V_I = 0$, $A_V = 2$			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		67		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		20		mA
		SE mode		10		
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	μA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 2 V/V, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.22%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 μF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	C_B = 0.47 μF, f = 20 Hz to 20 kHz	BTL mode		17		μV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Gain	2
		vs Frequency	3, 5, 7, 9, 11
		vs Output voltage	12
V_n	Output noise voltage	vs Bandwidth	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Bandwidth	20
	Closed loop respone		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_I	Input impedance	vs Gain	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

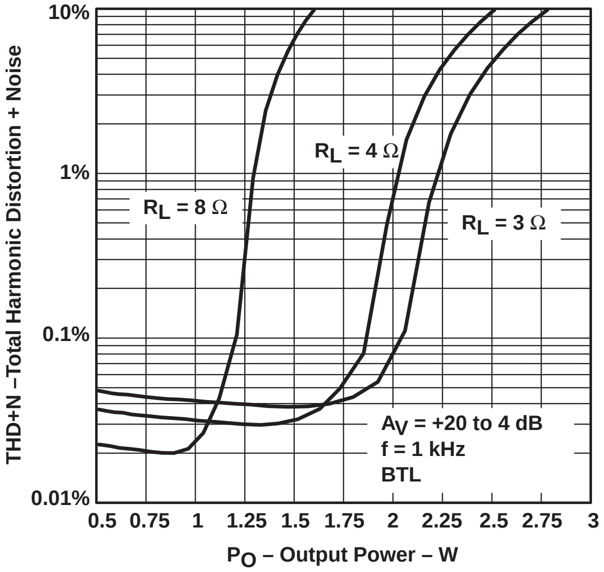


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
VOLTAGE GAIN

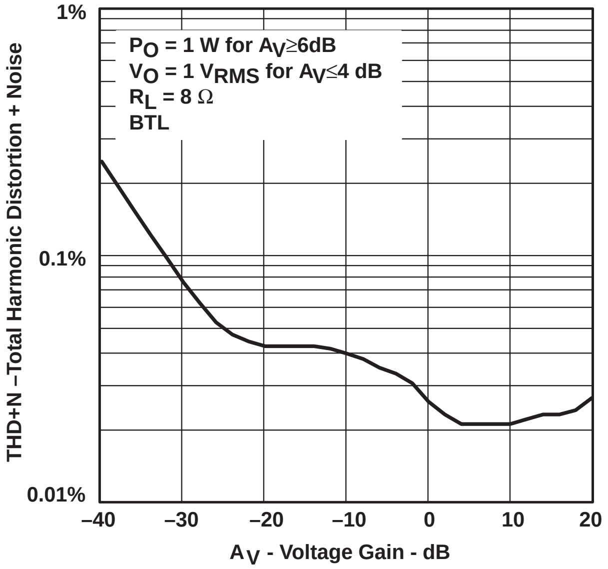


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

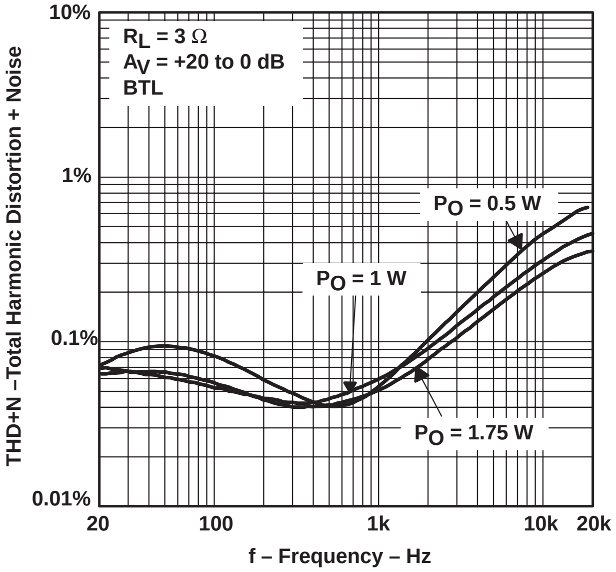


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

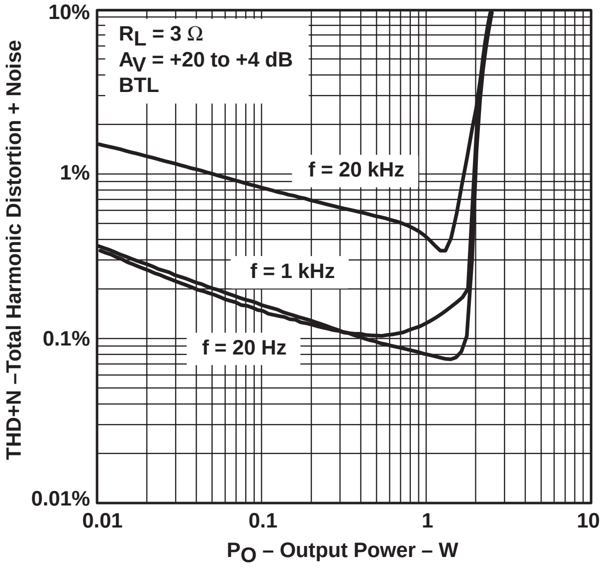


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

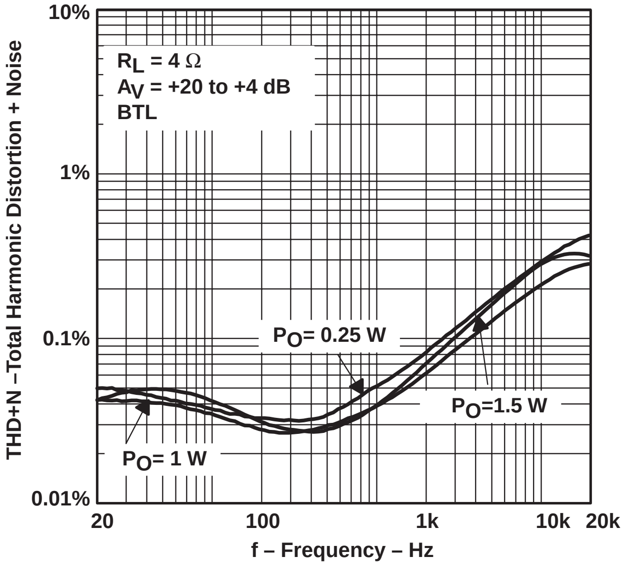


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

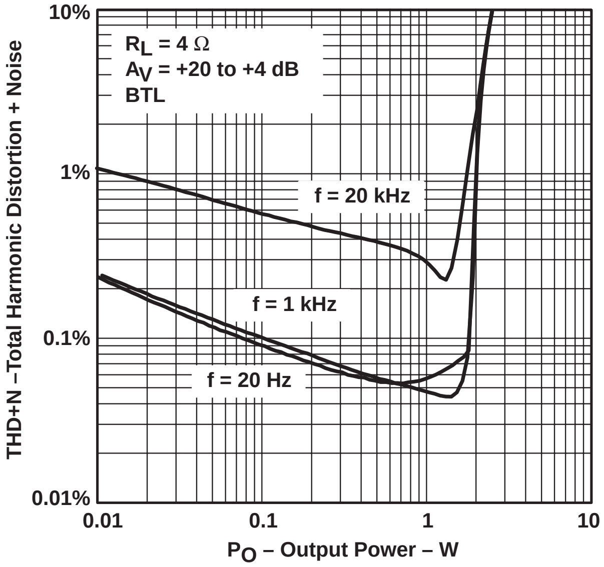


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

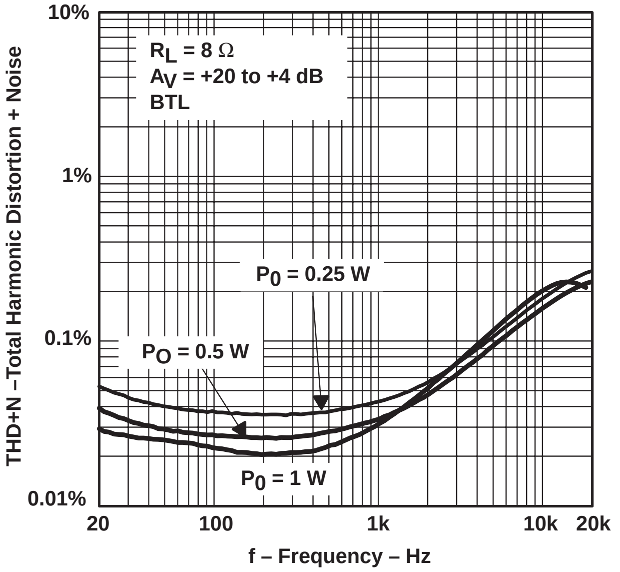


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

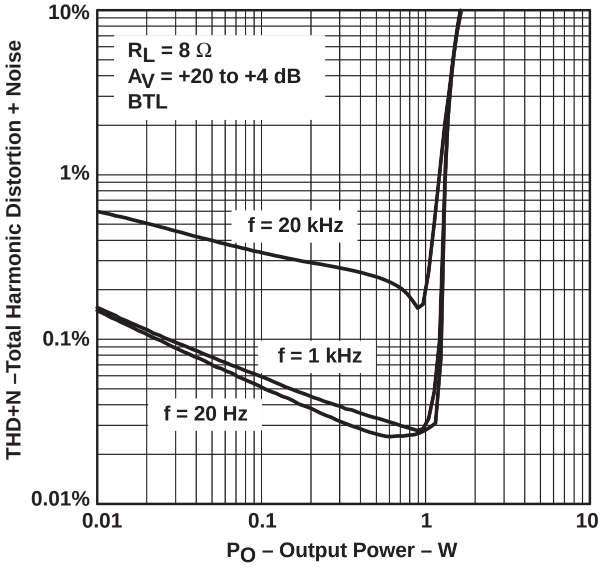


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

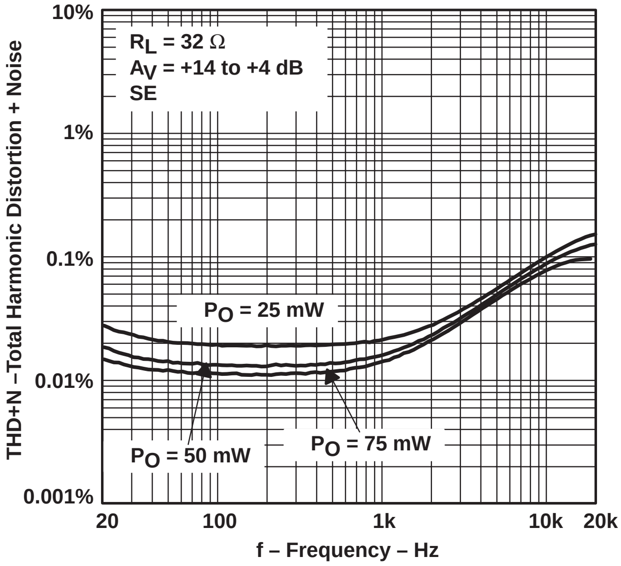


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

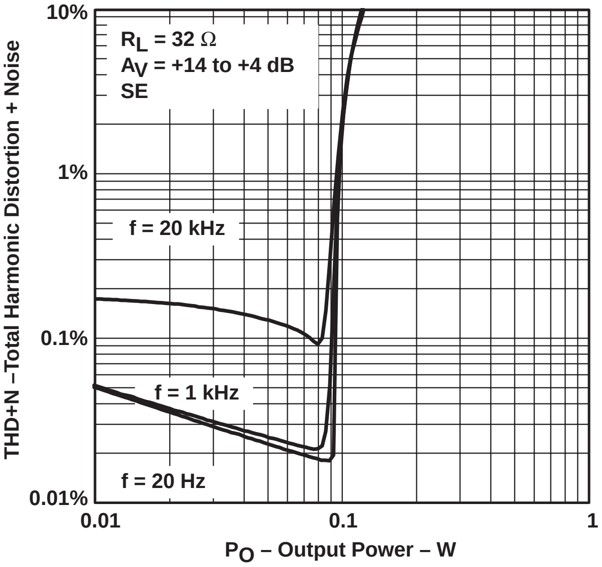


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

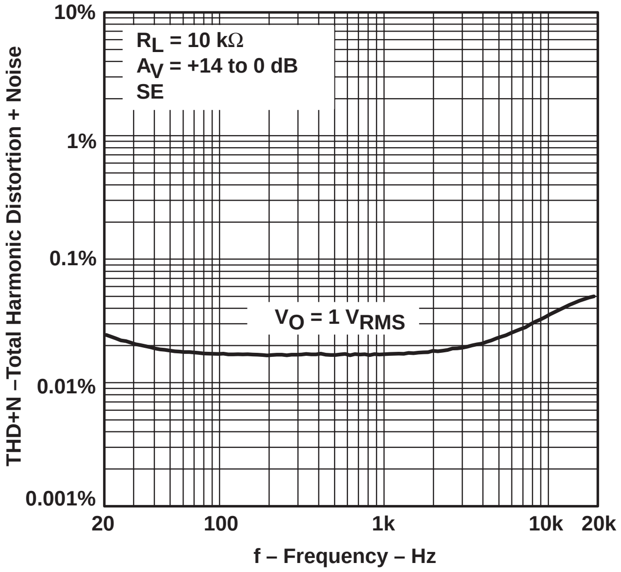


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT VOLTAGE

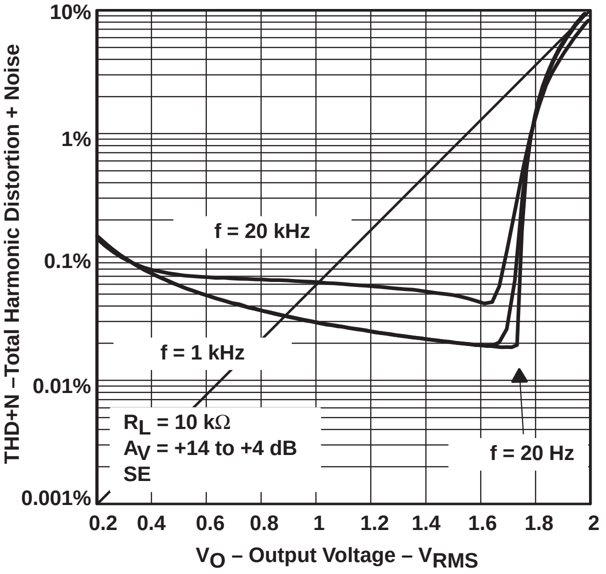


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE vs BANDWIDTH

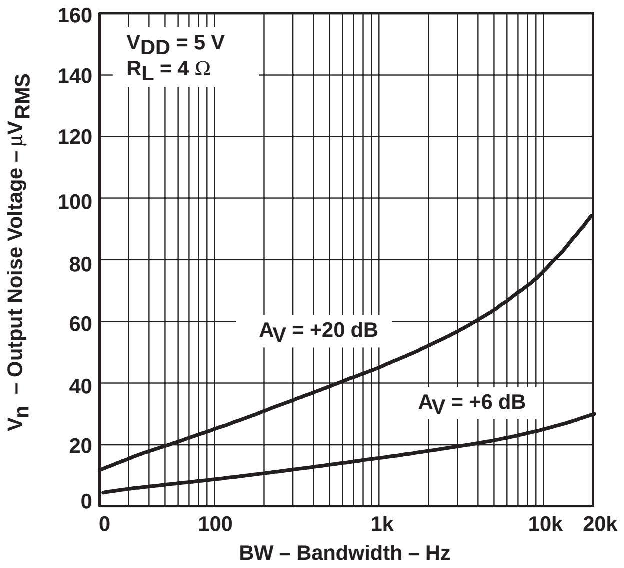


Figure 13

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

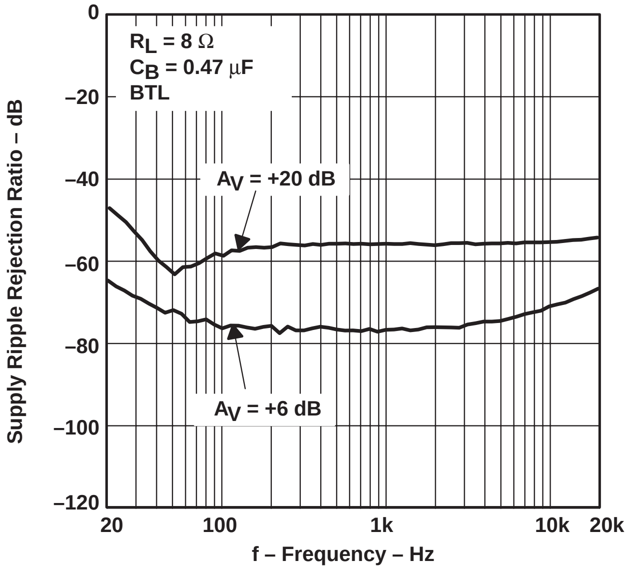


Figure 14

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

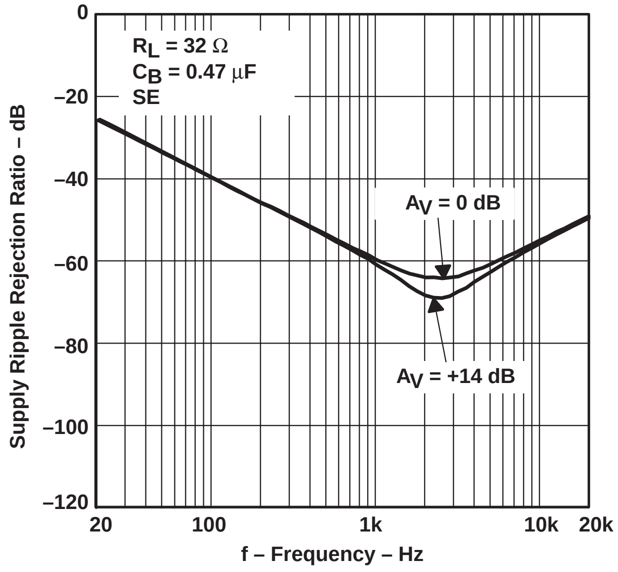


Figure 15

CROSSTALK vs FREQUENCY

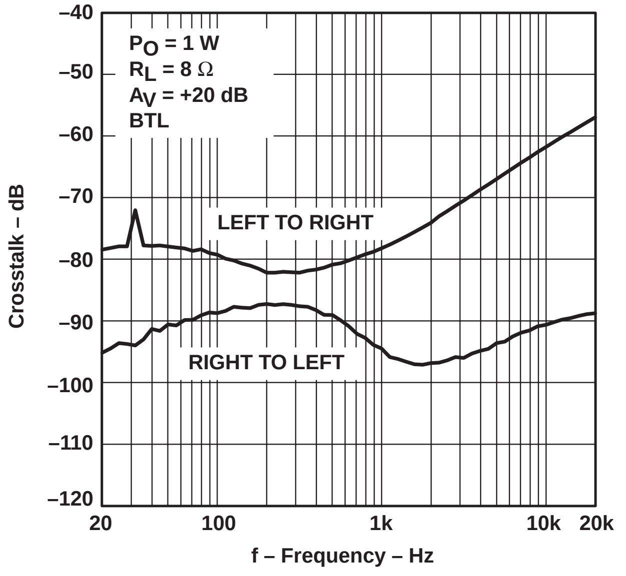
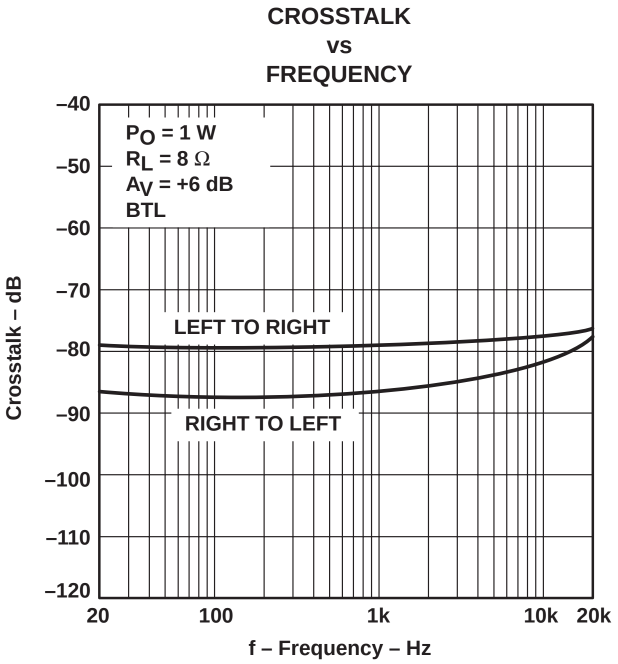


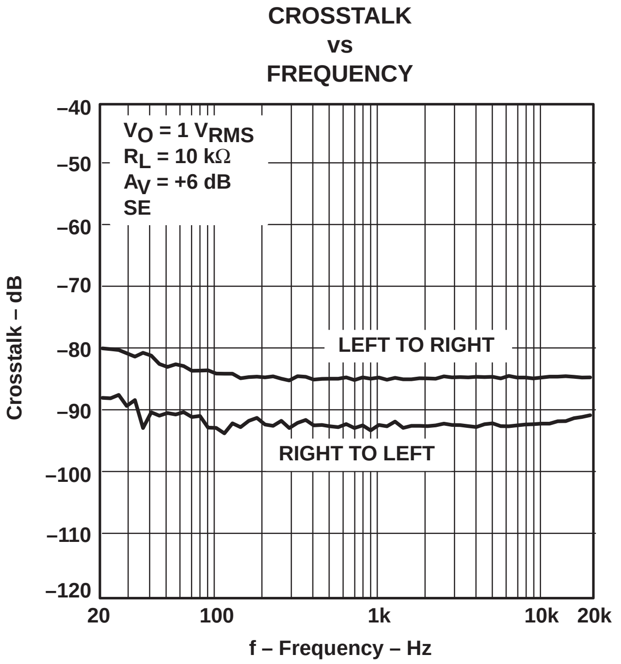
Figure 16

TYPICAL CHARACTERISTICS



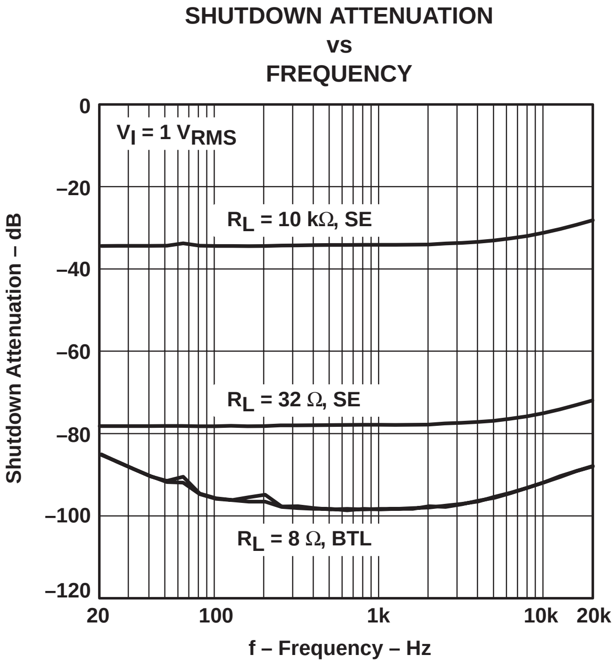
CROSSTALK
vs
FREQUENCY

Figure 17



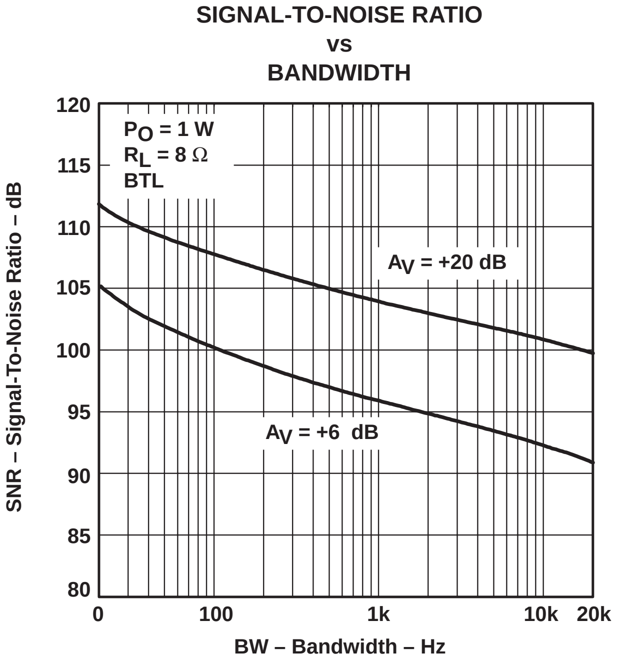
CROSSTALK
vs
FREQUENCY

Figure 18



SHUTDOWN ATTENUATION
vs
FREQUENCY

Figure 19



SIGNAL-TO-NOISE RATIO
vs
BANDWIDTH

Figure 20

TYPICAL CHARACTERISTICS

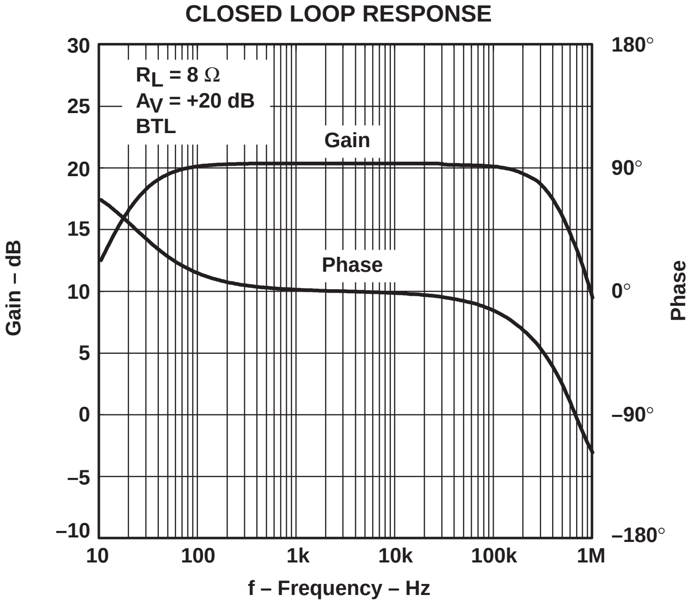


Figure 21

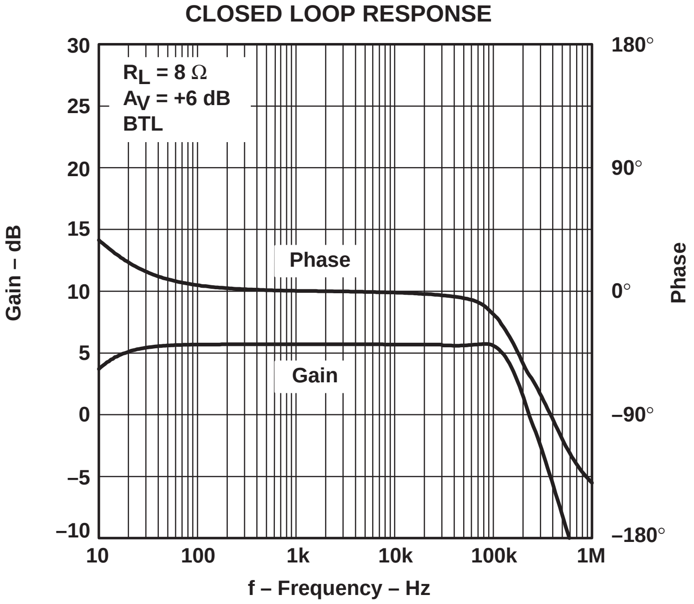


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

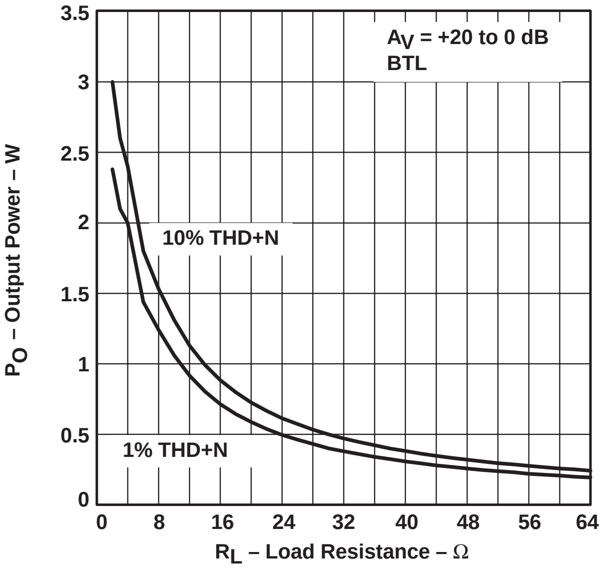


Figure 23

OUTPUT POWER
vs
LOAD RESISTANCE

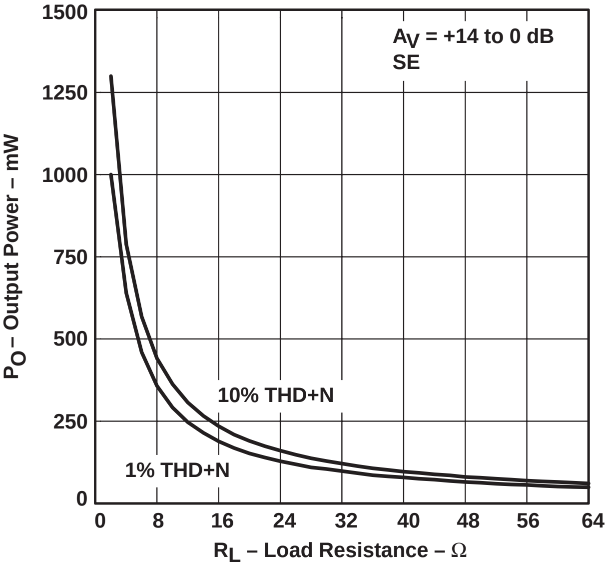


Figure 24

POWER DISSIPATION
vs
OUTPUT POWER

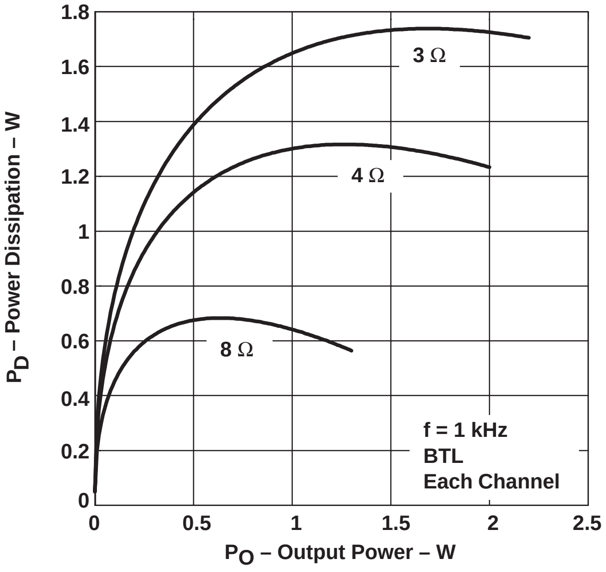


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

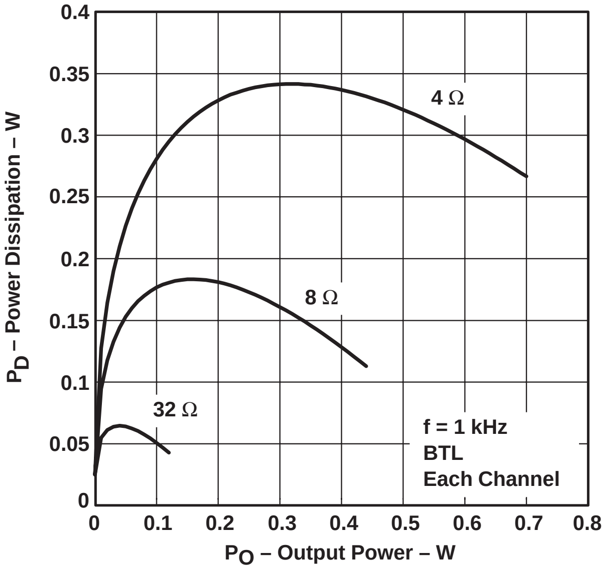


Figure 26

APPLICATION INFORMATION

POWER DISSIPATION vs AMBIENT TEMPERATURE

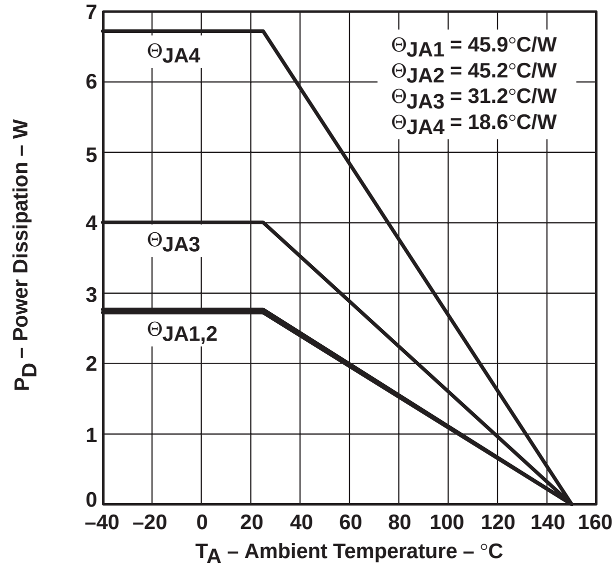


Figure 27

INPUT IMPEDANCE vs GAIN

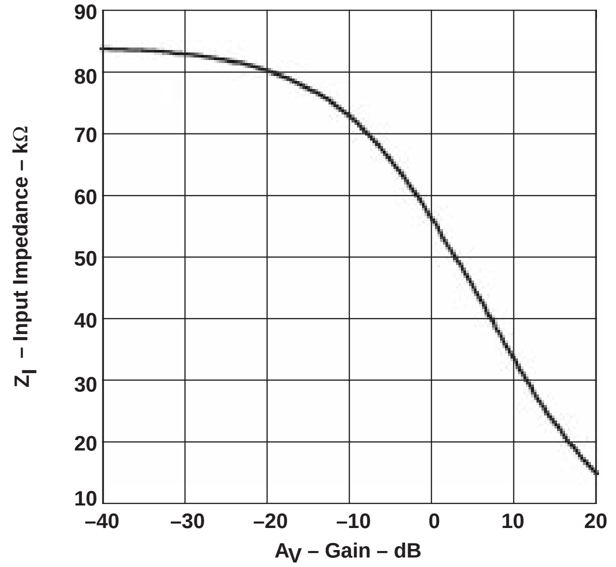


Figure 28

APPLICATION INFORMATION

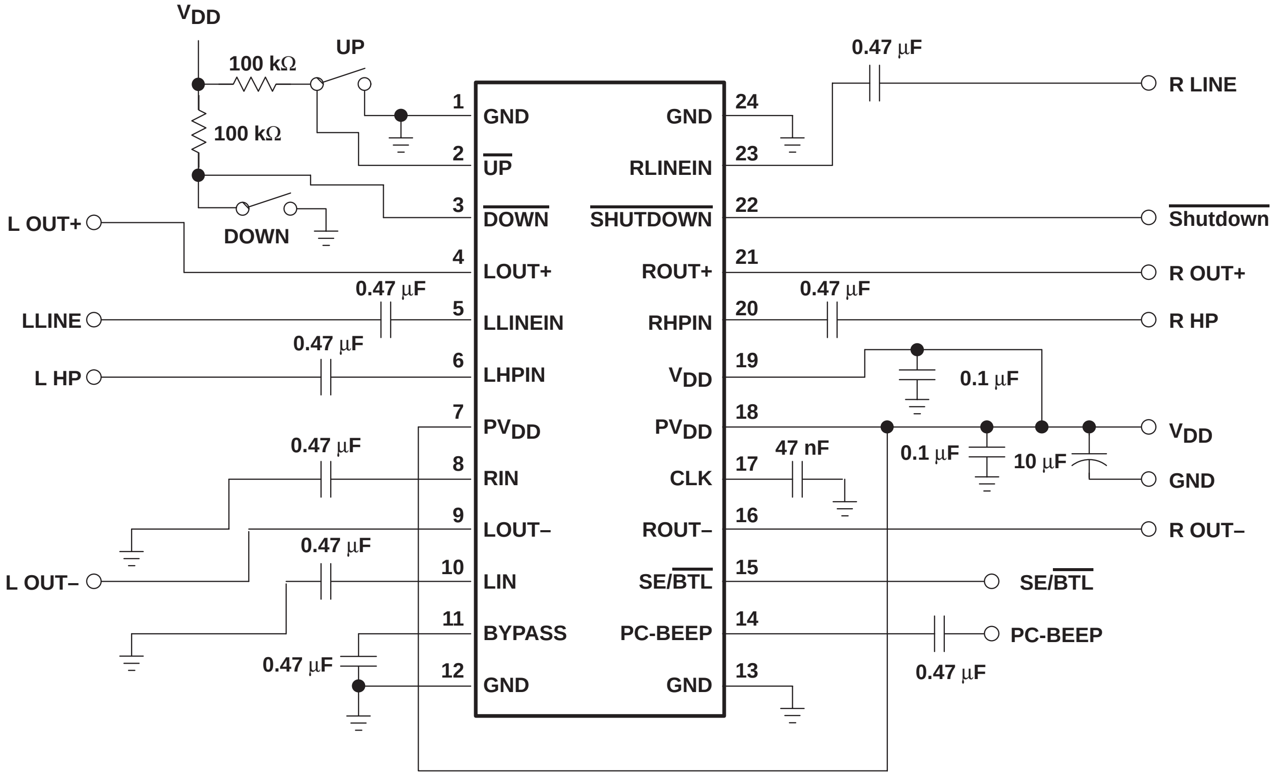
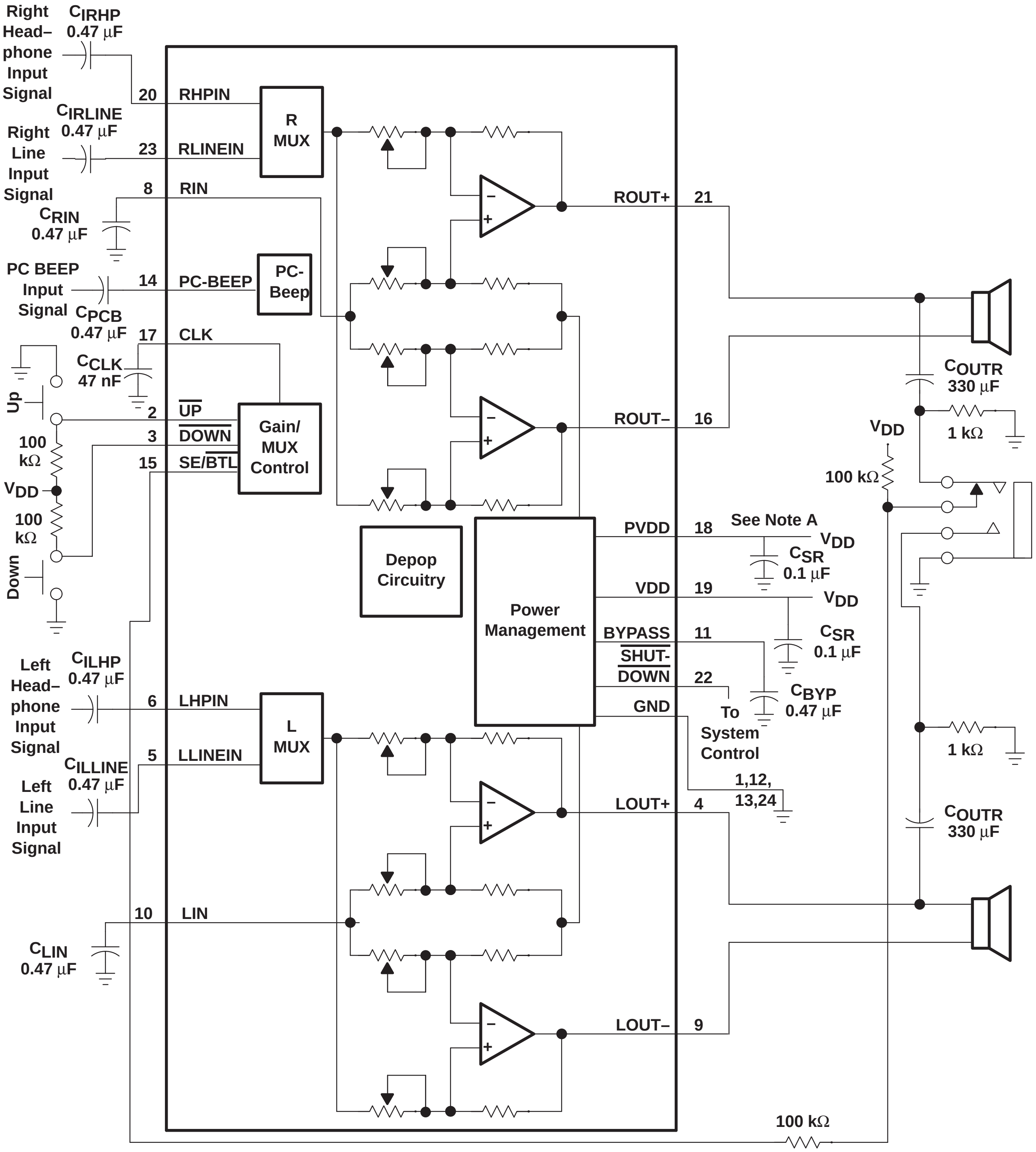


Figure 29. Typical TPA0162 Application Circuit

selection of components

Figure 30 and Figure 31 are a schematic diagrams of typical notebook computer application circuits.

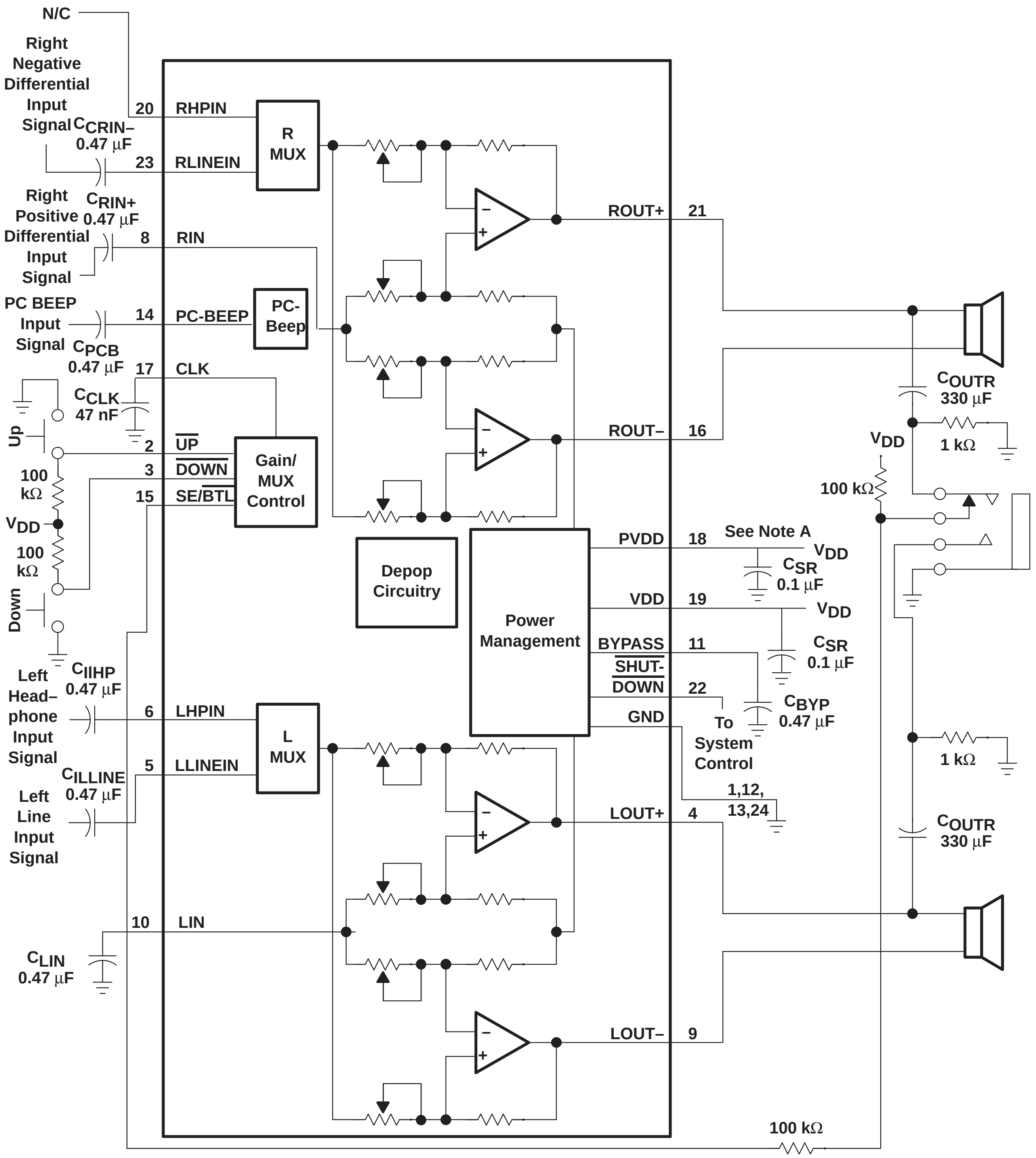
APPLICATION INFORMATION



NOTE A: A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0162 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



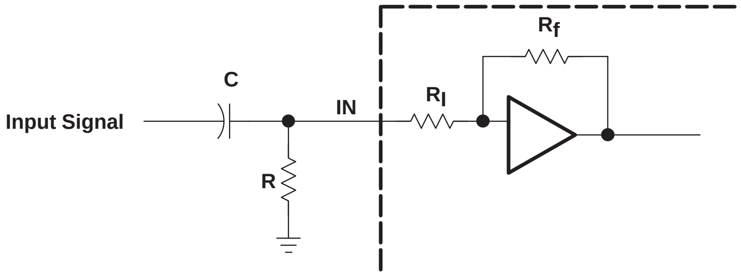
NOTE A: A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0162 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The input resistance at each gain setting is given in Figure 28.

The –3 dB frequency can be calculated using equation 1:

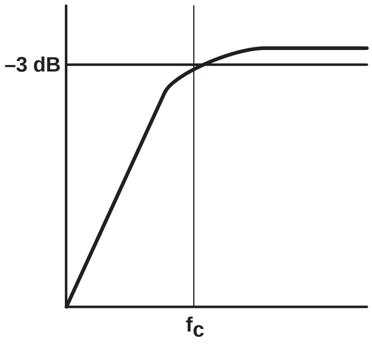
$$f_{-3\ \mathrm{dB}} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \qquad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(\mathrm{highpass})} = \frac{1}{2\pi Z_I C_I} \qquad (2)$$



APPLICATION INFORMATION

input capacitor, C_I (continued)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \tag{3}$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0162 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

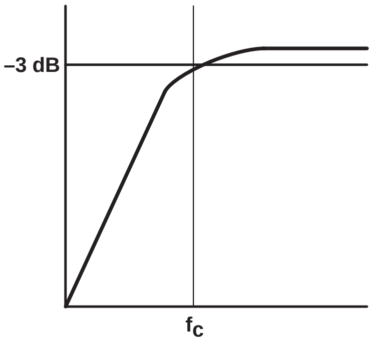
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \tag{4}$$



APPLICATION INFORMATION

output coupling capacitor, C_C (continued)

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 μF	161 Hz
4 Ω	330 μF	120 Hz
8 Ω	330 μF	60 Hz
32 Ω	330 μF	15 Hz
10,000 Ω	330 μF	0.05 Hz
47,000 Ω	330 μF	0.01 Hz

As Table 1 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 32 shows a class-AB audio power amplifier (APA) in a BTL configuration. The TPA0162 BTL amplifier consists of two class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^{2}}{R_L}$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

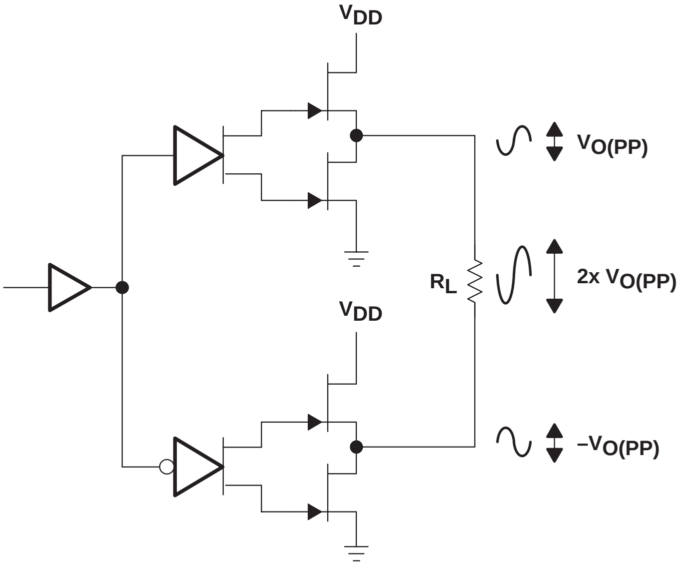


Figure 32. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 33. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_C = \frac{1}{2\pi R_L C_C} \qquad (6)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

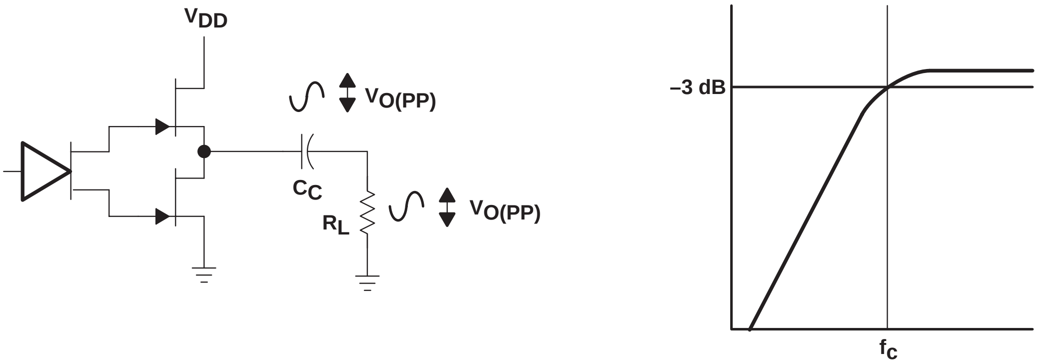


Figure 33. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor section.

single-ended operation

In SE mode (see Figure 32 and Figure 33), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier’s gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 34).

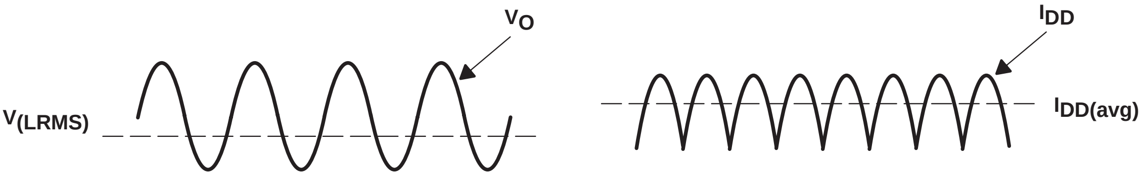


Figure 34. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{{V_P}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}\text{avg} \quad \text{and} \quad I_{DD}\text{avg} = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\pi} \times \frac{V_P}{R_L}\left[\cos(t)\right]_0^{\pi} = \frac{2V_P}{\pi\, R_L}$$

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Therefore,

$$P_{SUP} = \frac{2\ V_{DD}\ V_P}{\pi\ R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\dfrac{V_P^{\ 2}}{2\ R_L}}{\dfrac{2\ V_{DD}\ V_P}{\pi\ R_L}} = \frac{\pi\ V_P}{4\ V_{DD}}$$

Where:

$$V_P = \sqrt{2\ P_L\ R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\ \sqrt{2\ P_L\ R_L}}{4\ V_{DD}} \qquad (8)$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
I_{DD}avg = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 2 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 2. Efficiency vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature the internal dissipated power at the average output power level must be used. From the TPA0162 data sheet, one can see that when the TPA0162 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{4W}{1W}\right) = 6\ \text{dB} \tag{9}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$\begin{aligned} P_W &= 10^{PdB/10} \times P_{ref} \\ &= 63\ \text{mW (18 dB crest factor)} \\ &= 125\ \text{mW (15 dB crest factor)} \\ &= 250\ \text{mW (9 dB crest factor)} \\ &= 500\ \text{mW (6 dB crest factor)} \\ &= 1000\ \text{mW (3 dB crest factor)} \\ &= 2000\ \text{mW (15 dB crest factor)} \end{aligned} \tag{10}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0162 and maximum ambient temperatures is shown in Table 3.

Table 3. TPA0162 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 4. TPA0162 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \qquad (11)$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table on page 4. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°\text{C/W} \qquad (12)$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0162 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A\ \text{Max} &= T_J\ \text{Max} - \Theta_{JA} P_D \qquad (13) \\ &= 150 - 45(0.6 \times 2) = 96°\text{C (15 dB crest factor)} \end{aligned}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 3 and 4 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0162 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 3 and 4 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0162 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0162, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0162 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0162 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 35.

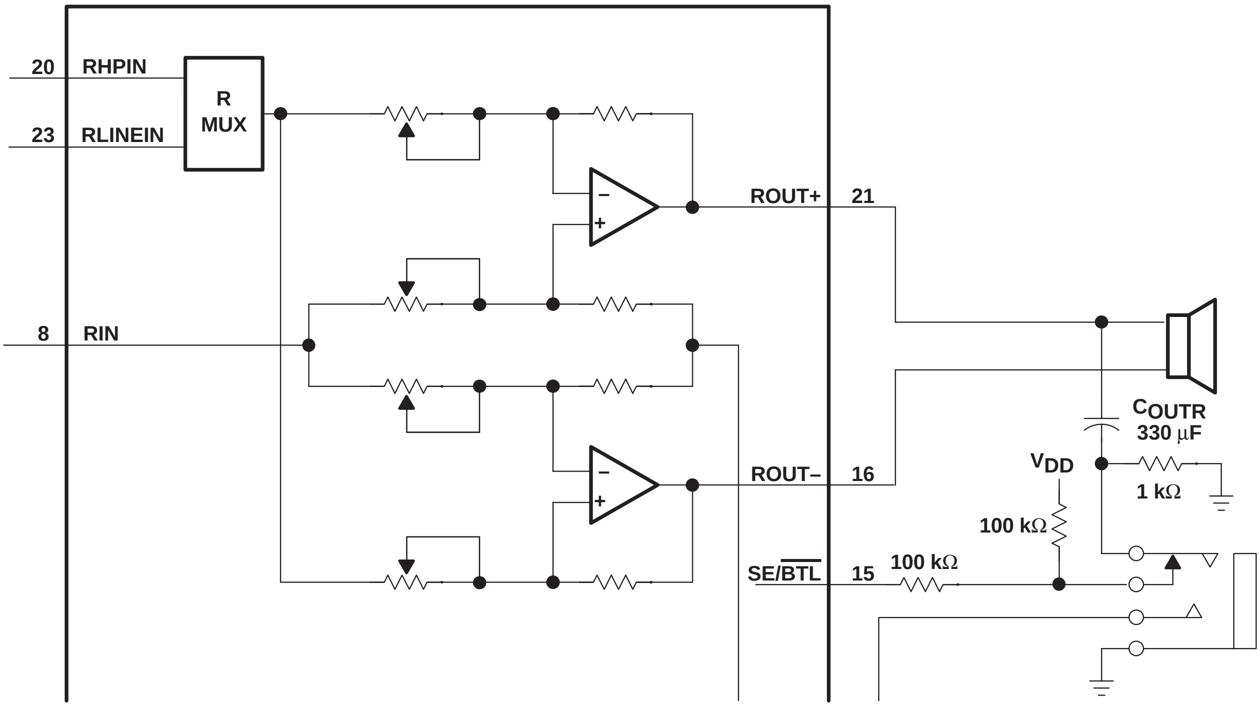


Figure 35. TPA0162 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut-down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

APPLICATION INFORMATION

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated automatically, but may be selected manually by pulling PCB ENABLE high. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be a accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

When PCB ENABLE is held high, PC BEEP is selected and the LINEIN and HPIN inputs are deactivated regardless of the input signal. PCB ENABLE has an internal 100 kΩ pulldown resistor and will trip at approximately $V_{DD}/2$.

If it is desired to ac couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi\ f_{PCB}\ (100\ k\Omega)} \qquad (14)$$

The PC BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

APPLICATION INFORMATION

Input MUX operation

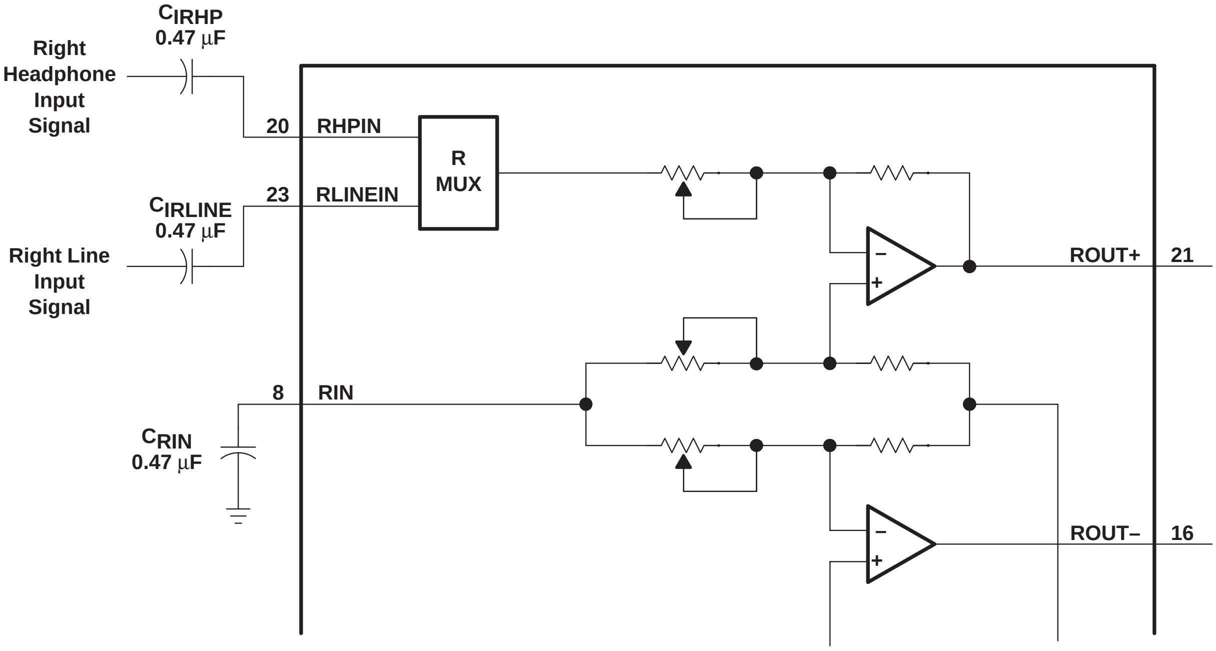


Figure 36. TPA0162 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

shutdown modes

The TPA0162 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 5. Shutdown and Mute Mode Functions

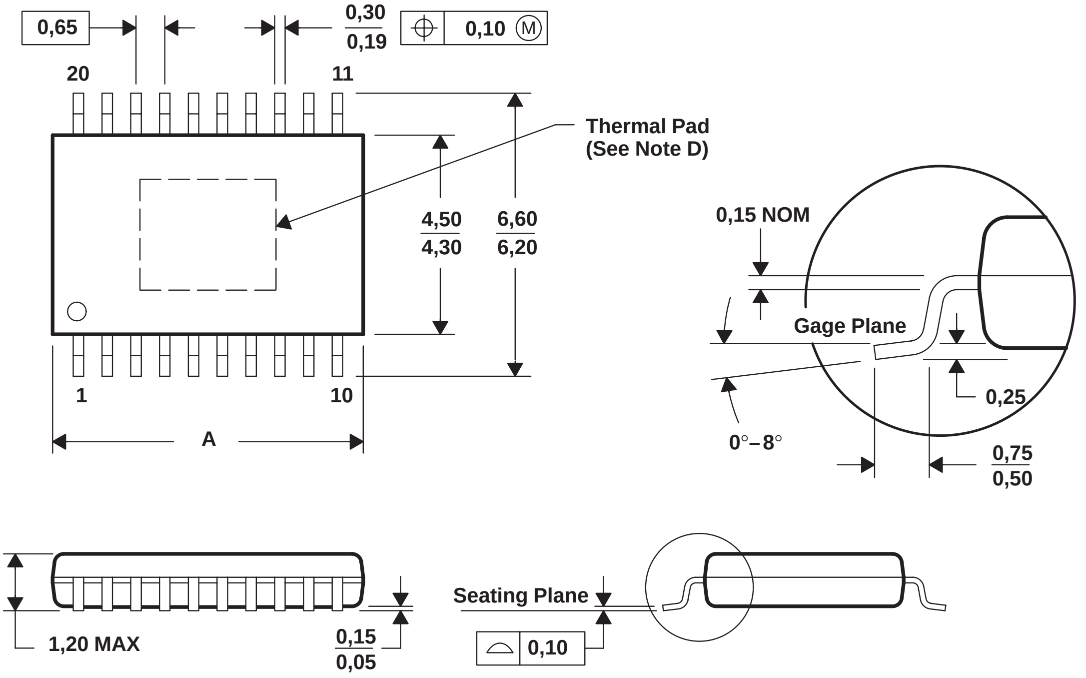
INPUTS†		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



PINS ** DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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