

TL05x, TL05xA, TL05xY
ENHANCED-JFET LOW-OFFSET
OPERATIONAL AMPLIFIERS
SLOS178 – FEBRUARY 1997

- Direct Upgrades to TL07x and TL08x BiFET Operational Amplifiers
- Faster Slew Rate (20 V/ μ s Typ) Without Increased Power Consumption
- On-Chip Offset Voltage Trimming for Improved DC Performance and Precision Grades Are Available (1.5 mV, TL051A)
- Available in TSSOP for Small Form-Factor Designs

description

The TL05x series of JFET-input operational amplifiers offers improved dc and ac characteristics over the TL07x and TL08x families of BiFET operational amplifiers. On-chip zener trimming of offset voltage yields precision grades as low as 1.5 mV (TL051A) for greater accuracy in dc-coupled applications. Texas Instruments improved BiFET process and optimized designs also yield improved bandwidth and slew rate without increased power consumption. The TL05x devices are pin-compatible with the TL07x and TL08x and can be used to upgrade existing circuits or for optimal performance in new designs.

BiFET operational amplifiers offer the inherently higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. This makes them better suited for interfacing with high-impedance sensors or very low-level ac signals. They also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption.

The TL05x family was designed to offer higher precision and better ac response than the TL08x with the low noise floor of the TL07x. Designers requiring significantly faster ac response or ensured lower noise should consider the Excalibur TLE208x and TLE207x families of BiFET operational amplifiers.

AVAILABLE OPTIONS

TA	V _{IOMAX} AT 25°C	PACKAGED DEVICES						CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	800 μ V	TL051ACD TL052ACD	—	—	—	—	—	TL051ACP TL052ACP
	1.5 mV	TL051CD TL052CD TL054ACD	—	—	—	TL054ACN	TL051CP TL052CP	TL051Y TL052Y TL054Y
	4 mV	TL054CD	—	—	—	TL054CN	—	
−40°C to 85°C	800 μ V	TL051AID TL052AID	—	—	—	—	TL051AIP TL052AIP	—
	1.5 mV	TL051ID TL052ID TL054AID	—	—	—	TL054AIN	TL051IP TL052IP	—
	4 mV	TL054ID	—	—	—	TL054IN	—	—
−55°C to 125°C	800 μ V	TL051AMD TL052AMD	TL051AMFK TL052AMFK	—	TL051AMJG TL052AMJG	—	TL051AMP TL052AMP	—
	1.5 mV	TL051MD TL052MD TL054AMD	TL051MFK TL052MFK TL054AMFK	TL054AMJ	TL051MJJG TL052MJJG	TL054AMN	TL051MP TL052MP	—
	4 mV	TL054MD	TL054MFK	TL054MJ	—	TL054MN	—	

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TL054CDR).

‡ Chip forms are tested at 25°C.



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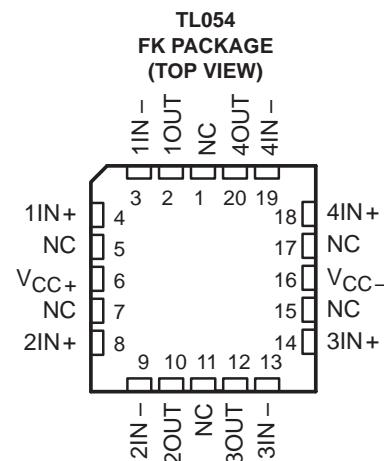
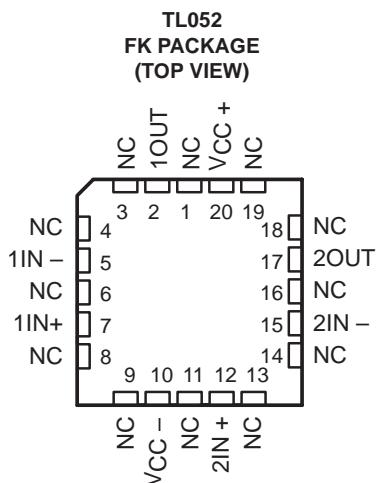
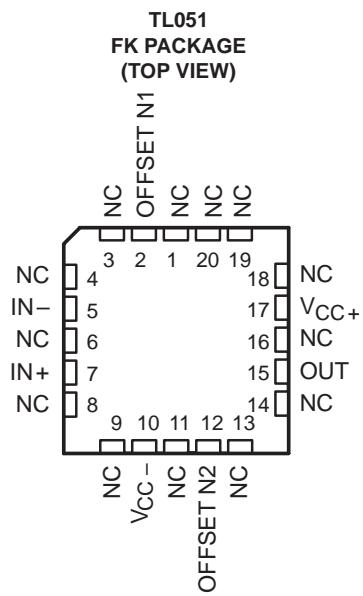
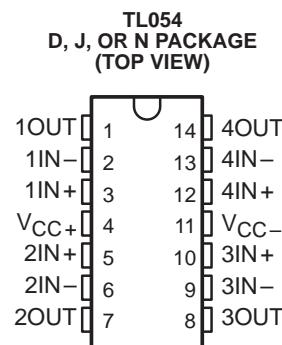
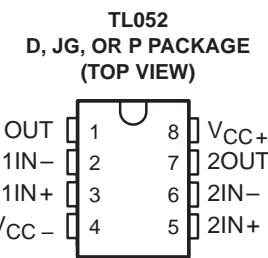
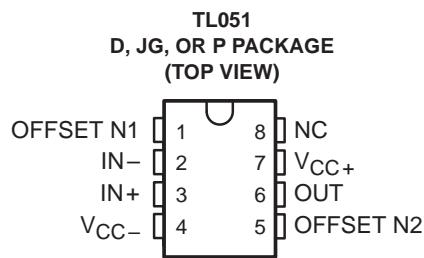
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description (continued)

Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required and loads should be terminated to a virtual-ground node at midsupply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

The TL05x are fully specified at ± 15 V and ± 5 V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC-prefix) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to the slew rate and bandwidth requirements, and also the output loading.

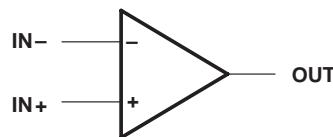


NC – No internal connection

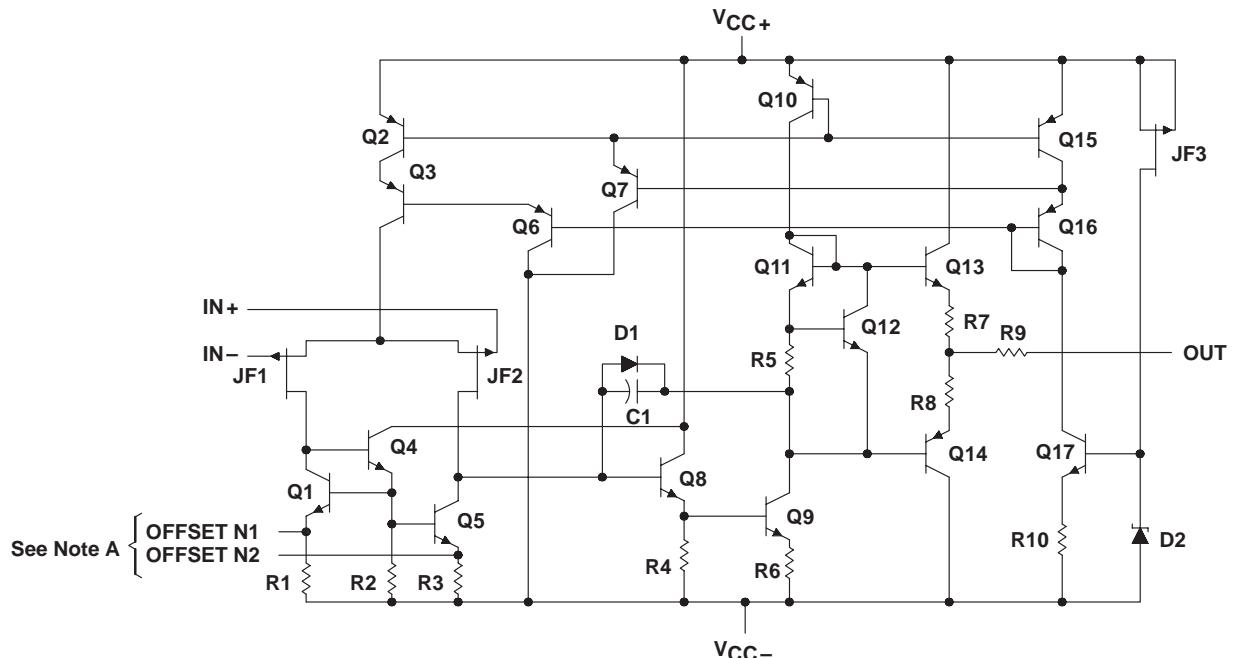


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symbol (each amplifier)



equivalent schematic (each amplifier)



NOTE A: OFFSET N1 and OFFSET N2 are only available on the TL051x.

ACTUAL DEVICE COMPONENT COUNT†			
COMPONENT	TL051	TL052	TL054
Transistors	20	34	62
Resistors	10	19	37
Diodes	2	3	5
Capacitors	1	2	4

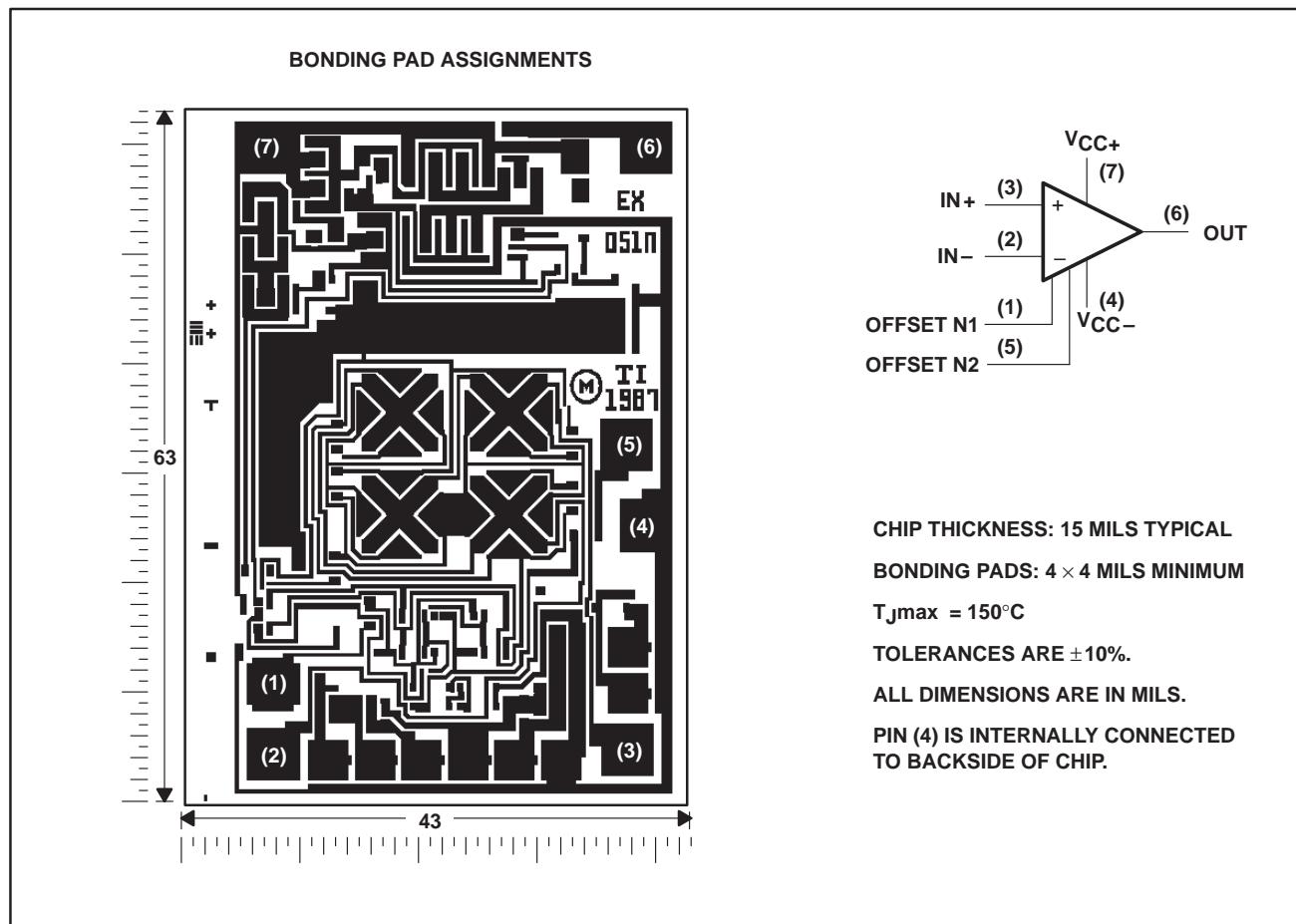
† These figures include all four amplifiers and all ESD, bias, and trim circuitry.

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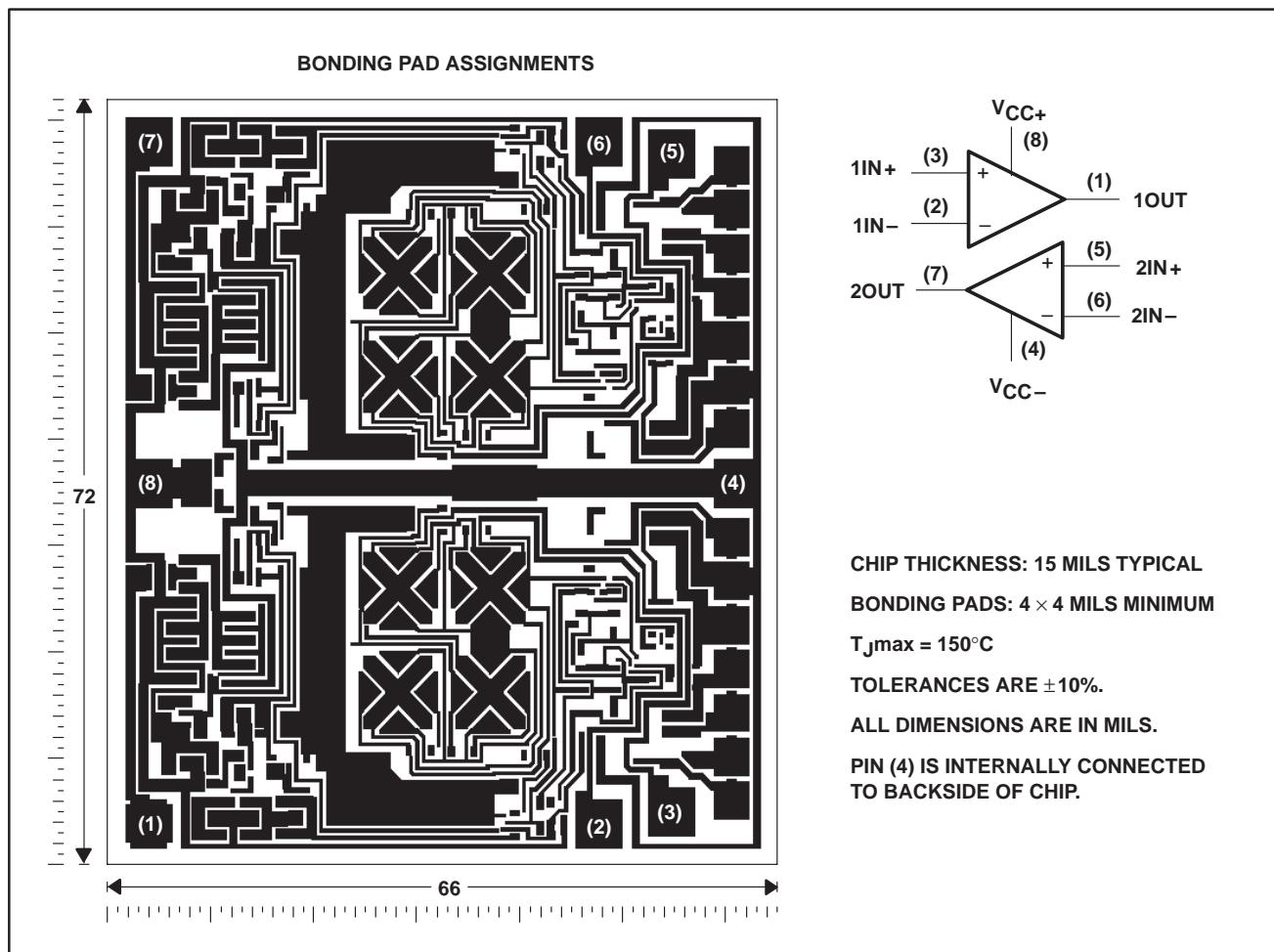
TL051Y chip information

This chip, when properly assembled, displays characteristics similar to the TL051. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



TL052Y chip information

This chip, when properly assembled, displays characteristics similar to the TL052. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

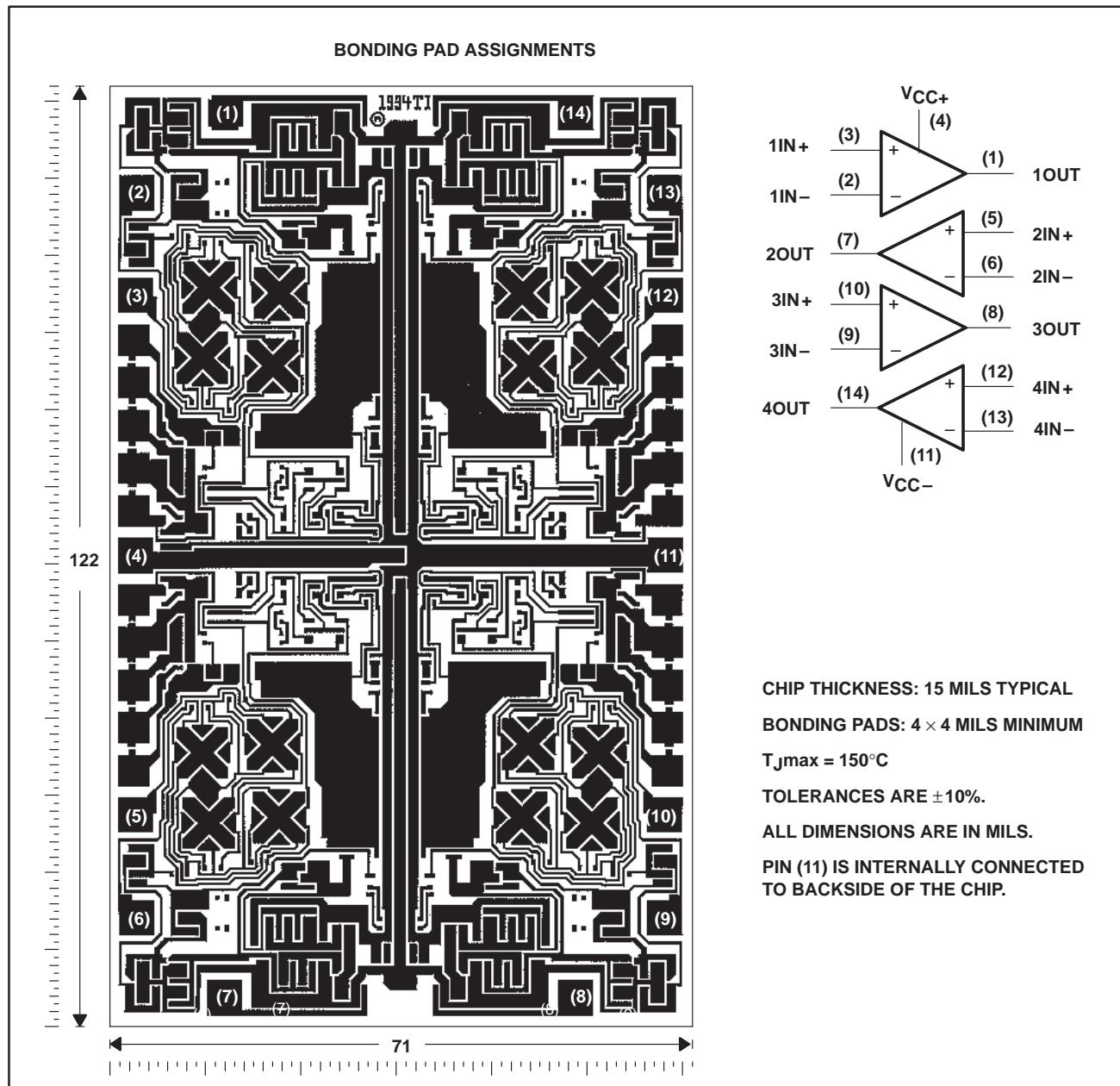


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TL054 chip information

This chip, when properly assembled, displays characteristics similar to the TL054C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. These chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	-18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 80 mA
Total current into V_{CC+}	160 mA
Total current out of V_{CC-}	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A :	C suffix	0°C to 70°C
	I suffix	-40°C to 85°C
	M suffix	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1.6 mm (1/16inch) from case for 10 seconds: D, N, or P package	260°C
Lead temperature 1.6 mm (1/16inch) from case for 60 seconds: J or JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING		
						C SUFFIX	I SUFFIX
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
D-8	725 mW	5.8 mW/ $^\circ\text{C}$	464 mW	377 mW	145 mW		
D-14	950 mW	7.6 mW/ $^\circ\text{C}$	608 mW	494 mW	190 mW		
FK	1375 mW	11.0 mW/ $^\circ\text{C}$	880 mW	715 mW	275 mW		
J	1375 mW	11.0 mW/ $^\circ\text{C}$	880 mW	715 mW	275 mW		
JG	1050 mW	8.4 mW/ $^\circ\text{C}$	672 mW	546 mW	210 mW		
N	1575 mW	12.6 mW/ $^\circ\text{C}$	1008 mW	819 mW	315 mW		
P	1000 mW	8.0 mW/ $^\circ\text{C}$	640 mW	520 mW	200 mW		

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 5	± 15	± 5	± 15	± 5	± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	-1	4	-1	4	-1	4	V
	$V_{CC\pm} = \pm 15$ V	-11	11	-11	11	-11	11	
Operating free-air temperature, T_A		0	70	-40	85	-55	125	°C



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TL051C and TL051AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL051C, TL051AC						UNIT	
			V _{CC} \pm ± 5 V			V _{CC} \pm ± 15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	TL051C	25°C	0.75	3.5	0.59	1.5		mV	
			Full range		4.5		2.5			
		TL051AC	25°C	0.55	2.8	0.35	0.8			
			Full range		3.8		1.8			
	αV_{IO} Temperature coefficient of input offset voltage [‡]	TL051C	25°C to 70°C		8		8		$\mu V/^\circ C$	
			25°C to 70°C		8		8	25		
			25°C		0.04		0.04			
I _{IO}	Input offset current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	4	100	5	100	pA		
			70°C	0.02	1	0.025	1	nA		
I _{IB}	Input bias current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	20	200	30	200	pA		
			70°C	0.15	4	0.2	4	nA		
V _{ICR}	Common-mode input voltage range		25°C	-1	-2.3	-11	-12.3		V	
				to 4	to 5.6	to 11	to 15.6			
			Full range	-1		-11				
				to 4		to 11				
V _{OM} +	Maximum positive peak output voltage swing	R _L = 10 k Ω	25°C	3	4.2	13	13.9		V	
			Full range	3		13				
		R _L = 2 k Ω	25°C	2.5	3.8	11.5	12.7			
			Full range	2.5		11.5				
V _{OM} -	Maximum negative peak output voltage swing	R _L = 10 k Ω	25°C	-2.5	-3.5	-12	-13.2		V	
			Full range	-2.5		-12				
		R _L = 2 k Ω	25°C	-2.3	-3.2	-11	-12			
			Full range	-2.3		-11				
AVD	Large-signal differential voltage amplification [¶]	R _L = 2 k Ω	25°C	25	59	50	105		V/mV	
			0°C	30	65	60	129			
			70°C	20	46	30	85			
r _i	Input resistance		25°C		10 ¹²		10 ¹²	Ω		
c _i	Input capacitance		25°C		10		12	pF		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω	25°C	65	85	75	93		dB	
			0°C	65	84	75	92			
			70°C	65	84	75	91			
k _{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V _O = 0, R _S = 50 Ω	25°C	75	99	75	99		dB	
			0°C	75	98	75	98			
			70°C	75	97	75	97			
I _{CC}	Supply current	V _O = 0, No load	25°C		2.6	3.2	2.7	3.2	mA	
			0°C		2.7	3.2	2.8	3.2		
			70°C		2.6	3.2	2.7	3.2		

[†] Full range is 0°C to 70°C.

[‡] This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[§] Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

[¶] For V_{CC \pm} = ± 5 V, V_O = ± 2.3 V, or for V_{CC \pm} = ± 15 V, V_O = ± 10 V.



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TL051C and TL051AC operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL051C, TL051AC						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR + Positive slew rate at unity gain‡	R _L = 2 kΩ, C _L = 100 pF, See Figure 1	25°C	16			13	20		V/μs	
		Full range		16.4		11	22.6			
		25°C	15			13	18			
		Full range		16		11	19.3			
SR - Negative slew rate at unity gain‡		25°C	55			56			ns	
		0°C	54			55				
		70°C	63			63				
		25°C	55			57				
t _r Rise time	V _I (PP) = ±10 mV, R _L = 2 kΩ, C _L = 100 pF, See Figures 1 and 2	0°C	54			56			ns	
		70°C	62			64				
		25°C	24%			19%				
		0°C	24%			19%				
t _f Fall time		70°C	24%			19%				
		25°C	55			57				
		0°C	54			56				
		70°C	62			64				
Overshoot factor		25°C	24%			19%				
		0°C	24%			19%				
		70°C	24%			19%				
		25°C	75			75			nV/√Hz	
V _n Equivalent input noise voltage§	R _S = 20 Ω, See Figure 3	f = 10 Hz	25°C	18		18	30			
		f = 1 kHz	25°C							
V _N (PP) Peak-to-peak equivalent input noise voltage	f = 10 Hz to 10 kHz	25°C		4		4			μV	
I _n Equivalent input noise current		f = 1 kHz	25°C	0.01		0.01			pA/√Hz	
THD Total harmonic distortion¶	R _S = 1 kΩ, f = 1 kHz	R _L = 2 kΩ,	25°C	0.003%		0.003%				
B ₁ Unity-gain bandwidth	V _I = 10 mV, C _L = 25 pF, See Figure 4	25°C		3		3.1			MHz	
		0°C		3.2		3.3				
		70°C		2.7		2.8				
φ _m Phase margin at unity gain	V _I = 10 mV, C _L = 25 pF, See Figure 4	25°C		59°		62°				
		0°C		58°		62°				
		70°C		59°		62°				

† Full range is 0°C to 70°C.

‡ For V_{CC}_± = ±5 V, V_I(PP) = ±1 V; for V_{CC}_± = ±15 V, V_I(PP) = ±5 V.

§ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For V_{CC}_± = ±5 V, V_Orms = 1 V; for V_{CC}_± = ±15 V, V_Orms = 6 V.

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TL051I and TL051AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL051I, TL051AI						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage Temperature coefficient of input offset voltage [‡] Input offset voltage long-term drift [§]	TL051I	25°C	0.75	3.5	0.59	1.5		mV	
			Full range		5.3			3.3		
		TL051AI	25°C	0.55	2.8	0.35	0.8			
			Full range		4.6			2.6		
		TL051I	25°C to 85°C		7		8		μV/°C	
			25°C to 85°C		8		8	25		
I _{IO}			25°C		0.04		0.04		μV/mo	
			85°C							
I _{IB}	Input bias current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	20	200	30	200	pA	pA	
			85°C	0.6	20	0.7	20	nA		
V _{ICR}	Common-mode input voltage range		25°C	-1 to 4	-2.3 to 5.6	-11 to 11	-12.3 to 15.6		V	
			Full range	-1 to 4		-11 to 11				
		R _L = 10 kΩ	25°C	3	4.2	13	13.9			
			Full range	3		13				
V _{OM} +	Maximum positive peak output voltage swing	R _L = 2 kΩ	25°C	2.5	3.8	11.5	12.7		V	
			Full range	2.5		11.5				
		R _L = 10 kΩ	25°C	-2.5	-3.5	-12	-13.2			
			Full range	-2.5		-12				
V _{OM} -	Maximum negative peak output voltage swing	R _L = 2 kΩ	25°C	-2.3	-3.2	-11	-12		V	
			Full range	-2.3		-11				
		R _L = 2 kΩ	25°C	25	59	50	105		V/mV	
			-40°C	30	74	60	145			
			85°C	20	43	30	76			
r _i	Input resistance		25°C		10 ¹²		10 ¹²	Ω		
c _i	Input capacitance		25°C		10		12	pF		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} _{min} , V _O = 0, R _S = 50 Ω	25°C	65	85	75	93		dB	
			-40°C	65	83	75	90			
			85°C	65	84	75	93			
k _{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V _O = 0, R _S = 50 Ω	25°C	75	99	75	99		dB	
			-40°C	75	98	75	98			
			85°C	75	99	75	99			
I _{CC}	Supply current	V _O = 0, No load	25°C		2.6	3.2	2.7	3.2	mA	
			-40°C		2.4	3.2	2.6	3.2		
			85°C		2.5	3.2	2.6	3.2		

[†] Full range is -40°C to 85°C

[‡] This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[§] Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

[¶] For V_{CC}_± = ±5 V, V_O = ±2.3 V, or for V_{CC}_± = ±15 V, V_O = ±10 V.



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TL051I and TL051AI operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL051I, TL051AI						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR + Positive slew rate at unity gain [‡]	R _L = 2 kΩ, C _L = 100 pF, See Figure 1	25°C	16			13	20		V/μs	
		Full range					11			
		25°C	15			13	18			
		Full range					11			
SR - Negative slew rate at unity gain [‡]		25°C	55			56			ns	
		-40°C	52			53				
		85°C	64			65				
		25°C	55			57				
t _r Rise time	V _I (PP) = ±10 mV, R _L = 2 kΩ, C _L = 100 pF, See Figures 1 and 2	-40°C	51			53				
		85°C	64			65				
		25°C	24%			19%				
		-40°C	24%			19%				
t _f Fall time		85°C	24%			19%				
		25°C	75			75			nV/√Hz	
		25°C	18			18	30			
		f = 10 Hz to 10 kHz	25°C	4		4				
V _n Equivalent input noise voltage [§]	R _S = 20 Ω, See Figure 3	f = 10 Hz	25°C	0.01		0.01			pA/√Hz	
V _N (PP) Peak-to-peak equivalent input noise voltage		f = 1 kHz	25°C	0.003%		0.003%				
I _n Equivalent input noise current	f = 1 kHz		25°C							
THD Total harmonic distortion [¶]	R _S = 1 kΩ, f = 1 kHz	R _L = 2 kΩ,	25°C	3		3.1				
B ₁ Unity-gain bandwidth	V _I = 10 mV, C _L = 25 pF, See Figure 4	R _L = 2 kΩ, See Figure 4	-40°C	3.5		3.6			MHz	
			85°C	2.6		2.7				
			25°C	59°		62°				
φ _m Phase margin at unity gain	V _I = 10 mV, C _L = 25 pF, See Figure 4	R _L = 2 kΩ, See Figure 4	-40°C	58°		61°				
			85°C	59°		62°				

[†] Full range is -40°C to 85°C.

[‡] For V_{CC}_± = ±5 V, V_I(PP) = ±1 V; for V_{CC}_± = ±15 V, V_I(PP) = ±5 V.

[§] This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[¶] For V_{CC}_± = ±5 V, V_Orms = 1 V; for V_{CC}_± = ±15 V, V_Orms = 6 V.

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TL051M and TL051AM electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL051M, TL051AM						UNIT	
			V _{CC} \pm ± 5 V			V _{CC} \pm ± 15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	TL051M	25°C	0.75	3.5	0.59	1.5		mV	
			Full range		6.5		4.5			
		TL051AM	25°C	0.55	2.8	0.35	0.8			
			Full range		5.8		3.8			
	Temperature coefficient of input offset voltage	TL051M	25°C to 125°C		8		8		$\mu\text{V}/^\circ\text{C}$	
		TL051AM	25°C to 125°C		8		8			
	Input offset voltage long-term drift‡		25°C		0.04		0.04		$\mu\text{V}/\text{mo}$	
I _{IO}	Input offset current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	4	100	5	100	pA	pA	
I _{IB}	Input bias current		125°C	1	20	2	20	nA		
V _{ICR}	Common-mode input voltage range		25°C	-1 to 4	-2.3 to 5.6	-11 to 11	-12.3 to 15.6		V	
			Full range	-1 to 4	to 5.6	-11 to 11	to 15.6			
			25°C	2.5	3.8	11.5	12.7			
			Full range	2.5		11.5				
V _{OM+}	Maximum positive peak output voltage swing	R _L = 10 k Ω	25°C	3	4.2	13	13.9		V	
			Full range	3		13				
	Maximum negative peak output voltage swing	R _L = 2 k Ω	25°C	2.5	3.8	11.5	12.7			
			Full range	2.5		11.5				
V _{OM-}	Maximum positive peak output voltage swing	R _L = 10 k Ω	25°C	-2.5	-3.5	-12	-13.2		V	
			Full range	-2.5		-12				
	Maximum negative peak output voltage swing	R _L = 2 k Ω	25°C	-2.3	-3.2	-11	-12			
			Full range	-2.3		-11				
AVD	Large-signal differential voltage amplification§	R _L = 2 k Ω	25°C	25	59	50	105		V/mV	
			-55°C	30	76	60	149			
			125°C	10	32	15	49			
r _i	Input resistance		25°C		10 ¹²		10 ¹²		Ω	
c _i	Input capacitance		25°C		10		12		pF	
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω	25°C	65	85	75	93		dB	
			-55°C	65	83	75	92			
			125°C	65	84	75	94			
k _{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V _O = 0, R _S = 50 Ω	25°C	75	99	75	99		dB	
			-55°C	75	98	75	98			
			125°C	75	100	75	100			
I _{CC}	Supply current	V _O = 0, No load	25°C		2.6	3.2	2.7	3.2	mA	
			-55°C		2.3	3.2	2.4	3.2		
			125°C		2.4	3.2	2.5	3.2		

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For V_{CC \pm} = ± 5 V, V_O = ± 2.3 V, or for V_{CC \pm} = ± 15 V, V_O = ± 10 V.



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TL051M and TL051AM operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA	TL051M, TL051AM						UNIT	
			V _{CC} ± = ±5 V			V _{CC} ± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR+	Positive slew rate at unity gain†	RL = 2 kΩ, CL = 100 pF, See Figure 1	25°C	16		13	20		V/μs	
SR-			25°C	15		13				
t _r	Rise time	VI(PP) = ±10 mV, RL = 2 kΩ, CL = 100 pF, See Figures 1 and 2	25°C	55		56			ns	
t _f	Fall time		-55°C	51		52				
			125°C	68		68				
	Overshoot factor		25°C	55		57				
			-55°C	51		52				
			125°C	68		69				
V _n	Equivalent input noise voltage‡	RS = 20 Ω, See Figure 3	f = 10 Hz	25°C	75		75		nV/√Hz	
V _{N(PP)}	Peak-to-peak equivalent input noise voltage		f = 1 kHz	25°C	18		19			
I _n	Equivalent input noise current		f = 10 Hz to 10 kHz	25°C	4		4			
THD	Total harmonic distortion§	RS = 1 kΩ, RL = 2 kΩ, f = 1 kHz		25°C	0.003%		0.003%			
B ₁	Unity-gain bandwidth	V _I = 10 mV, RL = 2 kΩ, CL = 25 pF, See Figure 4		25°C	3		3.1		MHz	
				-55°C	3.6		3.7			
				125°C	2.3		2.4			
φ _m	Phase margin at unity gain	V _I = 10 mV, RL = 2 kΩ, CL = 25 pF, See Figure 4		25°C	59°		62°			
				-55°C	57°		61°			
				125°C	59°		62°			

† For V_{CC}± = ±5 V, V_{I(PP)} = ±1 V; for V_{CC}± = ±15 V, V_{I(PP)} = ±5 V.

‡ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ For V_{CC}± = ±5 V, V_{Orms} = 1 V; for V_{CC}± = ±15 V, V_{Orms} = 6 V.

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TL051Y electrical characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL051Y						UNIT	
		$V_{CC} \pm = \pm 5 \text{ V}$			$V_{CC} \pm = \pm 15 \text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	$V_O = 0, V_{IC} = 0, R_S = 50 \Omega$		0.75			0.59		mV	
I_{IO}	$V_O = 0, V_{IC} = 0,$ See Figure 5			4		5		pA	
I_{IB}	$V_O = 0, V_{IC} = 0,$ See Figure 5		20		30			pA	
V_{ICR}	Common-mode input voltage range			-2.3 to 5.6		-12.3 to 15.6		V	
V_{OM+}	$R_L = 10 \text{ k}\Omega$		4.2		13.9			V	
	$R_L = 2 \text{ k}\Omega$		3.8		12.7				
V_{OM-}	$R_L = 10 \text{ k}\Omega$		-3.5		-13.2			V	
	$R_L = 2 \text{ k}\Omega$		-3.2		-12				
AVD	Large-signal differential voltage amplification†	$R_L = 2 \text{ k}\Omega$		59		105		V/mV	
r_i	Input resistance			10^{12}		10^{12}		Ω	
c_i	Input capacitance			10		12		pF	
$CMRR$	Common-mode rejection ratio	$V_{IC} = V_{ICR\min},$ $V_O = 0, R_S = 50 \Omega$		85		93		dB	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_O = 0, R_S = 50 \Omega$		99		99		dB	
I_{CC}	Supply current	$V_O = 0, \text{ No load}$		2.6		2.7		mA	

† For $V_{CC\pm} = \pm 5 \text{ V}$, $V_O = \pm 2.3 \text{ V}$, or for $V_{CC\pm} = \pm 15 \text{ V}$, $V_O = \pm 10 \text{ V}$.

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TL051Y operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL051Y						UNIT	
		$V_{CC} \pm \pm 5 \text{ V}$			$V_{CC} \pm \pm 15 \text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX		
SR+	Positive slew rate at unity gain†	$R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figure 1	16		20			$\text{V}/\mu\text{s}$	
SR-	Negative slew rate at unity gain†		15		18				
t_r	Rise time	$V_I(\text{PP}) = \pm 10 \text{ mV}$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figures 1 and 2	55		56			ns	
t_f	Fall time		55		57				
	Overshoot factor		24%		19%				
V_n	Equivalent input noise voltage‡	$R_S = 20 \Omega$, See Figure 3	f = 10 Hz	75		75		$\text{nV}/\sqrt{\text{Hz}}$	
$V_{N(\text{PP})}$	Peak-to-peak equivalent input noise voltage		f = 1 kHz	18		18			
I_n	Equivalent input noise current	f = 1 kHz		0.01		0.01		$\text{pA}/\sqrt{\text{Hz}}$	
THD	Total harmonic distortion§	$R_S = 1 \text{ k}\Omega$, f = 1 kHz	$R_L = 2 \text{ k}\Omega$,		0.003%		0.003%		
B_1	Unity-gain bandwidth	$V_I = 10 \text{ mV}$, $C_L = 25 \text{ pF}$, See Figure 4	$R_L = 2 \text{ k}\Omega$,		3		3.1	MHz	
ϕ_m	Phase margin at unity gain	$V_I = 10 \text{ mV}$, $C_L = 25 \text{ pF}$, See Figure 4	$R_L = 2 \text{ k}\Omega$,		59°		62°		

† For $V_{CC} \pm = \pm 5 \text{ V}$, $V_I(\text{PP}) = \pm 1 \text{ V}$; for $V_{CC} \pm = \pm 15 \text{ V}$, $V_I(\text{PP}) = \pm 5 \text{ V}$.

‡ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ For $V_{CC} \pm = \pm 5 \text{ V}$, $V_{O\text{rms}} = 1 \text{ V}$; for $V_{CC} \pm = \pm 15 \text{ V}$, $V_{O\text{rms}} = 6 \text{ V}$.

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TL052C and TL052AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL052C, TL052AC						UNIT	
			V _{CC_±} = ±5 V			V _{CC_±} = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage V _O = 0, V _{IC} = 0, R _S = 50 Ω	TL052C	25°C	0.73	3.5	0.65	1.5		mV	
			Full range		4.5		2.5			
		TL052AC	25°C	0.51	2.8	0.4	0.8			
			Full range		3.8		1.8			
αV _{IO}	Temperature coefficient of input offset voltage [‡]	TL052C	25°C to 70°C		8		8		μV/°C	
			25°C to 70°C		8		6	25		
Input offset voltage long-term drift [§]	V _O = 0, R _S = 50 Ω	V _{IC} = 0,	25°C		0.04		0.04		μV/mo	
I _{IO}	Input offset current See Figure 5	V _O = 0, V _{IC} = 0,	25°C	4	100	5	100	pA		
			70°C	0.02	1	0.025	1	nA		
I _{IB}	Input bias current See Figure 5	V _O = 0, V _{IC} = 0,	25°C	20	200	30	200	pA		
			70°C	0.15	4	0.2	4	nA		
V _{ICR}	Common-mode input voltage range		25°C	-1	-2.3	-11	-12.3		V	
			to	to		to	to			
			4	5.6		11	15.6			
			Full range	-1		-11				
V _{OM+}	Maximum positive peak output voltage swing R _L = 10 kΩ	25°C	3	4.2		13	13.9		V	
		Full range	3			13				
		R _L = 2 kΩ	25°C	2.5	3.8	11.5	12.7			
			Full range	2.5		11.5				
V _{OM-}	Maximum negative peak output voltage swing R _L = 10 kΩ	25°C	-2.5	-3.5		-12	-13.2		V	
		Full range	-2.5			-12				
		R _L = 2 kΩ	25°C	-2.3	-3.2	-11	-12			
			Full range	-2.3		-11				
AVD	Large-signal differential voltage amplification [¶] R _L = 2 kΩ	25°C	25	59		50	105		V/mV	
		0°C	30	65		60	129			
		70°C	20	46		30	85			
r _i	Input resistance	25°C		10 ¹²		10 ¹²		Ω		
c _i	Input capacitance	25°C		10		12		pF		
CMRR	Common-mode rejection ratio V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω	25°C	65	85		75	93		dB	
		0°C	65	84		75	92			
		70°C	65	84		75	91			

[†] Full range is 0°C to 70°C.

[‡] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[§] Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

[¶] For V_{CC_±} = ±5 V, V_O = ±2.3 V; at V_{CC_±} = ±15 V, V_O = ±10 V.



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TL052C and TL052AC electrical characteristics at specified free-air temperature (continued)

PARAMETER	TEST CONDITIONS	TA	TL052C, TL052AC						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
k _{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} \pm / \Delta V_{IO}$)	V _O = 0, R _S = 50 Ω	25°C	75	99	75	99	99	dB	
			0°C	75	98	75	98	98		
			70°C	75	97	75	97	97		
I _{CC}	Supply current (two amplifiers)	V _O = 0, No load	25°C	4.6	5.6	4.8	5.6	5.6	mA	
			0°C	4.7	6.4	4.8	6.4	6.4		
			70°C	4.4	6.4	4.6	6.4	6.4		
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100	25°C	120	120	120	120	120	dB	

TL052C and TL052AC operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL052C, TL052AC						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR +	Slew rate at unity gain	R _L = 2 kΩ, C _L = 100 pF, See Figure 1	25°C	17.8	9	20.7			V/μs	
			Full range			8				
			25°C	15.4	9	17.8				
			Full range			8				
t _r	Rise time	V _I (PP) = ±10 mV, R _L = 2 kΩ, C _L = 100 pF, See Figures 1 and 2	25°C	55	56				ns	
			0°C	54	55					
t _f	Fall time		70°C	63	63					
			25°C	55	57					
			0°C	54	56					
			70°C	62	64					
Overshoot factor			25°C	24%	19%					
			0°C	24%	19%					
			70°C	24%	19%					
V _n	Equivalent input noise voltage [§]	R _S = 20 Ω, See Figure 3	f = 10 Hz	25°C	71	71			nV/√Hz	
			f = 1 kHz	25°C	19	19	30			
V _N (PP)	Peak-to-peak equivalent input noise current	f = 10 Hz t 10 kHz	25°C		4	4			μV	
I _n	Equivalent input noise current		25°C		0.01	0.01			pA/√Hz	
THD	Total harmonic distortion [¶]	R _S = 1 kΩ, f = 1 kHz	R _L = 2 kΩ,	25°C	0.003%	0.003%				
B ₁	Unity-gain bandwidth	V _I = 10 mV, C _L = 25 pF, See Figure 4	R _L = 2 kΩ,	25°C	3	3			MHz	
				0°C	3.2	3.2				
				70°C	2.6	2.7				
φ _m	Phase margin at unity gain	V _I = 10 mV, C _L = 25 pF, See Figure 4	R _L = 2 kΩ,	25°C	60°	63°				
				0°C	59°	63°				
				70°C	60°	63°				

[†] Full range is 0°C to 70°C.

[‡] For V_{CC}_± = ±5 V, V_I(PP) = ±1 V; for V_{CC}_± = ±15 V, V_I(PP) = ±5 V.

[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or non-testing of other parameters.

[¶] For V_{CC}_± = ±5 V, V_O(RMS) = 1 V; for V_{CC}_± = ±15 V, V_O(RMS) = 6 V.



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TL052I and TL052AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL052I, TL052AI						UNIT	
			V _{CC_±} = ± 5 V			V _{CC_±} = ± 15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	V _O = 0, V _{IC} = 0, R _S = 50 Ω	TL052I	25°C	0.73	3.5	0.65	1.5		mV	
			Full range		5.3		3.3			
		TL052AI	25°C	0.51	2.8	0.4	0.8			
			Full range		4.6		2.6			
αV _{IO}		TL052I	25°C to 85°C		7		6		μV/°C	
		TL052AI	25°C to 85°C		6		6	25		
Input offset voltage long-term drift§	V _O = 0, R _S = 50 Ω	V _{IC} = 0,	25°C	0.04		0.04		μV/mo		
I _{IO}	V _O = 0, See Figure 5	V _{IC} = 0,	25°C	4	100	5	100	pA		
			85°C	0.06	10	0.07	10	nA		
I _{IB}	V _O = 0, See Figure 5	V _{IC} = 0,	25°C	20	200	30	200	pA		
			85°C	0.6	20	0.7	20	nA		
V _{ICR}			25°C	-1 to 4	-2.3 to 5.6	-11 to 11	-12.3 to 15.6		V	
			Full range	-1 to 4	to 5.6	-11 to 11	-12.3 to 15.6			
			25°C	3	4.2	13	13.9			
			Full range	3		13				
V _{OM+}	R _L = 10 kΩ		25°C	2.5	3.8	11.5	12.7		V	
			Full range	2.5		11.5				
			25°C	-2.5	-3.5	-12	-13.2			
			Full range	-2.5		-12				
V _{OM-}	R _L = 10 kΩ		25°C	-2.3	-3.2	-11	-12		V	
			Full range	-2.3		-11				
			25°C	25	59	50	105			
			-40°C	30	74	60	145			
AVD	Large-signal differential voltage amplification¶	R _L = 2 kΩ	85°C	20	43	30	76		V/mV	
			25°C	10 ¹²		10 ¹²		Ω		
			25°C	10		12		pF		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	65	85	75	93		dB	
			-40°C	65	83	75	90			
			85°C	65	84	75	93			

† Full range is -40°C to 85°C.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At V_{CC_±} = ± 5 V, V_O = ± 2.3 V; at V_{CC_±} = ± 15 V, V_O = ± 10 V.



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TL052I and TL052AI electrical characteristics at specified free-air temperature (continued)

PARAMETER	TEST CONDITIONS	TA	TL052I, TL052AI						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
k _{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V _O = 0, R _S = 50 Ω	25°C	75	99	75	99	99	dB	
			-40°C	75	98	75	98	98		
			85°C	75	99	75	99	99		
I _{CC}	Supply current (two amplifiers)	V _O = 0, No load	25°C	4.6	5.6	4.8	5.6	5.6	mA	
			-40°C	4.5	6.4	4.7	6.4	6.4		
			85°C	4.4	6.4	4.6	6.4	6.4		
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100	25°C	120	120	120	120	120	dB	

TL052I and TL052AI operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL052I, TL052AI						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR +	Slew rate at unity gain [‡]	R _L = 2 kΩ, C _L = 100 pF, See Figure 1	25°C	17.8	20.7	9	20.7	20.7	V/μs	
			Full range			8		8		
			25°C	15.4	17.8	9	17.8	17.8		
			Full range			8		8		
t _r	Rise time	V _I (PP) = ±10 mV, R _L = 2 kΩ, C _L = 100 pF, See Figures 1 and 2	25°C	55	56	56	56	56	ns	
			-40°C	52	53	53	53	53		
t _f	Fall time		85°C	64	65	65	65	65		
			25°C	55	57	57	57	57		
			-40°C	51	53	53	53	53		
			85°C	64	65	65	65	65		
Overshoot factor			25°C	24%	19%	19%	19%	19%		
			-40°C	24%	19%	19%	19%	19%		
			85°C	24%	19%	19%	19%	19%		
V _n	Equivalent input noise voltage [§]	R _S = 20 Ω, See Figure 3	f = 10 Hz	25°C	71	71	71	71	pA/√Hz	
			f = 1 kHz	25°C	19	19	19	30		
V _N (PP)	Peak-to-peak equivalent input noise current	f = 10 Hz to 10 kHz	25°C		4	4	4	4	μV	
I _n	Equivalent input noise current	f = 1 kHz	25°C	0.01	0.01	0.01	0.01	0.01	pA/√Hz	
THD	Total harmonic distortion [¶]	R _S = 1 kΩ, f = 1 kHz	R _L = 2 kΩ,	25°C	0.003%	0.003%	0.003%	0.003%		
B ₁	Unity-gain bandwidth	V _I = 10 mV, C _L = 25 pF, See Figure 4	25°C	3	3	3	3	3	MHz	
			-40°C	3.5	3.6	3.6	3.6	3.6		
			85°C	2.5	2.6	2.6	2.6	2.6		
φ _m	Phase margin at unity gain	V _I = 10 mV, C _L = 25 pF, See Figure 4	25°C	60°	63°	63°	63°	63°		
			-40°C	58°	61°	61°	61°	61°		
			85°C	60°	63°	63°	63°	63°		

[†] Full range is -40°C to 85°C.

[‡] For V_{CC}_± = ±5 V, V_I(PP) = ±1 V; for V_{CC}_± = ±15 V, V_I(PP) = ±5 V.

[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or non-testing of other parameters.

[¶] For V_{CC}_± = ±5 V, V_O(RMS) = 1 V; for V_{CC}_± = ±15 V, V_O(RMS) = 6 V.



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**TL05x, TL05xA, TL05xY
ENHANCED-JFET LOW-OFFSET
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TL052M and TL052AM electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T_A^\dagger	TL052M, TL052AM						UNIT	
			$V_{CC\pm} = \pm 5 \text{ V}$			$V_{CC\pm} = \pm 15 \text{ V}$				
			MIN	Typ	MAX	MIN	Typ	MAX		
V_{IO} Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50 \Omega$	TL052M	25°C	0.73	3.5	0.65	1.5		mV	
			Full range		6.5		4.5			
		TL052AM	25°C	0.51	2.8	0.4	0.8			
			Full range		5.8		3.8			
αV_{IO} Temperature coefficient of input offset voltage		TL052M	25°C to 125°C		10		9		$\mu\text{V}/^\circ\text{C}$	
		TL052AM	25°C to 125°C		9		8			
V_{IO} Input offset voltage long- term drift‡	$V_O = 0$, $R_S = 50 \Omega$	$V_{IC} = 0$,	25°C	0.04		0.04		$\mu\text{V}/\text{mo}$		
I_{IO} Input offset current	$V_O = 0$, See Figure 5	$V_{IC} = 0$,	25°C	4	100	5	100	pA		
			125°C	1	20	2	20	nA		
I_{IB} Input bias current	$V_O = 0$, See Figure 5	$V_{IC} = 0$,	25°C	20	200	30	200	pA		
			125°C	10	50	20	50	nA		
V_{ICR} Common-mode input voltage range			25°C	-1	-2.3	-11	-12.3		V	
			to	to		to	to			
			4	5.6		11	15.6			
			Full range	-1		-11				
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10 \text{ k}\Omega$	25°C	3	4.2	13	13.9		V		
		Full range	3		13					
	$R_L = 2 \text{ k}\Omega$	25°C	2.5	3.8	11.5	12.7				
		Full range	2.5		11.5					
V_{OM-} Maximum negative peak output voltage swing	$R_L = 10 \text{ k}\Omega$	25°C	-2.5	-3.5	-12	-13.2		V		
		Full range	-2.5		-12					
	$R_L = 2 \text{ k}\Omega$	25°C	-2.3	-3.2	-11	-12				
		Full range	-2.3		-11					
A_{VD} Large-signal differential voltage amplification§	$R_L = 2 \text{ k}\Omega$	25°C	25	59	50	105		V/mV		
		-55°C	30	76	60	149				
		125°C	10	32	15	49				
r_i	Input resistance	25°C	1012		1012		Ω			
c_i	Input capacitance	25°C	10		12		pF			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$, $V_O = 0$, $R_S = 50 \Omega$	25°C	65	85	75	93	dB		
			-55°C	65	83	75	92			
			125°C	65	84	75	94			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_O = 0$, $R_S = 50 \Omega$	25°C	75	99	75	99	dB		
			-55°C	75	98	75	98			
			125°C	75	100	75	100			
I_{CC} Supply current (two amplifiers)		$V_O = 0$, No load	25°C	4.6	5.6	4.8	5.6	mA		
			-55°C	4.4	6.4	4.5	6.4			
			125°C	4.2	6.4	4.4	6.4			
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C	120		120		dB		

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For $V_{CC\pm} = \pm 5 \text{ V}$, $V_O = \pm 2.3 \text{ V}$; at $V_{CC\pm} = \pm 15 \text{ V}$, $V_O = \pm 10 \text{ V}$.



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TL052M and TL052AM operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL052M, TL052AM						UNIT	
			V _{CC} [‡] = ± 5 V			V _{CC} [‡] = ± 15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR + Positive slew rate at unity gain [‡]	RL = 2 kΩ, CL = 100 pF, See Figure 1	25°C	17.8	9	20.7				V/μs	
		Full range				8				
		25°C	15.4	9	17.8					
		Full range				8				
SR - Negative slew rate at unity gain [‡]		25°C	55	56					ns	
		-55°C	51	52						
		125°C	68	68						
		25°C	55	57						
t _r Rise time	V _I (PP) = ± 10 mV, RL = 2 kΩ, CL = 100 pF, See Figures 1 and 2	-55°C	51	52					ns	
		125°C	68	69						
t _f Fall time		25°C	55	57						
		-55°C	51	52						
		125°C	68	69						
		25°C	24%	19%						
Overshoot factor		-55°C	25%	19%						
		125°C	25%	19%						
		25°C	71	71						
V _n Equivalent input noise voltage [§]	RS = 20 Ω, See Figure 3	f = 10 Hz	19	19					nV/√Hz	
		f = 1 kHz	25°C	4	4					
V _{N(PP)} Peak-to-peak equivalent input noise current		f = 10 Hz to 10 kHz	25°C						μV	
I _n Equivalent input noise current	f = 1 kHz	25°C	0.01	0.01					pA/√Hz	
THD Total harmonic distortion [¶]	RS = 1 kΩ, f = 1 kHz	RL = 2 kΩ,	25°C	0.003%	0.003%					
B ₁ Unity-gain bandwidth	V _I = 10 mV, CL = 25 pF, See Figure 4	V _I = 10 mV, CL = 25 pF, See Figure 4	25°C	3	3				MHz	
		-55°C	3.6	3.7						
		125°C	2.3	2.4						
φ _m Phase margin at unity gain	V _I = 10 mV, CL = 25 pF, See Figure 4	V _I = 10 mV, CL = 25 pF, See Figure 4	25°C	60°	63°					
		-55°C	57°	61°						
		125°C	60°	63°						

[†] Full range is –55°C to 125°C.

[‡] For V_{CC}[±] = ± 5 V, V_I(PP) = ± 1 V; for V_{CC}[±] = ± 15 V, V_I(PP) = ± 5 V.

[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[¶] For V_{CC}[±] = ± 5 V, V_O(RMS) = 1 V; for V_{CC}[±] = ± 15 V, V_O(RMS) = 6 V.



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**TL05x, TL05xA, TL05xY
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TL052Y electrical characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL052Y						UNIT	
		$V_{CC\pm} = \pm 5 \text{ V}$			$V_{CC\pm} = \pm 15 \text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50 \Omega$	$V_{IC} = 0$,	0.73		0.65		mV	
	Input offset voltage long-term drift			0.04		0.04		$\mu\text{V}/\text{mo}$	
I_{IO}	Input offset current	$V_O = 0$, See Figure 5	$V_{IC} = 0$,	4		5		pA	
I_{IB}	Input bias current	$V_O = 0$, See Figure 5	$V_{IC} = 0$,	20		30		pA	
V_{ICR}	Common-mode input voltage range			-2.3 to 5.6		-12.3 to 15.6		V	
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10 \text{ k}\Omega$		4.2		13.9		V	
		$R_L = 2 \text{ k}\Omega$		3.8		12.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10 \text{ k}\Omega$		-3.5		-13.2		V	
		$R_L = 2 \text{ k}\Omega$		-3.2		-12			
A_{VD}	Large-signal differential voltage amplification [†]	$R_L = 2 \text{ k}\Omega$		59		105		V/mV	
r_i	Input resistance			10^{12}		10^{12}		Ω	
c_i	Input capacitance			10		12		pF	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$, $V_O = 0$,	$R_S = 50 \Omega$	85		93		dB	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_O = 0$,	$R_S = 50 \Omega$	99		99		dB	
I_{CC}	Supply current (two amplifiers)	$V_O = 0$,	No load	4.6		4.8		mA	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		120		120		dB	

[†] For $V_{CC\pm} = \pm 5 \text{ V}$, $V_O = \pm 2.3 \text{ V}$; at $V_{CC\pm} = \pm 15 \text{ V}$, $V_O = \pm 10 \text{ V}$.

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TL052Y operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL052Y						UNIT	
		$V_{CC\pm} = \pm 5 \text{ V}$			$V_{CC\pm} = \pm 15 \text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX		
SR +	Positive slew rate at unity gain†	$R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figure 1	17.8		20.7			$\text{V}/\mu\text{s}$	
SR -	Negative slew rate at unity gain†		15.4		17.8				
t_r	Rise time	$V_I(\text{PP}) = \pm 10 \text{ mV}$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figures 1 and 2	55		56			ns	
t_f	Fall time		55		57				
	Overshoot factor		24%		19%				
V_n	Equivalent input noise voltage‡	$R_S = 20 \Omega$, See Figure 3	f = 10 Hz	71	71			$\text{nV}/\sqrt{\text{Hz}}$	
	Peak-to-peak equivalent input noise current		f = 1 kHz	19	19				
			f = 10 Hz to 10 kHz	4	4				
I_n	Equivalent input noise current	f = 1 kHz		0.01	0.01			$\text{pA}/\sqrt{\text{Hz}}$	
THD	Total harmonic distortion§	$R_S = 1 \text{ k}\Omega$, $f = 1 \text{ kHz}$	$R_L = 2 \text{ k}\Omega$,		0.003%	0.003%			
B_1	Unity-gain bandwidth	$V_I = 10 \text{ mV}$, $C_L = 25 \text{ pF}$, See Figure 4	$R_L = 2 \text{ k}\Omega$,		3	3		MHz	
ϕ_m	Phase margin at unity gain	$V_I = 10 \text{ mV}$, $C_L = 25 \text{ pF}$, See Figure 4	$R_L = 2 \text{ k}\Omega$,		60°	63°			

† This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

‡ For $V_{CC\pm} = \pm 5 \text{ V}$, $V_I(\text{PP}) = \pm 1 \text{ V}$; for $V_{CC\pm} = \pm 15 \text{ V}$, $V_I(\text{PP}) = \pm 5 \text{ V}$.

§ For $V_{CC\pm} = \pm 5 \text{ V}$, $V_O(\text{RMS}) = 1 \text{ V}$; for $V_{CC\pm} = \pm 15 \text{ V}$, $V_O(\text{RMS}) = 6 \text{ V}$.

**TL05x, TL05xA, TL05xY
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TL054C and TL054AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL054C, TL054AC						UNIT	
			V _{CC} \pm ± 5 V			V _{CC} \pm ± 15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	TL054C	25°C	0.64	5.5	0.56	4	4	mV	
			Full range		7.7			6.2		
		TL054AC	25°C	0.57	3.5	0.5	1.5	1.5		
			Full range		5.7			3.7		
	Temperature coefficient of input offset voltage	TL054C	25°C to 70°C		25		23	23		
		TL054AC	25°C to 70°C		24		23	23		
αV _{IO}	Input offset voltage long-term drift‡		25°C		0.04		0.04	0.04	μV/mo	
	Input offset current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	4	100	5	100	pA	pA	
			70°C	0.02	1	0.025	1	nA		
	Input bias current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	20	200	30	200	pA	pA	
			70°C	0.15	4	0.2	4	nA		
V _{ICR}	Common-mode input voltage range	25°C	-1	-2.3		-11	-12.3		V	
			to	to		to	to			
			4	5.6		11	15.6			
			Full range	-1		-11				
		Full range	to	to		to	to			
			4			11				
V _{OM} +	Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	3	4.2	13	13.9		V	
			Full range	3		13				
		R _L = 2 kΩ	25°C	2.5	3.8	11.5	12.7			
			Full range	2.5		11.5				
V _{OM} -	Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	-2.5	-3.5	-12	-13.2		V	
			Full range	-2.5		-12				
		R _L = 2 kΩ	25°C	-2.3	-3.2	-11	-12			
			Full range	-2.3		-11				
AVD	Large-signal differential voltage amplification§	R _L = 2 kΩ	25°C	25	72	50	133		V/mV	
			0°C	30	88	60	173			
			70°C	20	57	30	85			
r _i	Input resistance		25°C		10 ¹²		10 ¹²		Ω	
c _i	Input capacitance		25°C		10		12		pF	
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, V _O = 0, R _S = 50 Ω	25°C	65	84	75	92		dB	
			0°C	65	84	75	92			
			70°C	65	84	75	93			
k _{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} \pm / \Delta V_{IO}$)	V _{CC} \pm ± 5 V to ± 15 V, V _O = 0, R _S = 50 Ω	25°C	75	99	75	99		dB	
			0°C	75	99	75	99			
			70°C	75	99	75	99			
I _{CC}	Supply current (four amplifiers)	V _O = 0, No load	25°C		8.1	11.2	8.4	11.2	mA	
			0°C		8.2	12.8	8.5	12.8		
			70°C		7.9	11.2	8.2	11.2		
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100	25°C		120		120		dB	

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For V_{CC} \pm ± 5 V, V_O = ± 2.3 V, at V_{CC} \pm ± 15 V, V_O = ± 10 V.B



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TL054C and TL054AC operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL054C, TL054C						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR+	Positive slew rate at unity gain RL = 2 kΩ, CL = 100 pF, See Figure 1 and Note 7	25°C	15.4	10	17.8				V/μs	
		0°C	15.7	8	17.9					
		70°C	14.4	8	17.5					
		25°C	13.9	10	15.9					
		0°C	14.3	8	16.1					
		70°C	13.3	8	15.5					
t _r	Rise time	25°C	55		56				ns	
		0°C	54		55					
		70°C	63		63					
		25°C	55		57					
		0°C	54		56					
		70°C	62		64					
t _f	Fall time	25°C	24%		19%					
		0°C	24%		19%					
		70°C	24%		19%					
		25°C	24%		19%					
		0°C	24%		19%					
		70°C	24%		19%					
V _n	Equivalent input noise voltage [§] RS = 20 Ω, See Figure 3	f = 10 Hz	25°C	75		75			nV/√Hz	
		f = 1 kHz	25°C	21		21	45			
		f = 10 Hz to 10 kHz	25°C	4		4				
		f = 1 kHz	25°C	0.01		0.01				
		RS = 1 kΩ, f = 1 kHz	25°C	0.003%		0.003%				
		V _I = 10 mV, CL = 25 pF, See Figure 4	25°C	2.7		2.7				
B ₁	Unity-gain bandwidth	0°C	3		3				MHz	
		70°C	2.4		2.4					
		25°C	61°		64°					
		0°C	60°		64°					
		70°C	61°		63°					
		V _I = 10 mV, CL = 25 pF, See Figure 4								
φ _m	Phase margin at unity gain									

[†] Full range is 0°C to 70°C.

[‡] For V_{CC}_± = ±5 V, V_I(PP) = ±1 V; for V_{CC}_± = ±15 V, V_I(PP) = ±5 V.

[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or non-testing of other parameters.

[¶] For V_{CC}_± = ±5 V, V_o(rms) = 1 V; for V_{CC}_± = ±15 V, V_o(rms) = 6 V.



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TL054I and TL054AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL054I, TL054AI						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	TL054I	25°C	0.64	5.5	0.56	4	7.3	mV	
			Full range		8.8					
	Temperature coefficient of input offset voltage	TL054AI	25°C	0.57	3.5	0.5	1.5	4.8		
			Full range		6.8					
		TL054I	25°C to 85°C		25		24			
		TL054AI	25°C to 85°C		25		23			
αV _{IO}	Input offset voltage long-term drift‡		25°C		0.04		0.04		μV/mo	
I _{IO}	Input offset current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	4	100	5	100	pA	nA	
			85°C	0.06	10	0.07	10			
I _{IB}	Input bias current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	20	200	30	200	pA	nA	
			85°C	0.6	20	0.7	20			
V _{ICR}	Common-mode input voltage range		25°C	-1	-2.3	-11	-12.3		V	
				to	to	to	to			
			Full range	4	5.6	11	15.6			
				-1		-11				
V _{OM} +	Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	3	4.2	13	13.9		V	
			Full range	3		13				
		R _L = 2 kΩ	25°C	2.5	3.8	11.5	12.7			
			Full range	2.5		11.5				
V _{OM} -	Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	-2.5	-3.5	-12	-13.2		V	
			Full range	-2.5		-12				
		R _L = 2 kΩ	25°C	-2.3	-3.2	-11	-12			
			Full range	-2.3		-11				
AVD	Large-signal differential voltage amplification§	R _L = 2 kΩ	25°C	25	72	50	133		V/mV	
			-40°C	30	101	60	212			
			85°C	20	50	30	70			
r _i	Input resistance		25°C		10 ¹²		10 ¹²		Ω	
c _i	Input capacitance		25°C		10		12		pF	
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} _{min} , V _O = 0, R _S = 50 Ω	25°C	65	84	75	92		dB	
			-40°C	65	83	75	92			
			85°C	65	84	75	93			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} _± /ΔV _{IO})	V _{CC} _± = ±5 V to ±15 V, V _O = 0, R _S = 50 Ω	25°C	75	99	75	99		dB	
			-40°C	75	98	75	99			
			85°C	75	99	75	99			
I _{CC}	Supply current (four amplifiers)	V _O = 0, No load	25°C		8.1	11.2	8.4	11.2	mA	
			-40°C		7.9	12.8	8.2	12.8		
			85°C		7.6	11.2	7.9	11.2		
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100	25°C		120		120		dB	

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For V_{CC}_± = ±5 V, V_O = ±2.3 V, at V_{CC}_± = ±15 V, V_O = ±10 V.



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TL054I and TL054AI operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL054I, TL054AI						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR+	Positive slew rate at unity gain R _L = 2 kΩ, C _L = 100 pF, See Figure 1	25°C	15.4			10	17.8		V/μs	
		-40°C	16.4			8	18			
		85°C	14			8	17.3			
		25°C	13.9			10	15.9			
		-40°C	14.7			8	16.1			
		85°C	13			8	15.3			
t _r	Rise time	25°C	55			56			ns	
		-40°C	52			53				
t _f	Fall time V _I (PP) = ±10 mV, R _L = 2 kΩ, C _L = 100 pF, See Figures 1 and 2	85°C	64			65				
		25°C	55			57				
		-40°C	51			53				
		85°C	64			65				
		25°C	24%			19%				
		-40°C	24%			19%				
Overshoot factor		85°C	24%			19%				
		25°C	75			75				
		25°C	21			21	45			
V _n	Equivalent input noise voltage [§] R _S = 20 Ω, See Figure 3	f = 10 Hz							nV/√Hz	
V _N (PP)		f = 1 kHz								
I _n	Equivalent input noise current	f = 1 kHz	25°C	0.01		0.01			pA/√Hz	
THD	Total harmonic distortion [¶]	R _S = 1 kΩ, f = 1 kHz	R _L = 2 kΩ,	25°C	0.003%		0.003%			
B ₁	Unity-gain bandwidth	V _I = 10 mV, C _L = 25 pF, See Figure 4	R _L = 2 kΩ,	25°C	2.7		2.7	MHz		
				-40°C	3.3		3.3			
				85°C	2.3		2.4			
φ _m	Phase margin at unity gain	V _I = 10 mV, C _L = 25 pF, See Figure 4	R _L = 2 kΩ,	25°C	61°		64°			
				-40°C	59°		62°			
				85°C	61°		64°			

[†] Full range is -40°C to 85°C.

[‡] For V_{CC}_± = ±5 V, V_I(PP) = ±1 V; for V_{CC}_± = ±15 V, V_I(PP) = ±5 V.

[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[¶] For V_{CC}_± = ±5 V, V_O(rms) = 1 V; for V_{CC}_± = ±15 V, V_O(rms) = 6 V.



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TL054M and TL054AM electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A [†]	TL054M, TL054AM						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	TL054M	25°C	0.64	5.5	0.56	4	9	mV	
			Full range		10.5			6.5		
		TL054AM	25°C	0.57	3.5	0.5	1.5			
			Full range		8.5					
	Temperature coefficient of input offset voltage	TL054M	25°C to 85°C		21		20		μV/°C	
			25°C to 85°C		21		20			
α _{VIO}	Input offset voltage long-term drift‡		25°C		0.04		0.04		μV/mo	
I _{IO}	Input offset current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	4	100	5	100	pA		
			125°C	1	20	2	20	nA		
I _{IB}	Input bias current	V _O = 0, V _{IC} = 0, See Figure 5	25°C	20	200	30	200	pA		
			125°C	10	50	20	50	nA		
V _{ICR}	Common-mode input voltage range		25°C	-1	-2.3	-11	-12.3		V	
				to	to	to	to			
			Full range	4	5.6	11	15.6			
				-1		-11				
V _{OM} +	Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	3	4.2	13	13.9		V	
			Full range	3		13				
		R _L = 2 kΩ	25°C	2.5	3.8	11.5	12.7			
			Full range	2.5		11.5				
V _{OM} -	Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	-2.5	-3.5	-12	-13.2		V	
			Full range	-2.5		-12				
		R _L = 2 kΩ	25°C	-2.3	-3.2	-11	-12			
			Full range	-2.3		-11				
AVD	Large-signal differential voltage amplification§	R _L = 2 kΩ	25°C	25	72	50	133		V/mV	
			-55°C	30	99	60	209			
			125°C	10	35	15	35			
r _i	Input resistance		25°C		10 ¹²		10 ¹²		Ω	
c _i	Input capacitance		25°C		10		12		pF	
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω	25°C	65	84	75	92		dB	
			-55°C	65	83	75	92			
			125°C	65	84	75	93			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} _± /ΔV _{IO})	V _{CC} _± = ±5 V to ±15 V, V _O = 0, R _S = 50 Ω	25°C	75	99	75	99		dB	
			-40°C	75	98	75	98			
			85°C	75	100	75	100			
I _{CC}	Supply current (four amplifiers)	V _O = 0, No load	25°C		8.1	11.2	8.4	11.2	mA	
			-55°C		7.8	12.8	8.1	12.8		
			125°C		7.1	11.2	7.5	11.2		
V _{O1} /V _{O2}	Crosstalk attenuation	AVD = 100	25°C		120		120		dB	

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For V_{CC}_± = ±5 V, V_O = ±2.3 V, at V_{CC}_± = ±15 V, V_O = ±10 V.



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TL054M and TL054AM operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	TA [†]	TL054M, TL054AM						UNIT	
			V _{CC} _± = ±5 V			V _{CC} _± = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR+	Positive slew rate at unity gain	RL = 2 kΩ, CL = 100 pF, See Figure 1	25°C	15.4		10	17.8		V/μs	
			-55°C	16.7			18.3			
			125°C	12.9			16.7			
			25°C	13.9		10	15.9			
			-55°C	14.7			16.3			
			125°C	12.2			14.5			
t _r	Rise time	VI(PP) = ±10 mV, RL = 2 kΩ, CL = 100 pF, See Figures 1 and 2	25°C	55		56			ns	
			-55°C	51		52				
			125°C	68		68				
			25°C	55		57				
			-55°C	51		52				
			125°C	68		69				
t _f	Fall time	VI(PP) = ±10 mV, RL = 2 kΩ, CL = 100 pF, See Figures 1 and 2	25°C	24%		19%				
			-55°C	25%		19%				
			125°C	25%		19%				
			25°C	75		75				
			25°C	21		21	45			
			25°C	4		4				
V _n	Equivalent input noise voltage [§]	RS = 20 Ω, See Figure 3	f = 10 Hz	25°C	0.01	0.01			nV/√Hz	
V _{N(PP)}	Peak-to-peak equivalent input noise voltage		f = 1 kHz	25°C					μV	
I _n	Equivalent input noise current		f = 1 kHz	25°C					pA/√Hz	
THD	Total harmonic distortion [¶]	RS = 1 kΩ, f = 1 kHz	RL = 2 kΩ,	25°C	0.003%	0.003%				
B ₁	Unity-gain bandwidth	VI = 10 mV, CL = 25 pF, See Figure 4	RL = 2 kΩ,	25°C	2.7	2.7			MHz	
			CL = 25 pF,	-55°C	3.4	3.4				
			See Figure 4	125°C	2.1	2.1				
φ _m	Phase margin at unity gain	VI = 10 mV, CL = 25 pF, See Figure 4	RL = 2 kΩ,	25°C	61°	64°				
			CL = 25 pF,	-55°C	58°	62°				
			See Figure 4	125°C	60°	64°				

[†] Full range is -55°C to 125°C.

[‡] For V_{CC}_± = ±5 V, VI(PP) = ±1 V; for V_{CC}_± = ±15 V, VI(PP) = ±5 V.

[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[¶] For V_{CC}_± = ±5 V, V_{0rms} = 1 V; for V_{CC}_± = ±15 V, V_{0rms} = 6 V.



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TL054Y electrical characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL054Y						UNIT	
		$V_{CC \pm} = \pm 5 \text{ V}$			$V_{CC \pm} = \pm 15 \text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	$V_O = 0, V_{IC} = 0, R_S = 50 \Omega$		0.64			0.56		mV	
I_{IO}	$V_O = 0, V_{IC} = 0,$ See Figure 5		4			5		pA	
I_{IB}	$V_O = 0, V_{IC} = 0,$ See Figure 5		20			30		pA	
V_{ICR}	Common-mode input voltage range		-2.3 to 5.6			-12.3 to 15.6		V	
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10 \text{ k}\Omega$	4.2			13.9		V	
		$R_L = 2 \text{ k}\Omega$	3.8			12.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10 \text{ k}\Omega$	-3.5			-13.2		V	
		$R_L = 2 \text{ k}\Omega$	-3.2			-12			
AVD	Large-signal differential voltage amplification†	$R_L = 2 \text{ k}\Omega$	72			133		V/mV	
r_i	Input resistance		10^{12}			10^{12}		Ω	
c_i	Input capacitance		10			12		pF	
$CMRR$	Common-mode rejection ratio	$V_{IC} = V_{ICR\min}, V_O = 0, R_S = 50 \Omega$	84			92		dB	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC \pm} / \Delta V_{IO}$)	$V_{CC \pm} = \pm 5 \text{ V to } \pm 15 \text{ V}, V_O = 0, R_S = 50 \Omega$	99			99		dB	
I_{CC}	Supply current (four amplifiers)	$V_O = 0, \text{ No load}$	8.1			8.4		mA	
V_{O1}/V_{O2}	Crosstalk attenuation	$AVD = 100$	120			120		dB	

† For $V_{CC \pm} = \pm 5 \text{ V}, V_O = \pm 2.3 \text{ V}$, at $V_{CC \pm} = \pm 15 \text{ V}, V_O = \pm 10 \text{ V}$.

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TL054Y operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL054Y						UNIT							
		$V_{CC \pm} = \pm 5 \text{ V}$			$V_{CC \pm} = \pm 15 \text{ V}$										
		MIN	TYP	MAX	MIN	TYP	MAX								
SR+	Positive slew rate at unity gain [†]	$R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figure 1	15.4	17.8											
SR-	Negative slew rate at unity gain														
t_r	Rise time	$V_I(\text{PP}) = \pm 10 \text{ mV}$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figures 1 and 2	55	56				ns							
t_f	Fall time		55	57											
Overshoot factor			24%	19%											
V_n	Equivalent input noise voltage [‡]	$R_S = 20 \Omega$, See Figure 3	f = 10 Hz	75	75			nV/ $\sqrt{\text{Hz}}$							
			f = 1 kHz	21	21										
$V_{N(\text{PP})}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	4	4			μV							
I_n	Equivalent input noise current		f = 1 kHz	0.01	0.01										
THD	Total harmonic distortion [§]	$R_S = 1 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$, f = 1 kHz		0.003%	0.003%										
B_1	Unity-gain bandwidth	$V_I = 10 \text{ mV}$, $R_L = 2 \text{ k}\Omega$, $C_L = 25 \text{ pF}$, See Figure 4		2.7	2.7			MHz							
ϕ_m	Phase margin at unity gain	$V_I = 10 \text{ mV}$, $R_L = 2 \text{ k}\Omega$, $C_L = 25 \text{ pF}$, See Figure 4		61°	64°										

[†] For $V_{CC \pm} = \pm 5 \text{ V}$, $V_I(\text{PP}) = \pm 1 \text{ V}$; for $V_{CC \pm} = \pm 15 \text{ V}$, $V_I(\text{PP}) = \pm 5 \text{ V}$.

[‡] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[§] For $V_{CC \pm} = \pm 5 \text{ V}$, $V_o(\text{rms}) = 1 \text{ V}$; for $V_{CC \pm} = \pm 15 \text{ V}$, $V_o(\text{rms}) = 6 \text{ V}$.

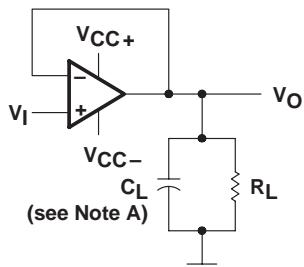


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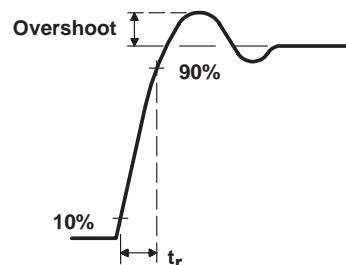
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PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

**Figure 1 . Slew Rate, Rise/Fall Time,
and Overshoot Test Circuit**



**Figure 2 . Rise Time and Overshoot
Waveform**

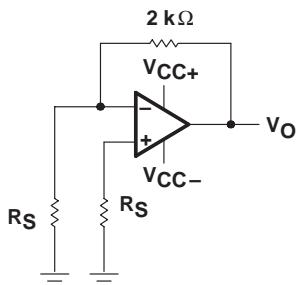
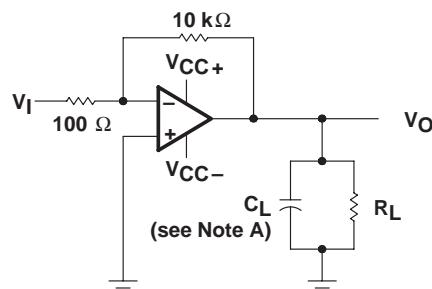


Figure 3 . Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.
**Figure 4 . Unity-Gain Bandwidth and
Phase-Margin Test Circuit**

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp-bias-current level typical of the TL05x and TL05xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample tested at $f = 1$ kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

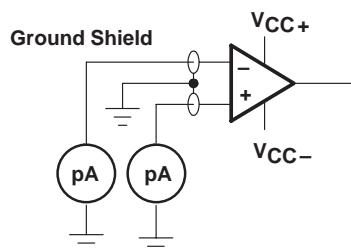


Figure 5. Input-Bias and Offset-Current Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V_{IO}	Input offset voltage	Distribution 6 – 11
αV_{IO}	Temperature coefficient of input offset voltage	Distribution 12, 13, 14
I_{IB}	Input bias current	vs Common-mode input voltage 15 vs Free-air temperature 16
I_{IO}	Input offset current	vs Free-air temperature 16
V_{IC}	Common-mode input voltage range limits	vs Supply voltage 17 vs Free-air temperature 18
V_O	Output voltage	vs Differential input voltage 19, 20
V_{OM}	Maximum peak output voltage	vs Supply voltage 21 vs Output current 25, 26 vs Free-air temperature 27, 28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency 22, 23, 24
A_{VD}	Large-signal differential voltage amplification	vs Load resistance 29 vs Frequency 30 vs Free-air temperature 31, 32, 33
$CMRR$	Common-mode rejection ratio	vs Frequency 34, 35 vs Free-air temperature 36
z_o	Output impedance	vs Frequency 37
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature 38
I_{OS}	Short-circuit output current	vs Supply voltage 39 vs Time 40 vs Free-air temperature 41
I_{CC}	Supply current	vs Supply voltage 42, 43, 44 vs Free-air temperature 45, 46, 47
SR	Slew rate	vs Load resistance 48 – 53 vs Free-air temperature 54 – 59
	Overshoot factor	vs Load capacitance 60
V_n	Equivalent input noise voltage	vs Frequency 61, 62
THD	Total harmonic distortion	vs Frequency 63
B_1	Unity-gain bandwidth	vs Supply voltage 64, 65, 66 vs Free-air temperature 67, 68, 69
ϕ_m	Phase margin	vs Supply voltage 70, 71, 72 vs Load capacitance 73, 74, 75 vs Free-air temperature 76, 77, 78
	Phase shift	vs Frequency 30
	Voltage-follower small-signal pulse response	vs Time 79
	Voltage-follower large-signal pulse response	vs Time 80

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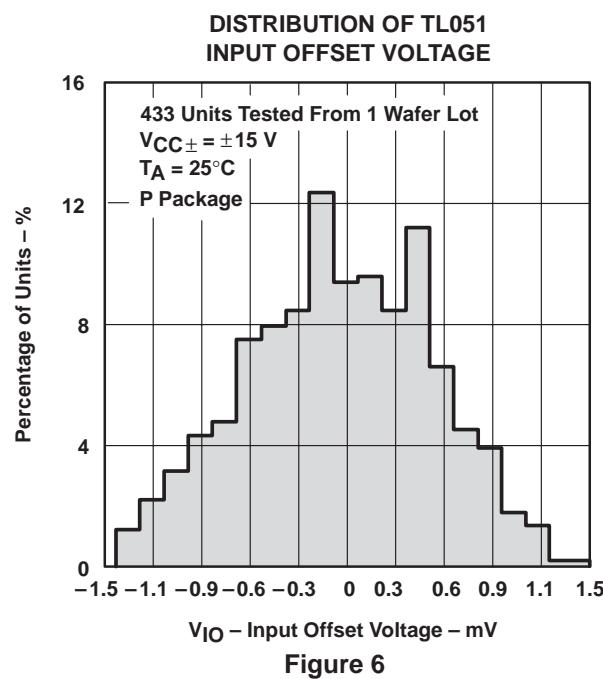


Figure 6

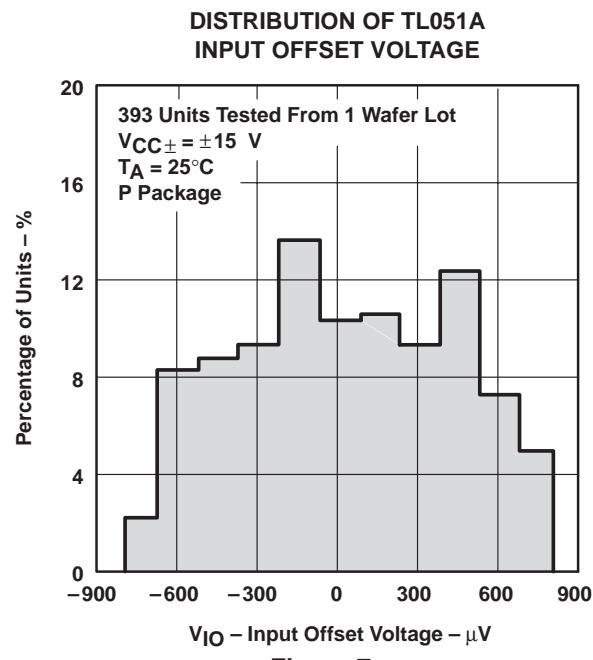


Figure 7

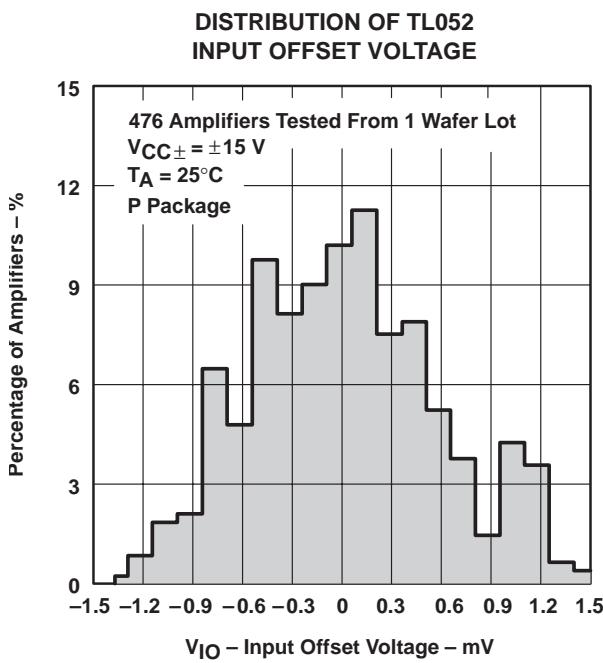


Figure 8

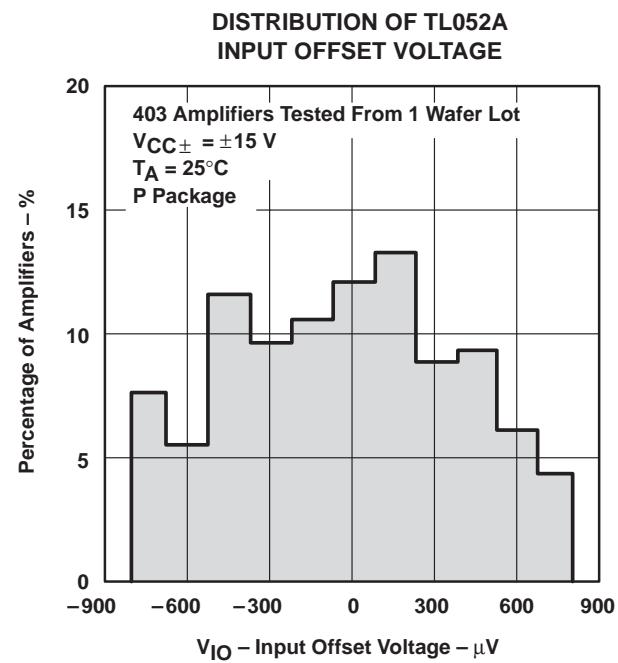


Figure 9

TYPICAL CHARACTERISTICS

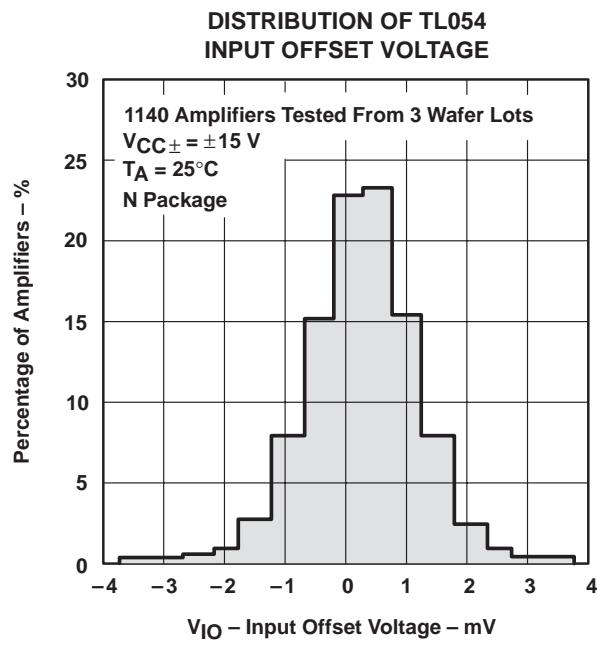


Figure 10

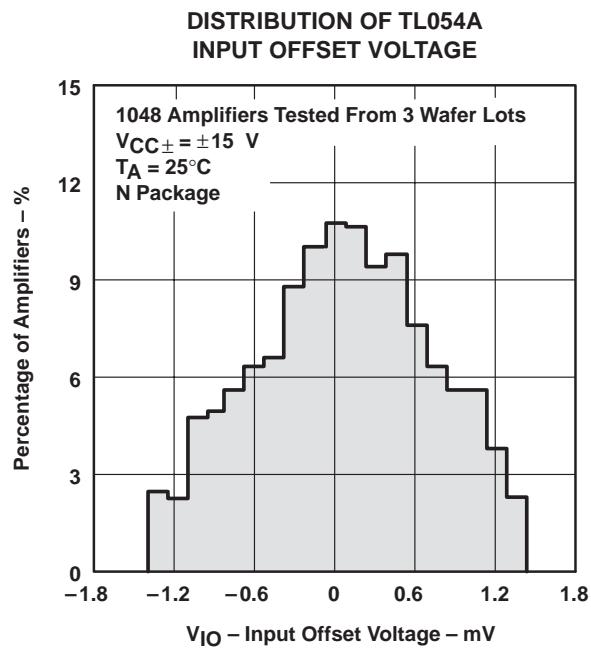


Figure 11

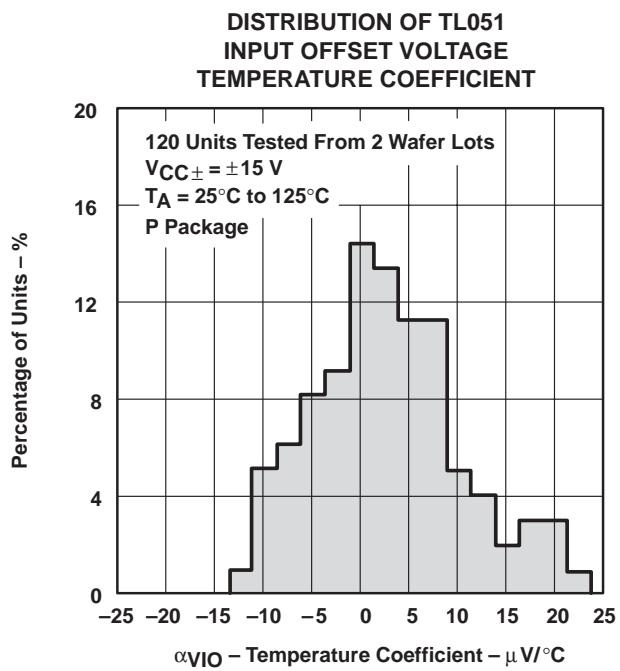


Figure 12

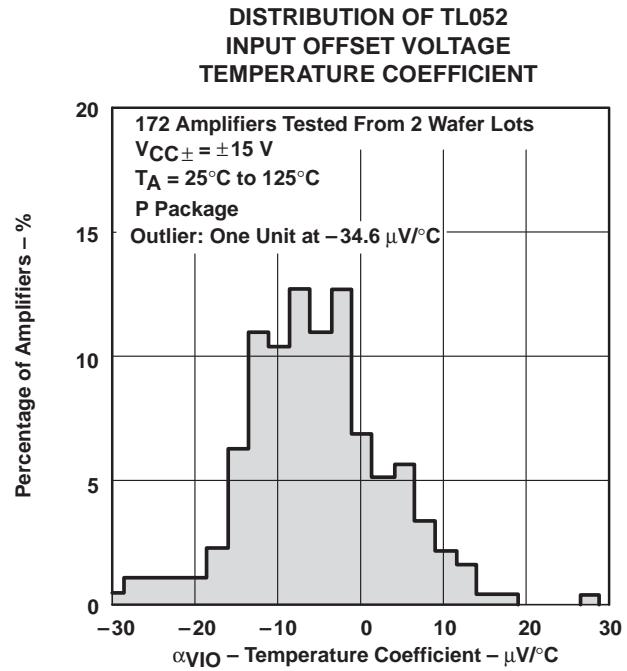
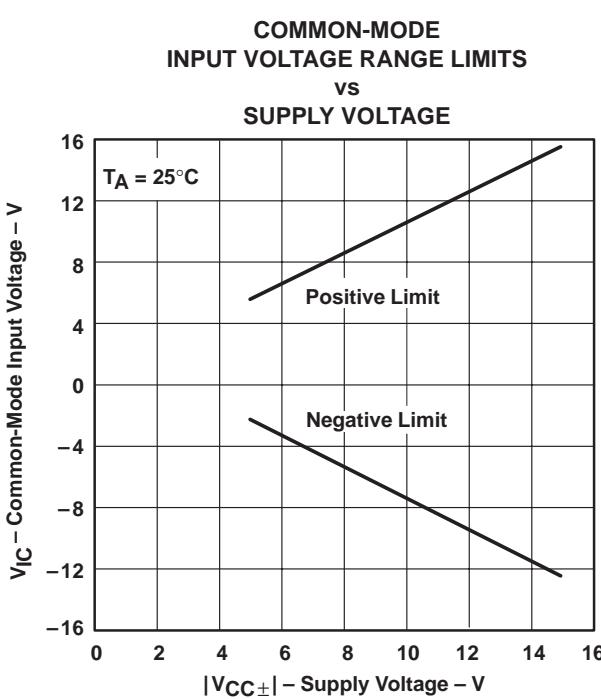
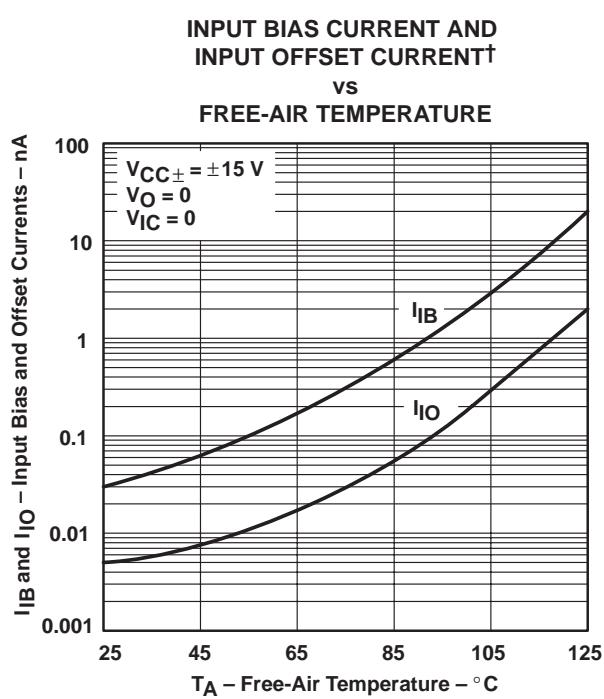
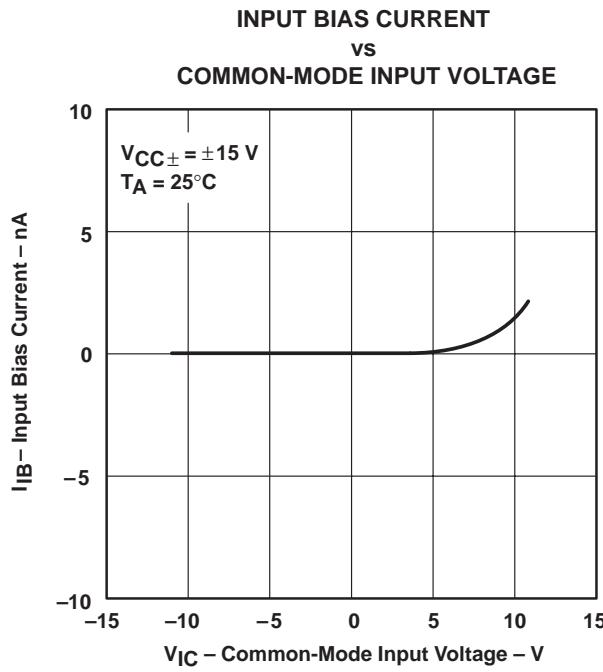
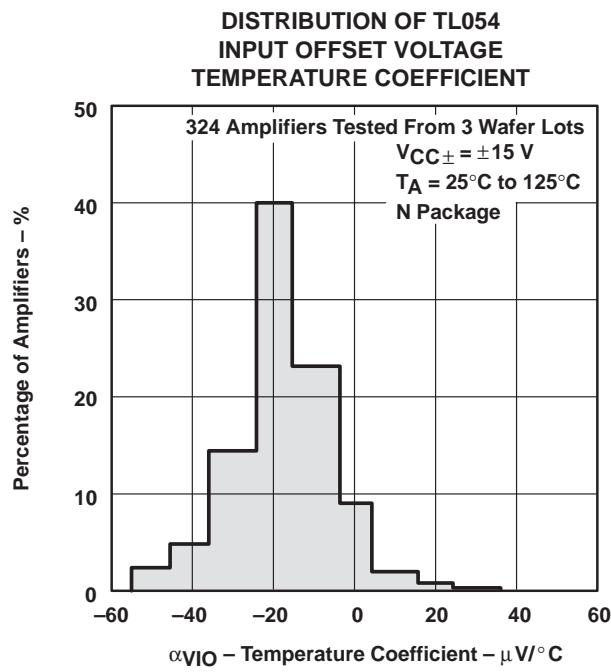


Figure 13

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TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

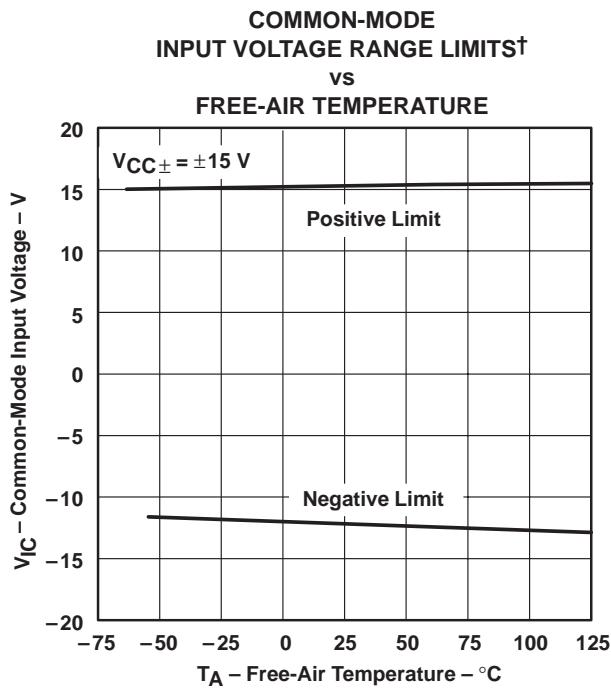


Figure 18

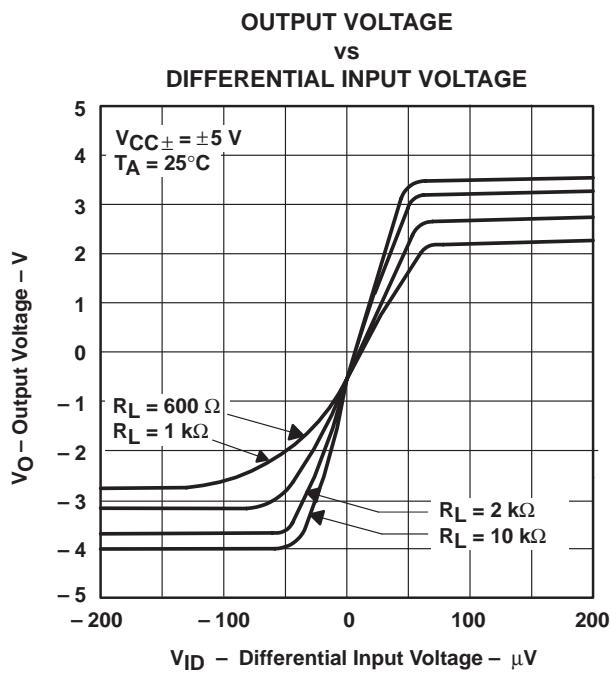


Figure 19

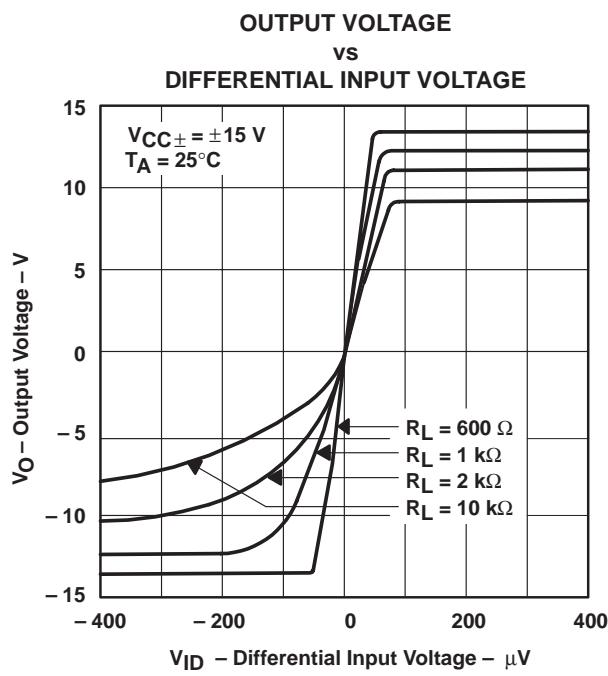


Figure 20

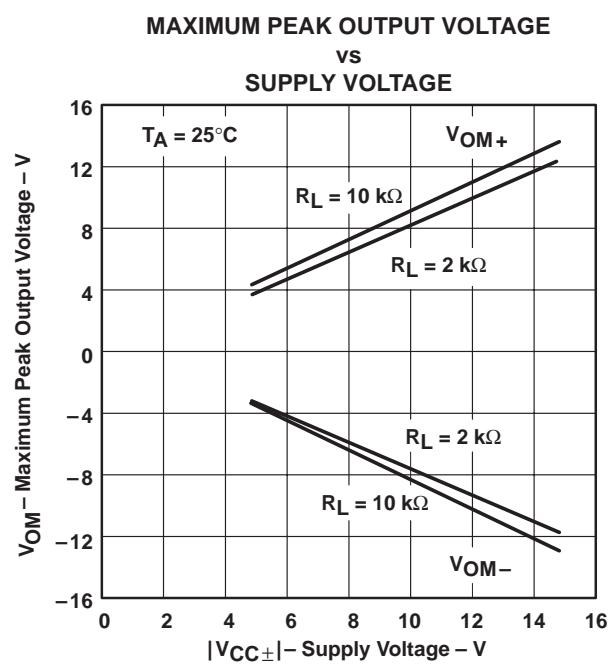


Figure 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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OPERATIONAL AMPLIFIERS**

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TYPICAL CHARACTERISTICS

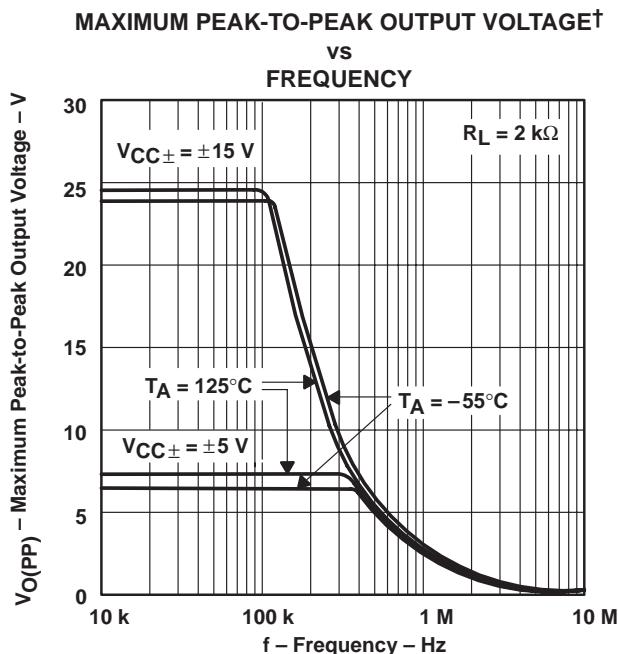


Figure 22

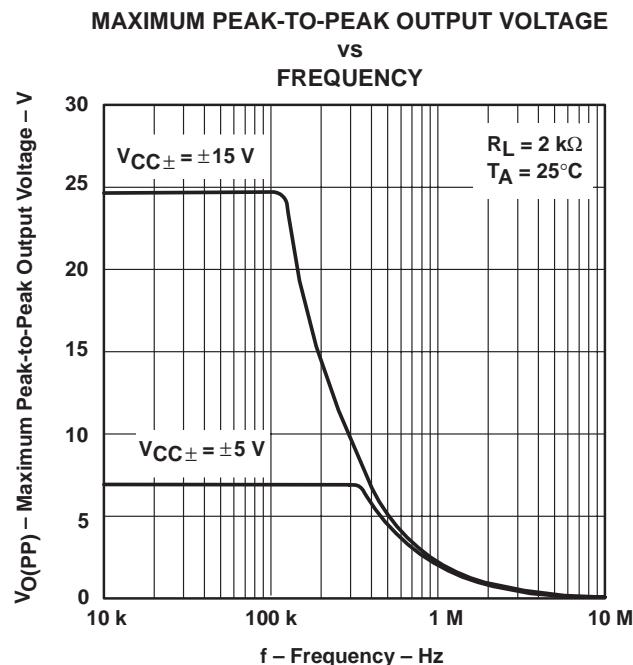


Figure 23

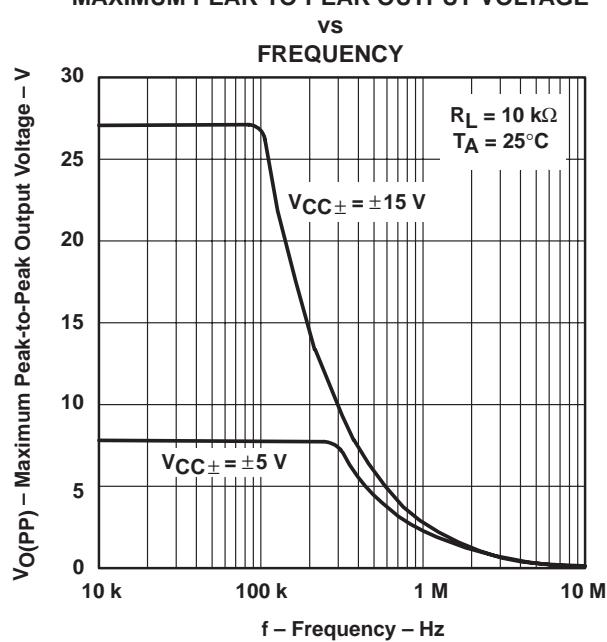


Figure 24

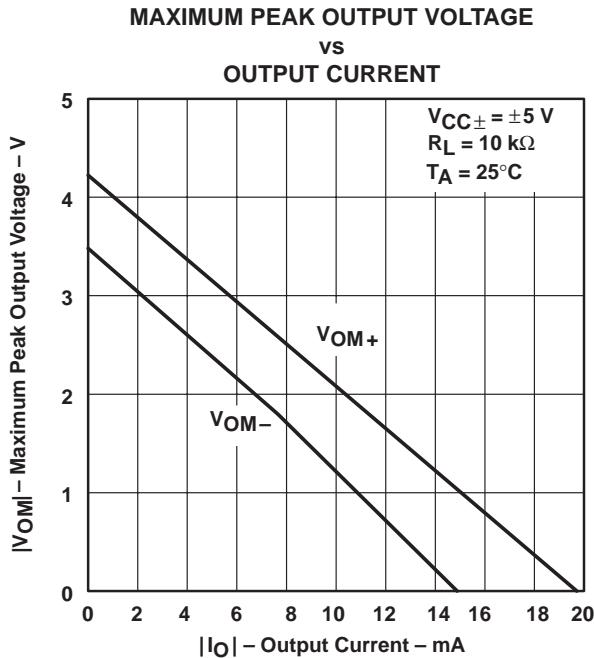


Figure 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

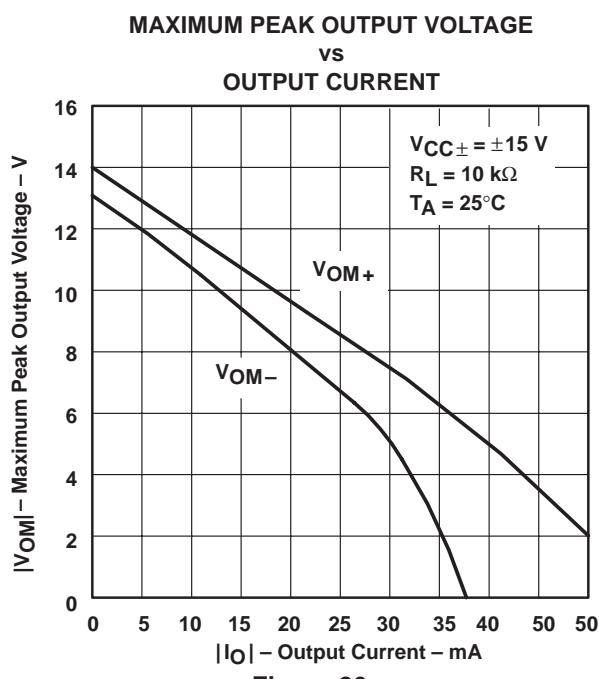


Figure 26

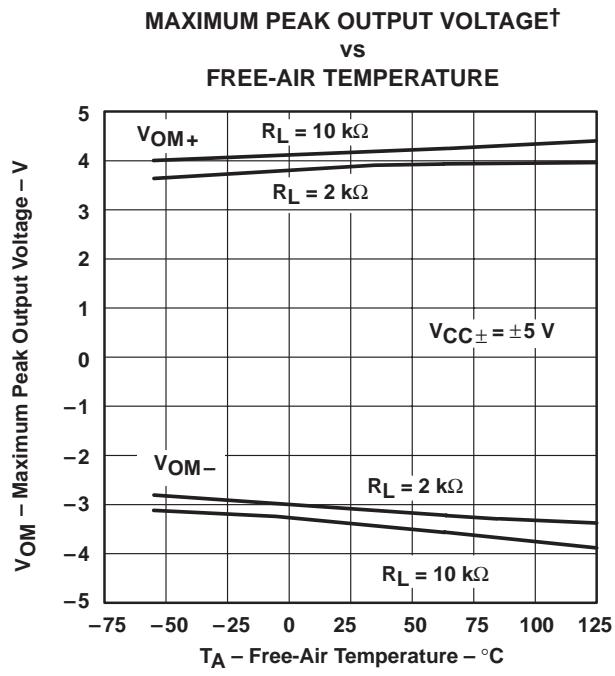


Figure 27

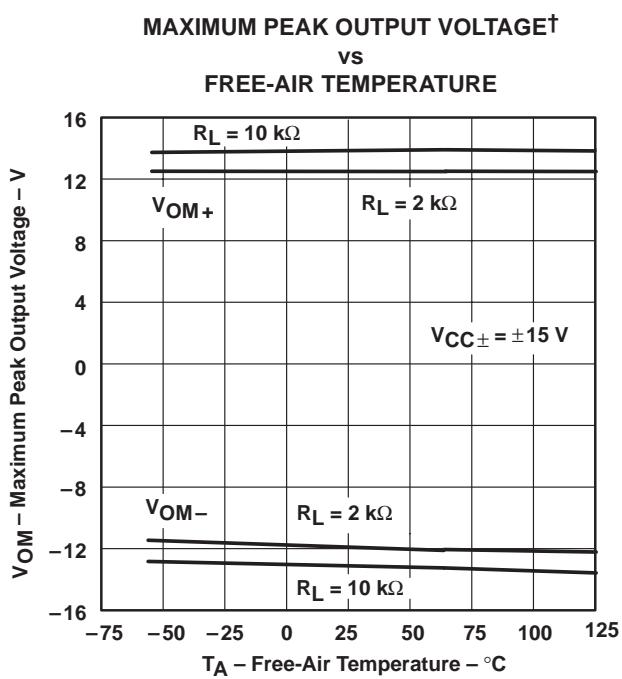


Figure 28

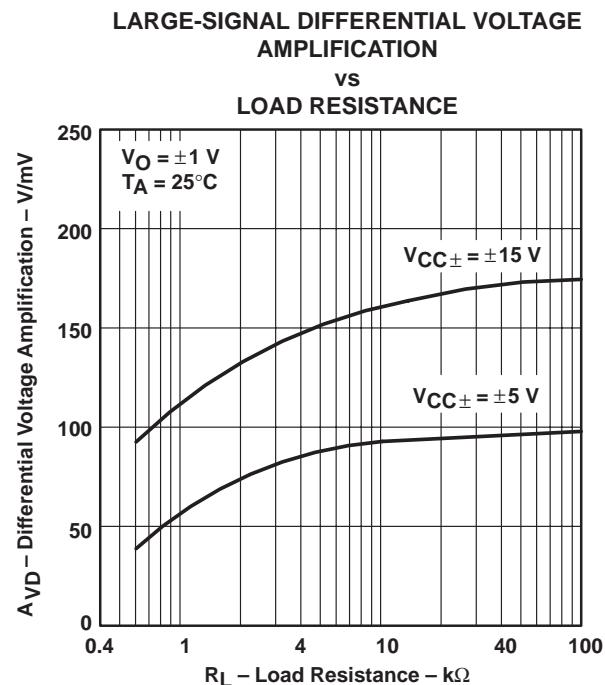


Figure 29

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL05x, TL05xA, TL05xY
ENHANCED-JFET LOW-OFFSET
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TYPICAL CHARACTERISTICS

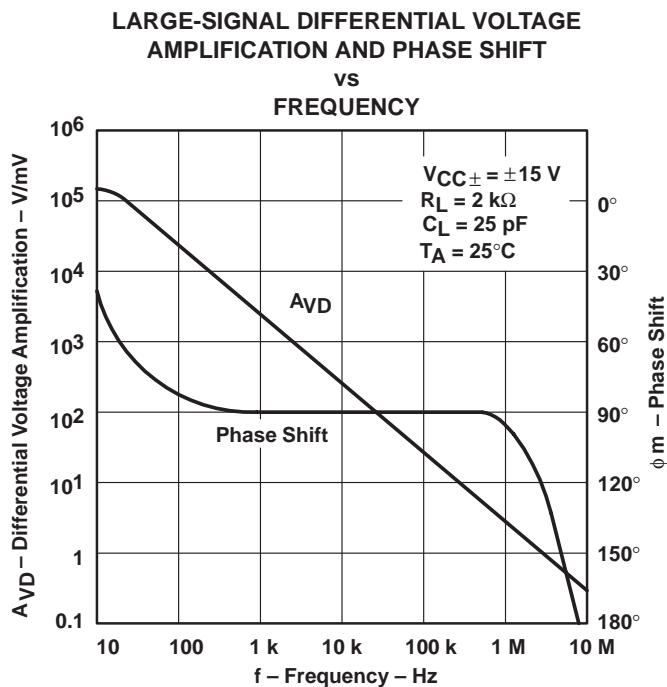
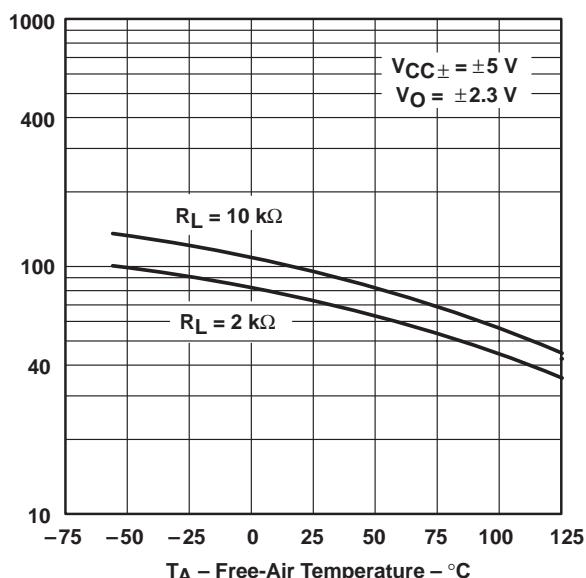
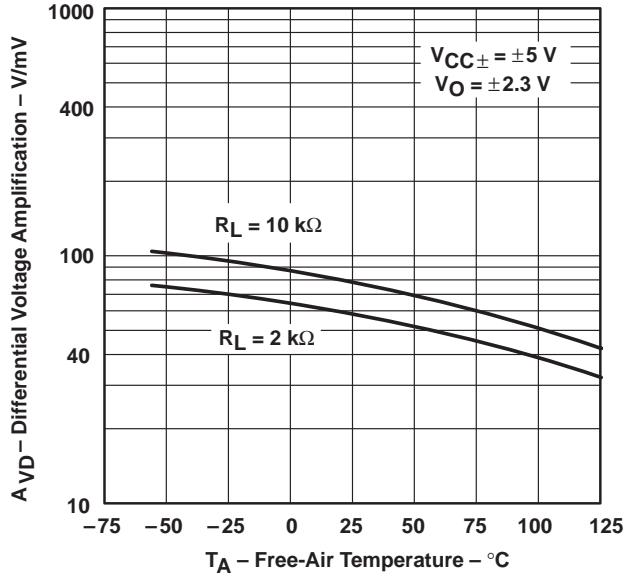


Figure 30



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

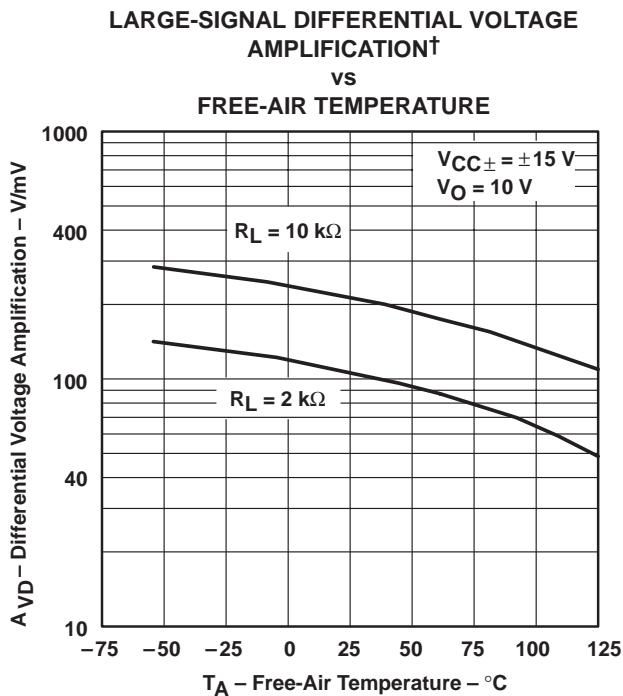


Figure 33

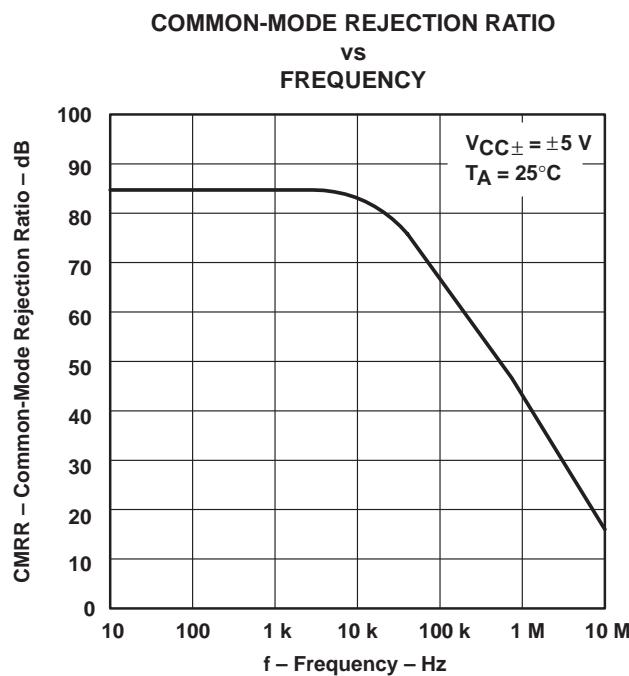


Figure 34

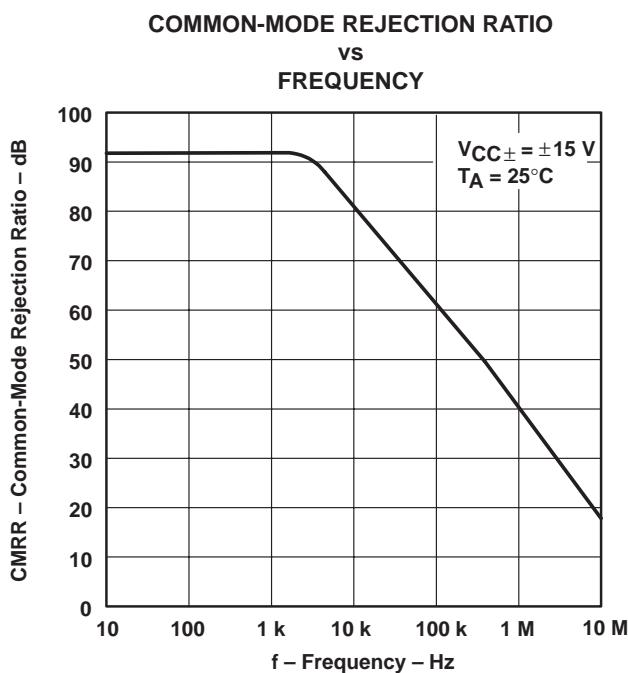


Figure 35

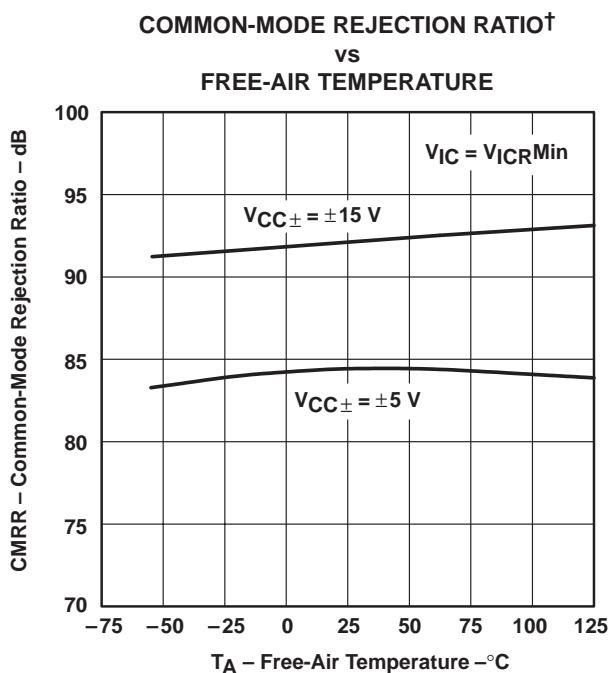


Figure 36

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL05x, TL05xA, TL05xY
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TYPICAL CHARACTERISTICS

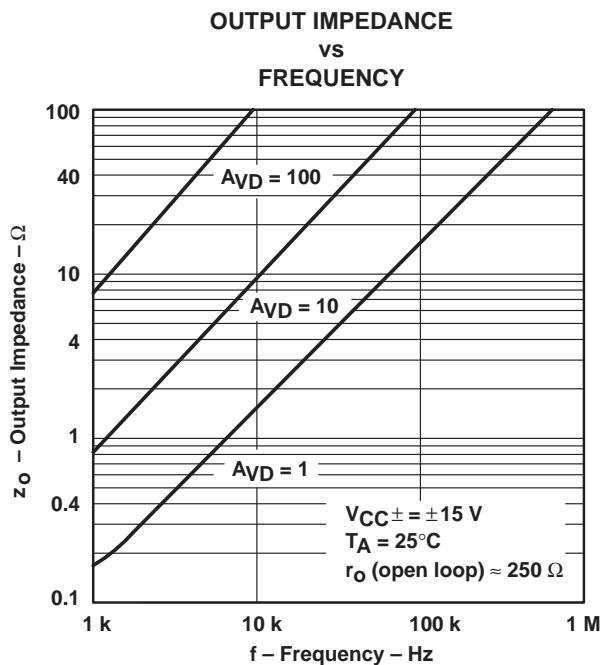


Figure 37

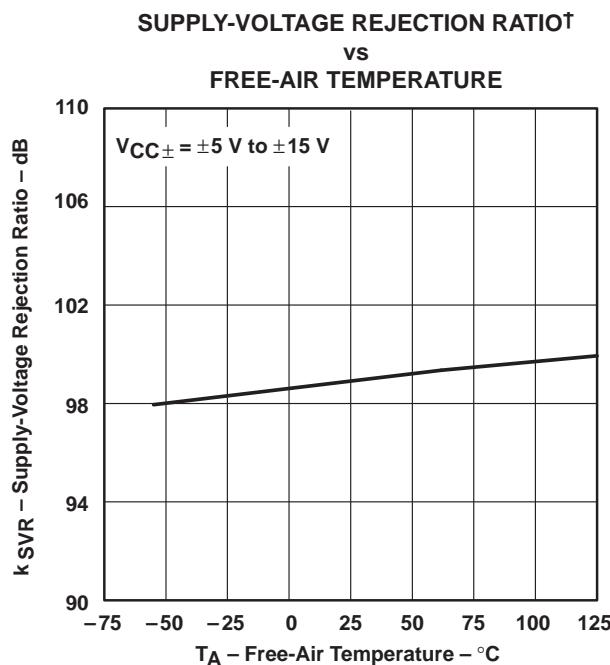


Figure 38

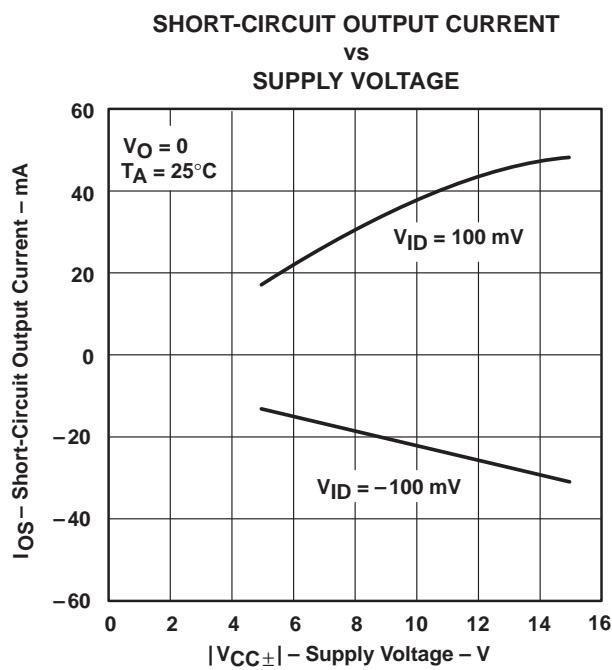


Figure 39

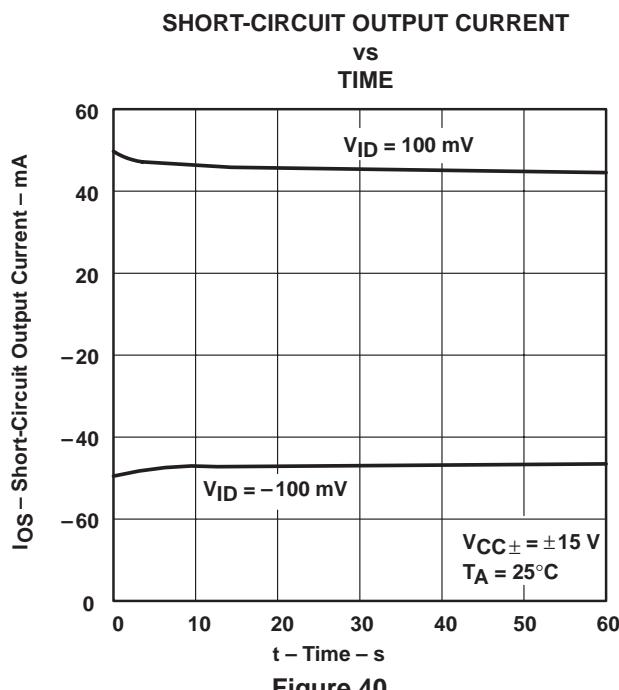


Figure 40

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

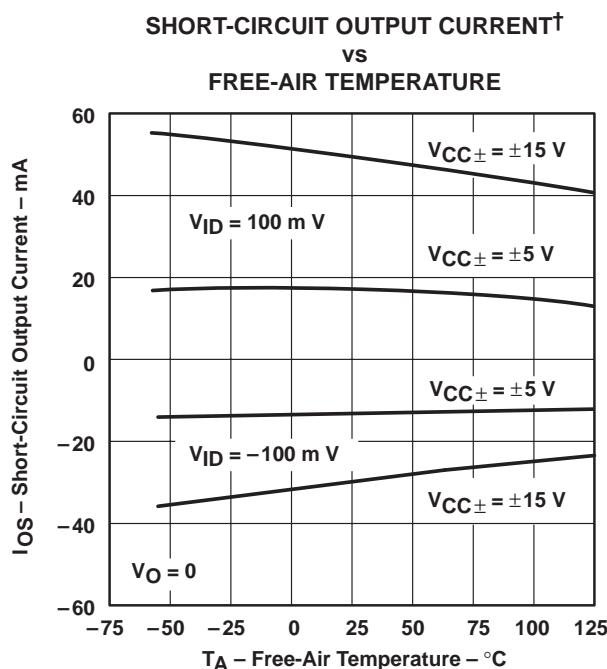


Figure 41

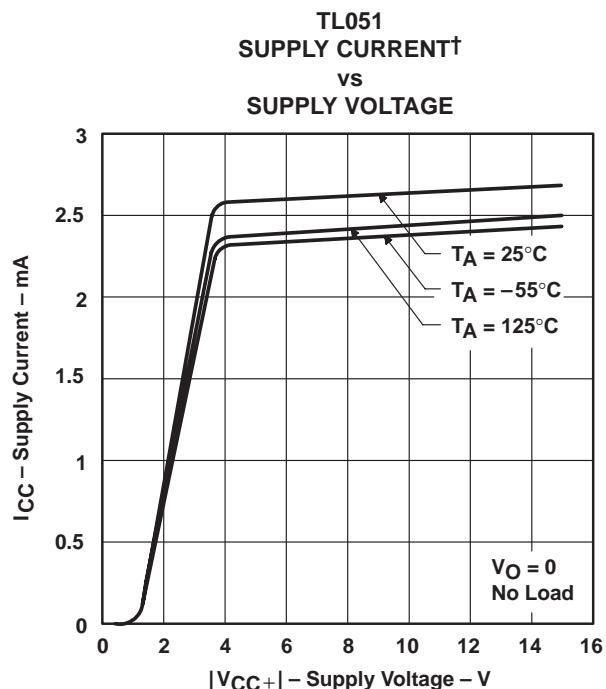


Figure 42

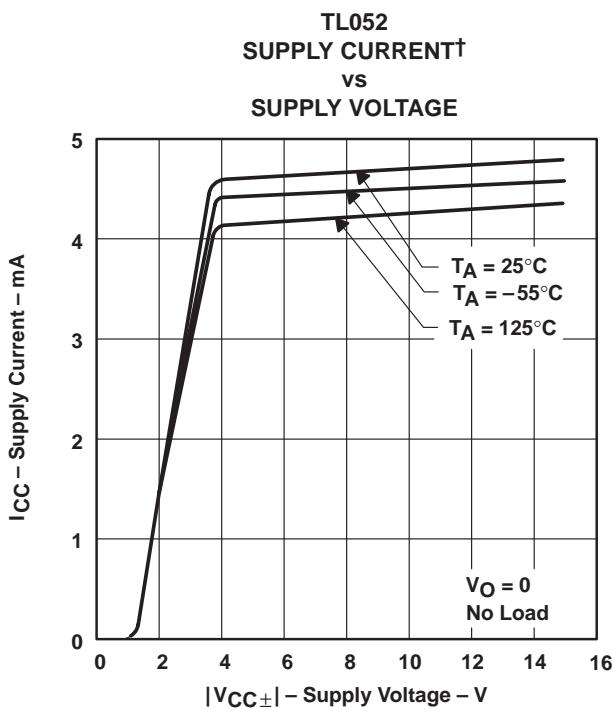


Figure 43

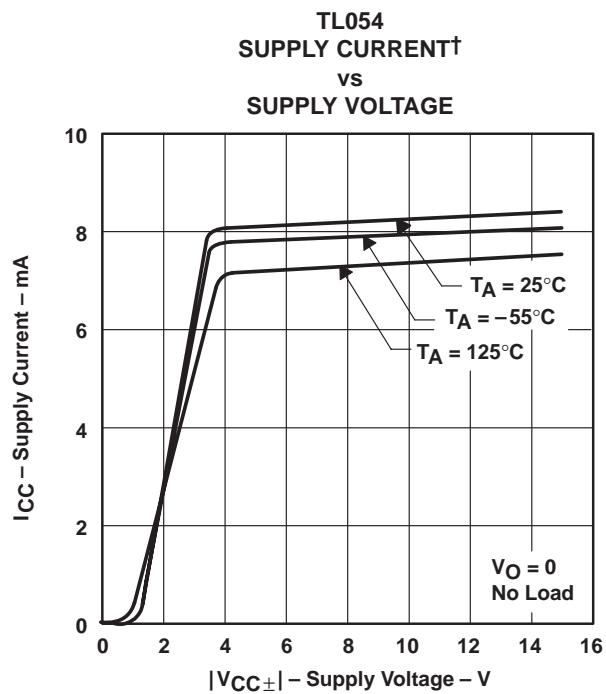


Figure 44

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL05x, TL05xA, TL05xY
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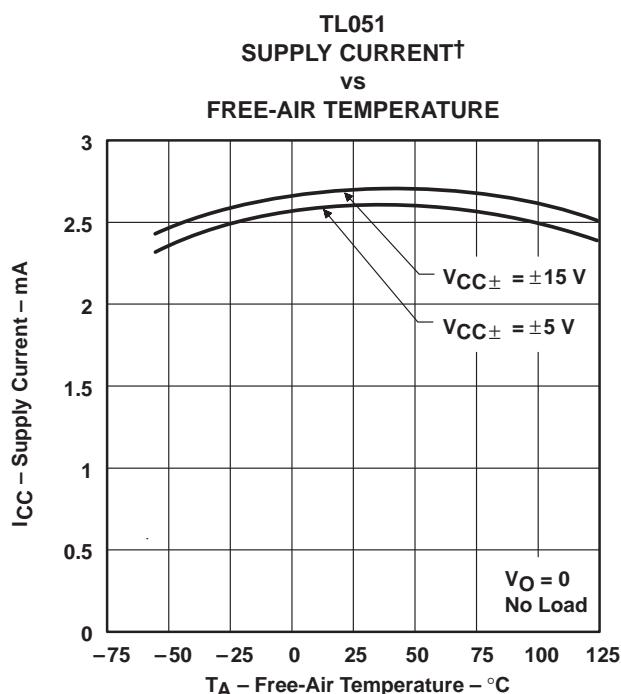


Figure 45

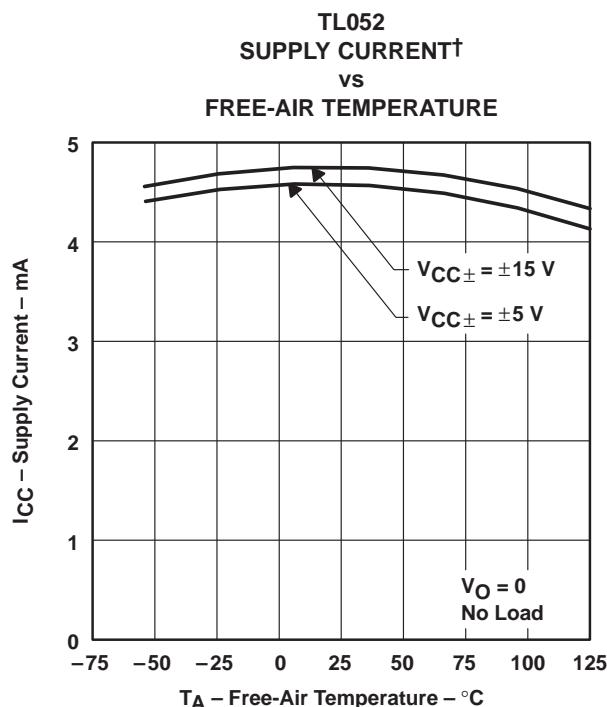


Figure 46

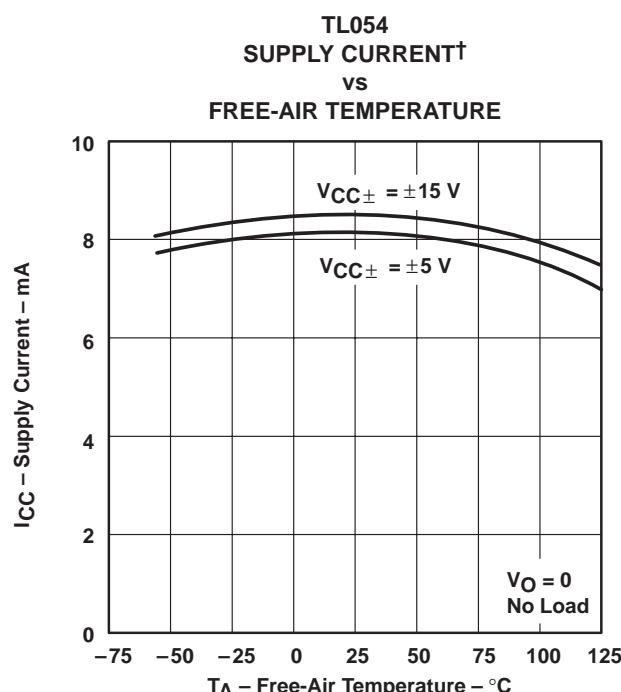


Figure 47

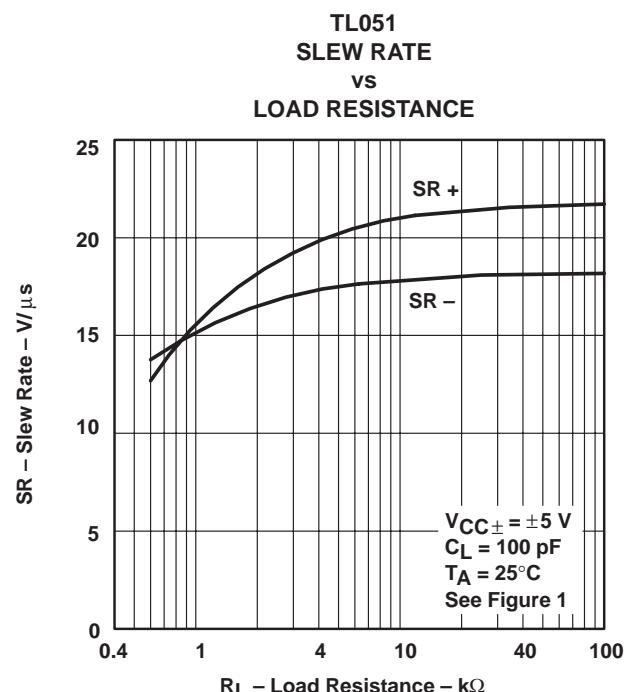


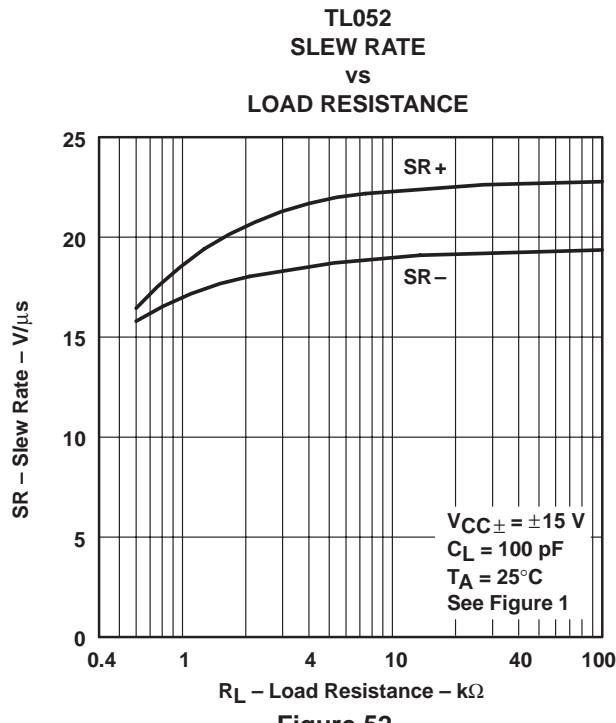
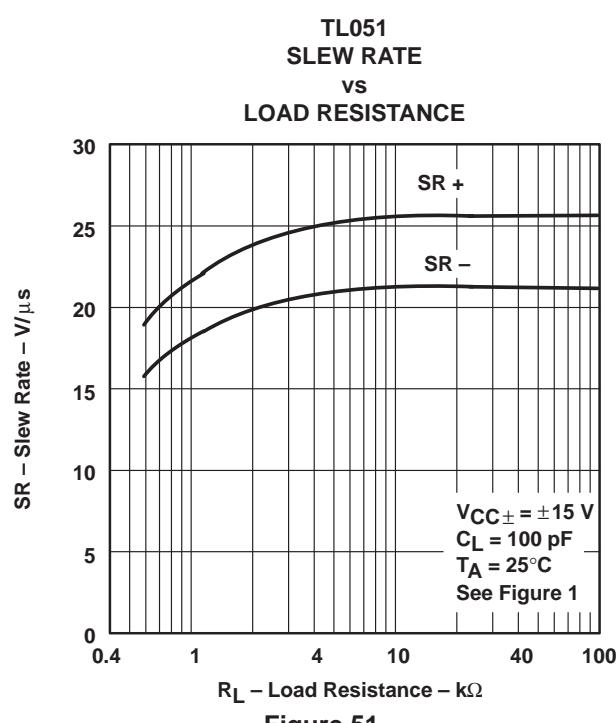
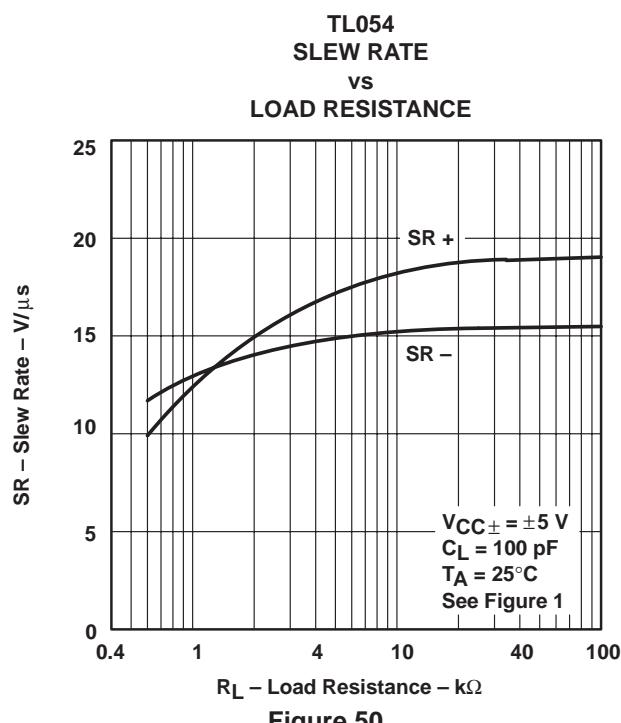
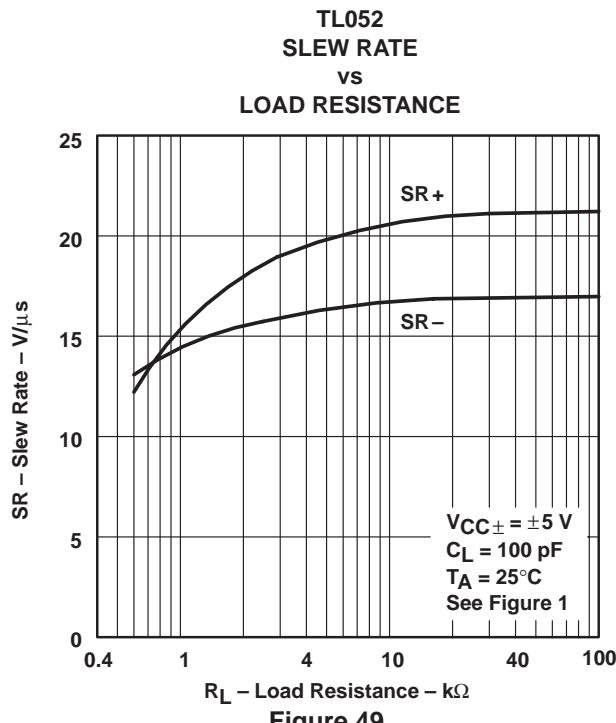
Figure 48

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

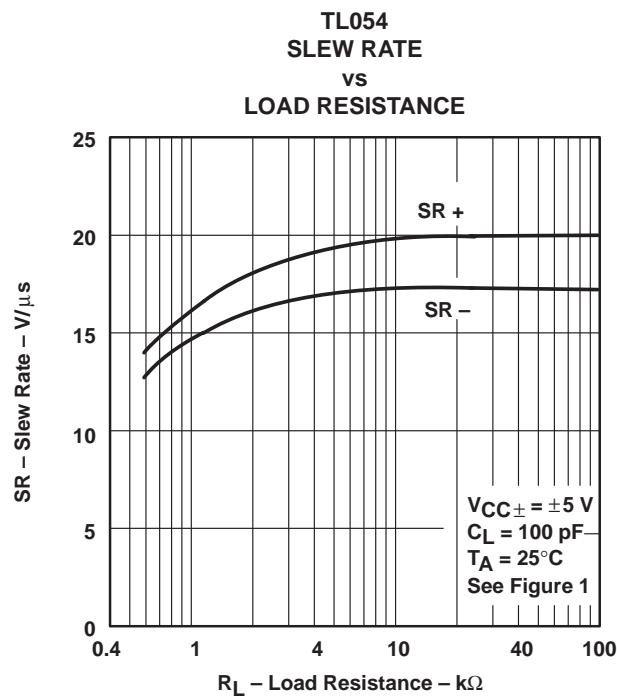


Figure 53

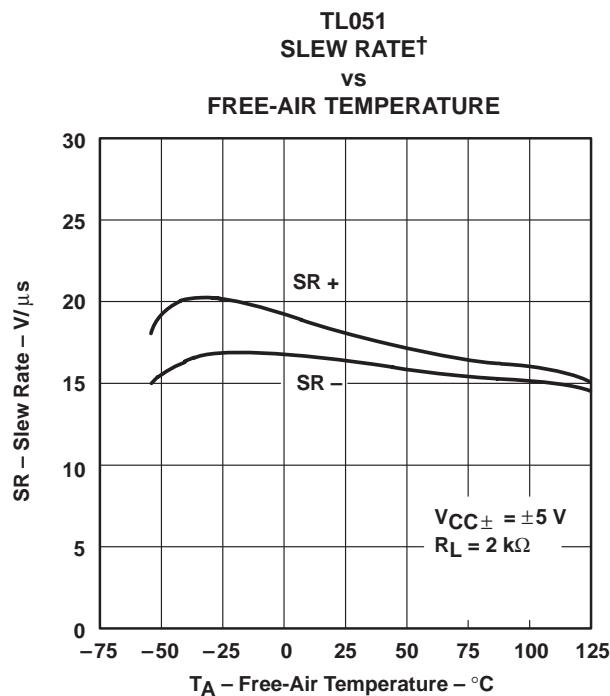


Figure 54

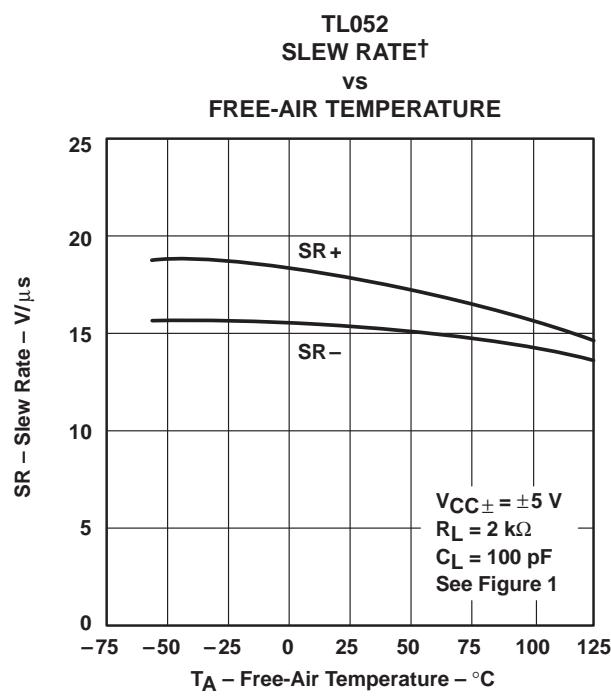


Figure 55

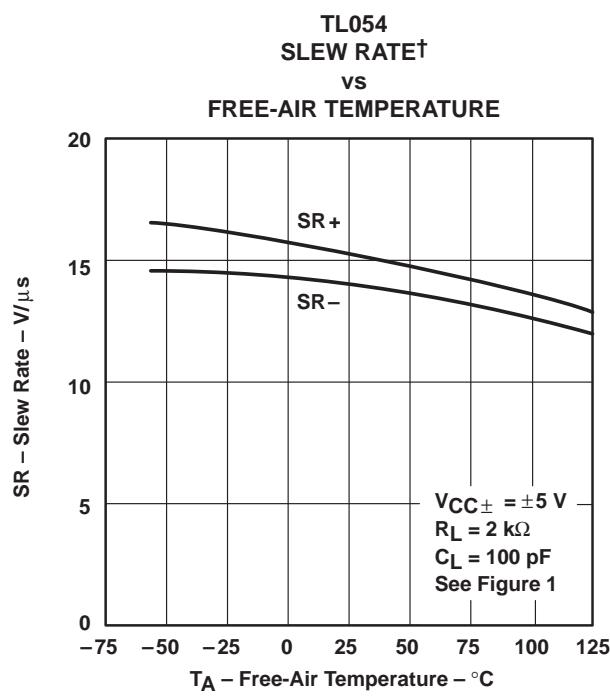


Figure 56

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

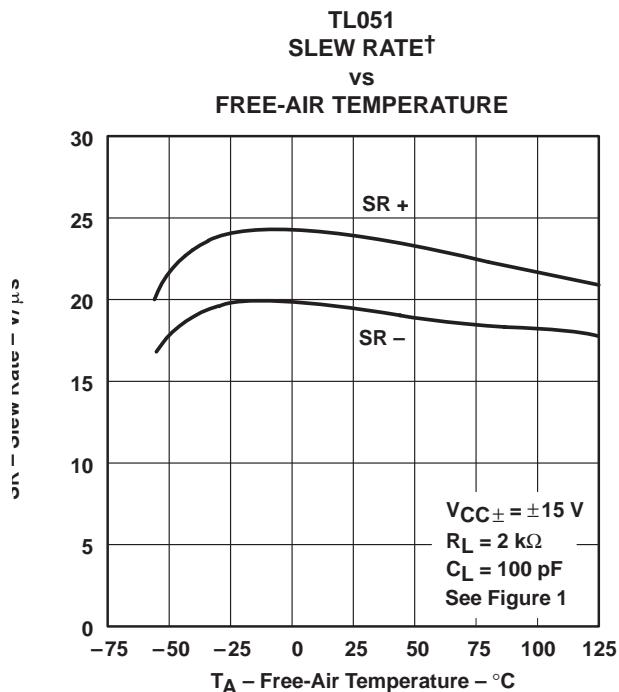


Figure 57

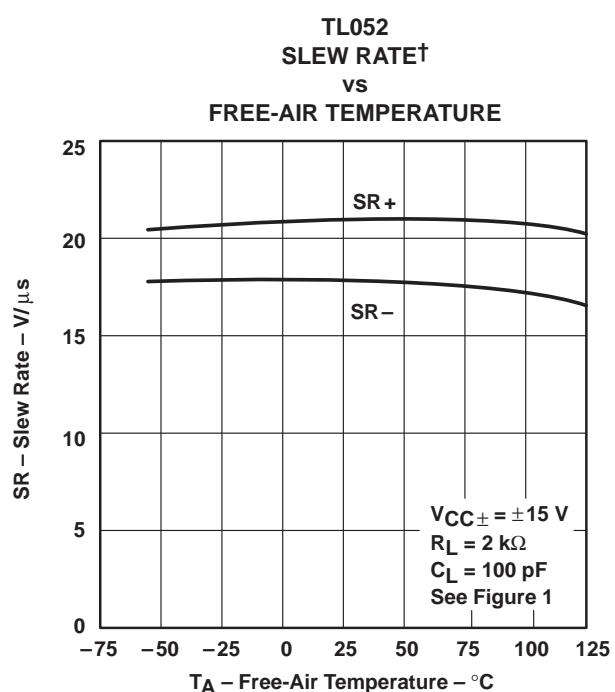


Figure 58

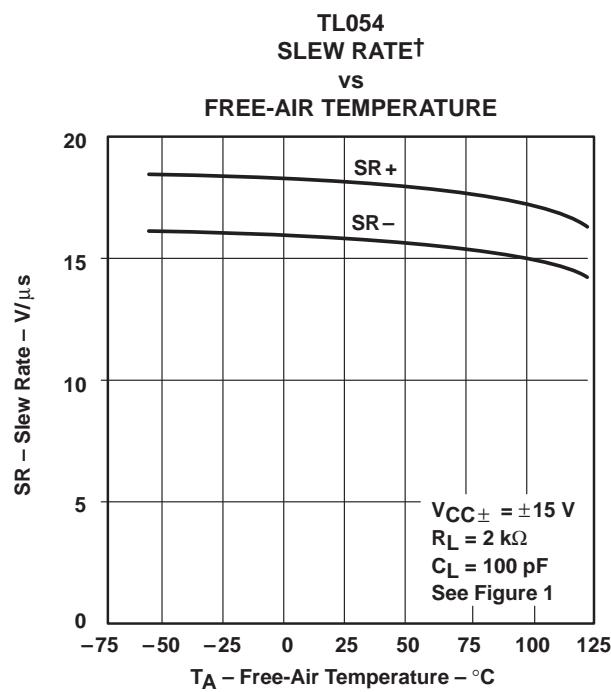


Figure 59

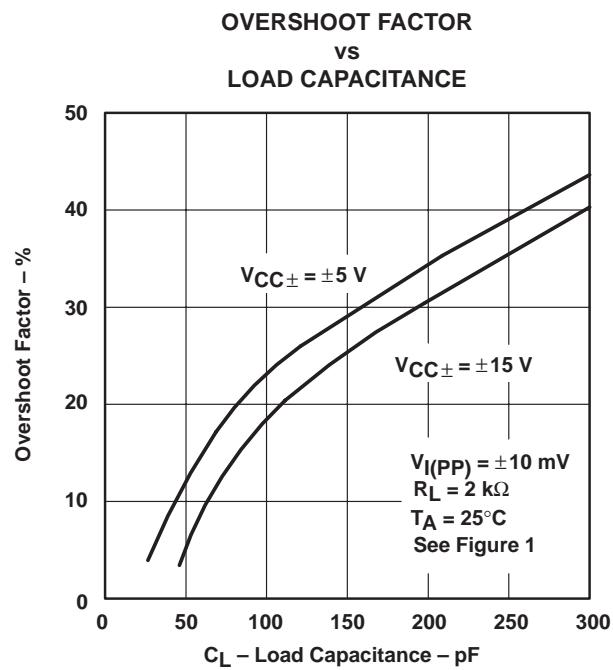


Figure 60

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL05x, TL05xA, TL05xY
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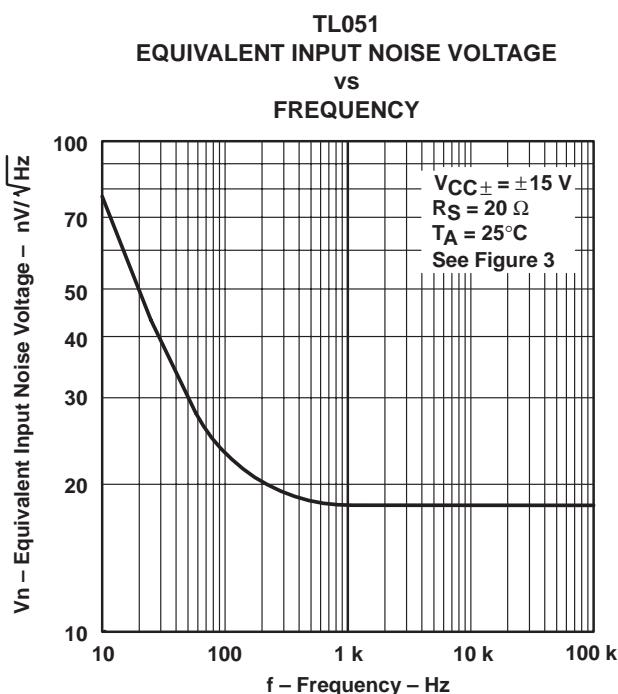


Figure 61

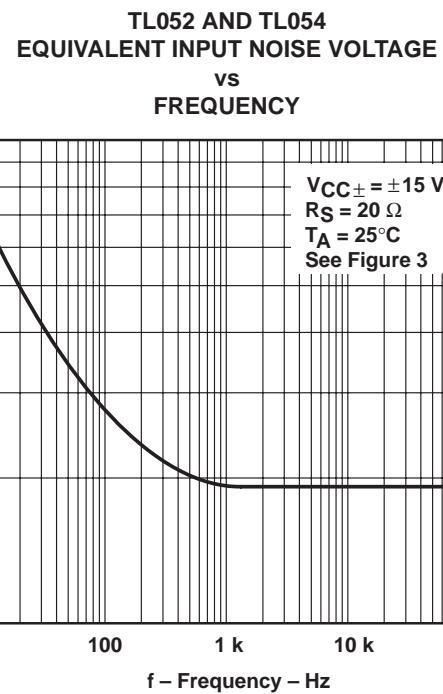


Figure 62

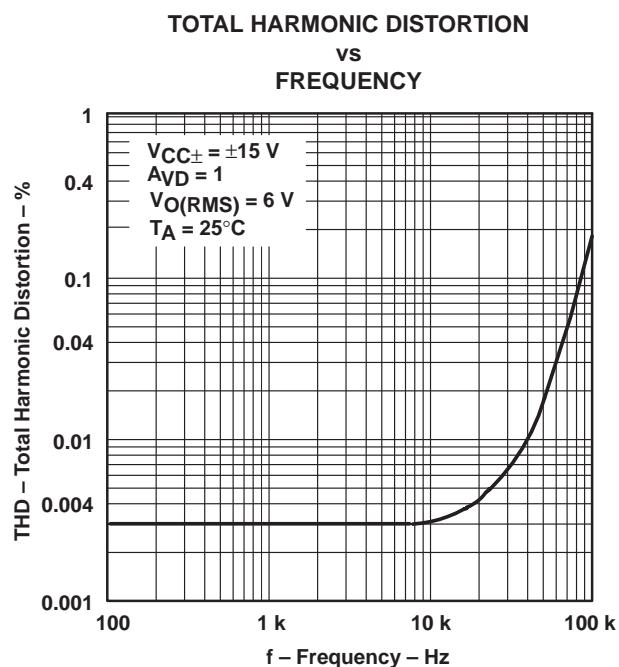


Figure 63

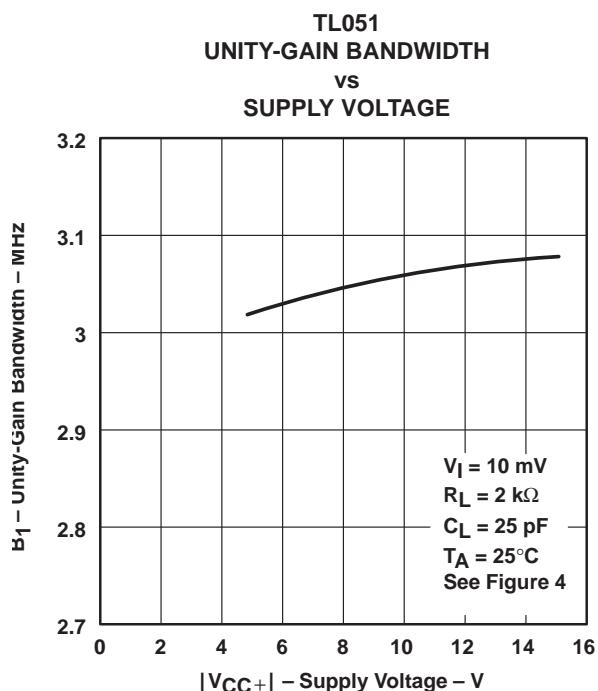


Figure 64



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TYPICAL CHARACTERISTICS

TL052
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

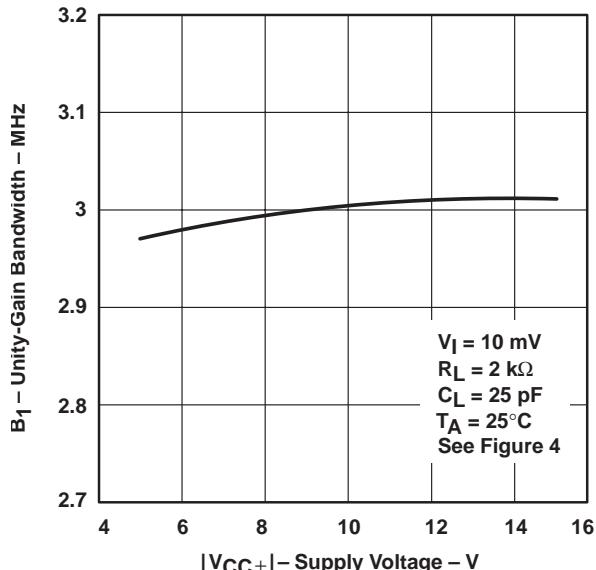


Figure 65

TL054
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

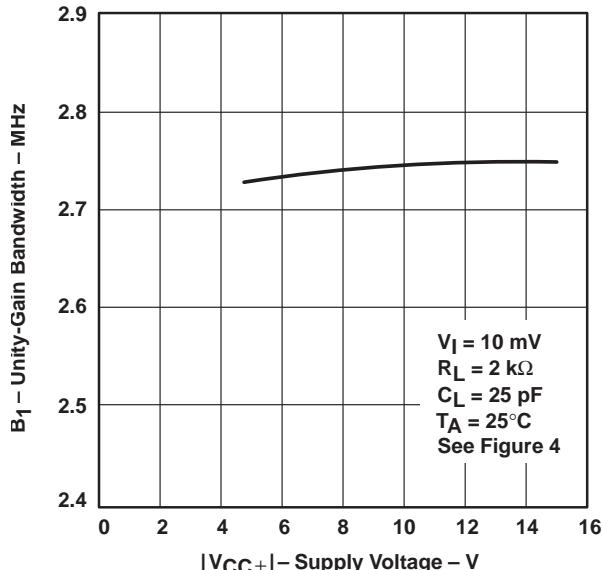


Figure 66

TL051
UNITY-GAIN BANDWIDTH†
vs
FREE-AIR TEMPERATURE

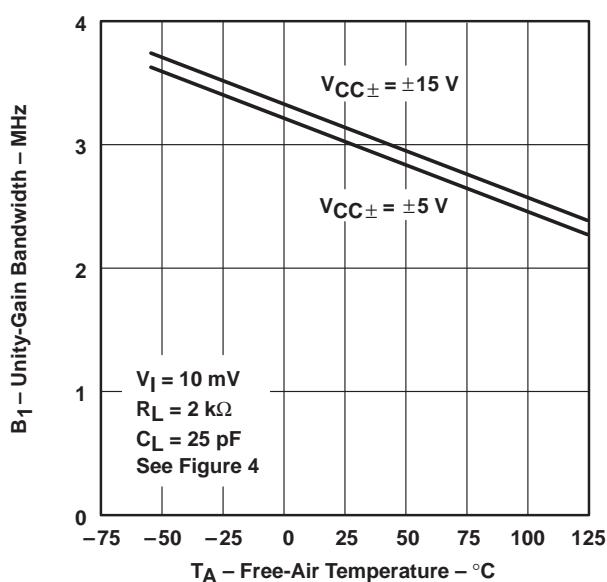


Figure 67

TL052
UNITY-GAIN BANDWIDTH†
vs
FREE-AIR TEMPERATURE

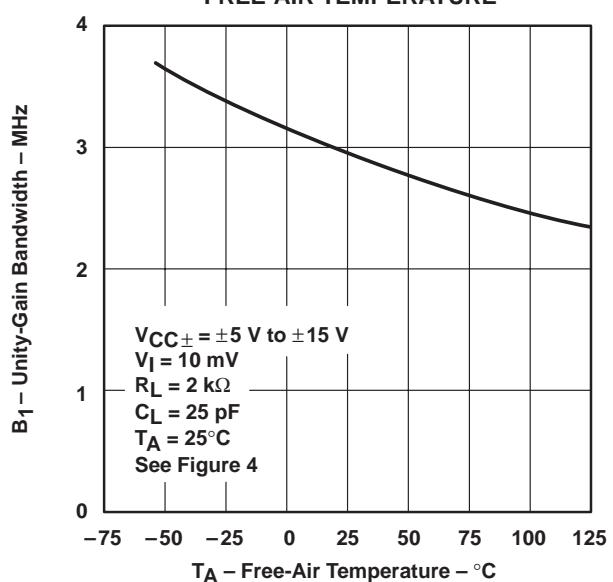


Figure 68

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL05x, TL05xA, TL05xY
ENHANCED-JFET LOW-OFFSET
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TYPICAL CHARACTERISTICS

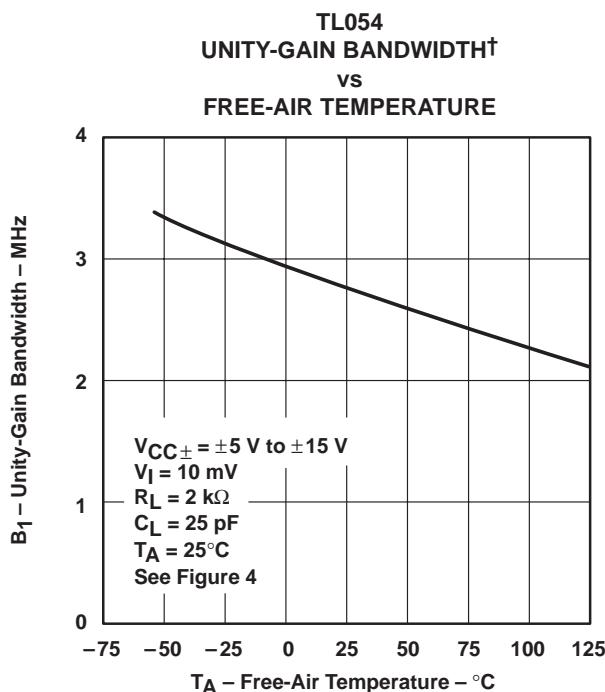


Figure 69

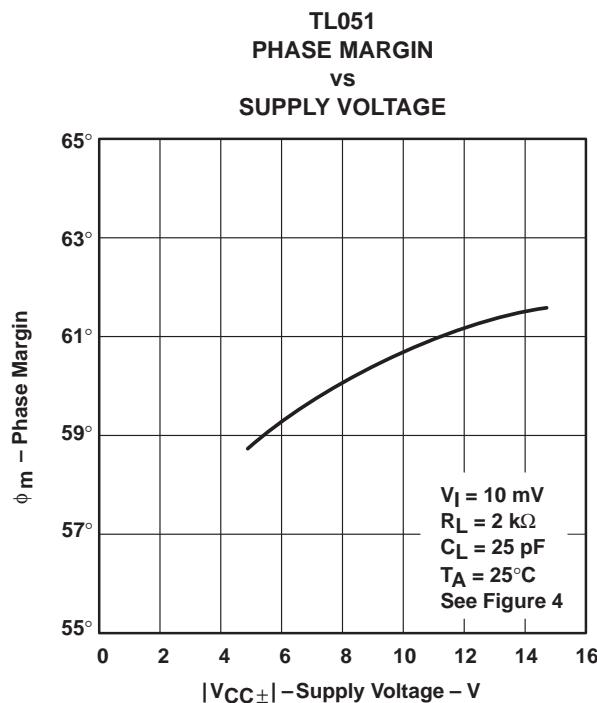


Figure 70

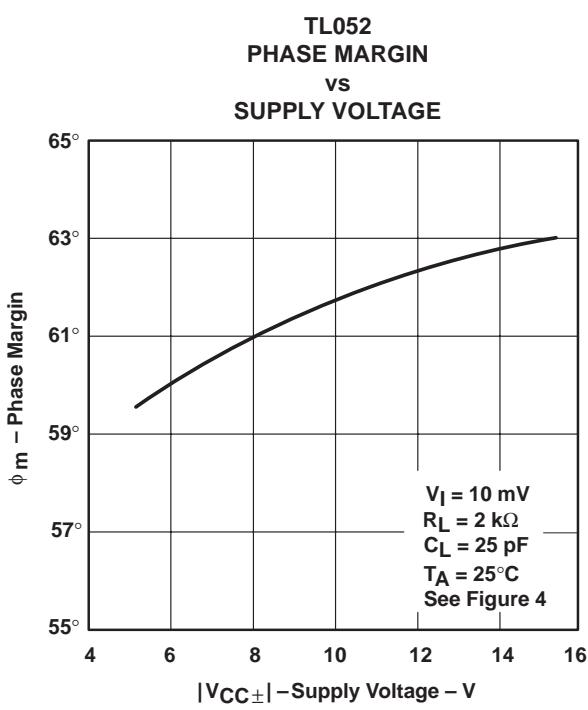


Figure 71

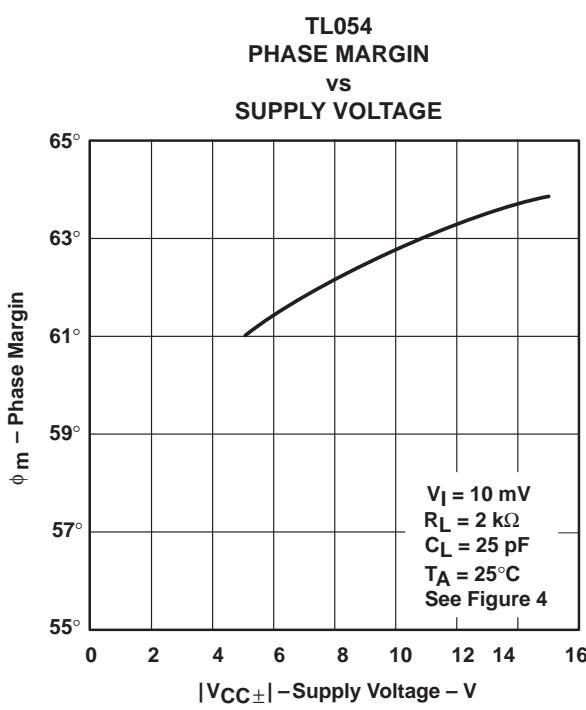


Figure 72

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

TL051
 PHASE MARGIN[†]
 VS
 LOAD CAPACITANCE

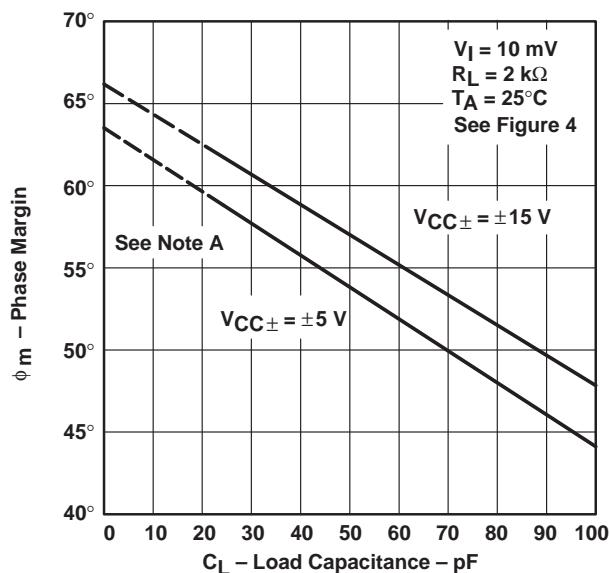


Figure 73

TL052
 PHASE MARGIN[†]
 VS
 LOAD CAPACITANCE

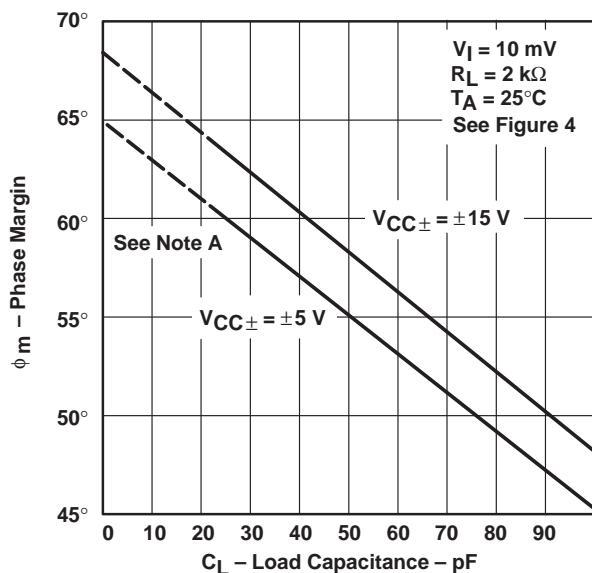


Figure 74

TL054
 PHASE MARGIN[†]
 VS
 LOAD CAPACITANCE

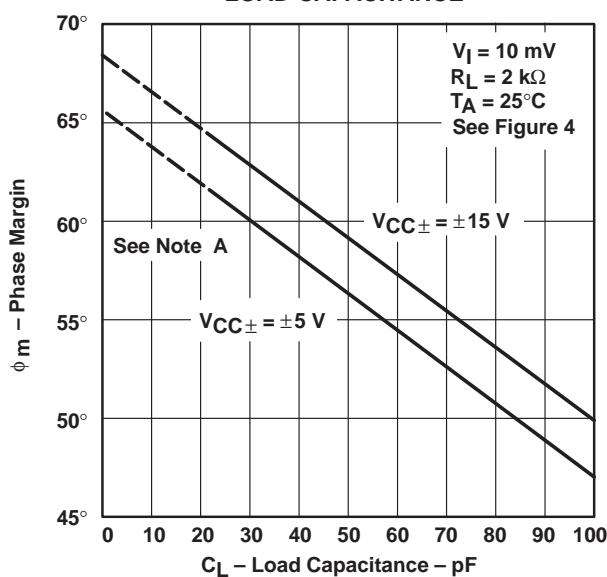


Figure 75

[†] Values of phase margin below a load capacitance of 25 pF were estimated.

**TL05x, TL05xA, TL05xY
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TYPICAL CHARACTERISTICS

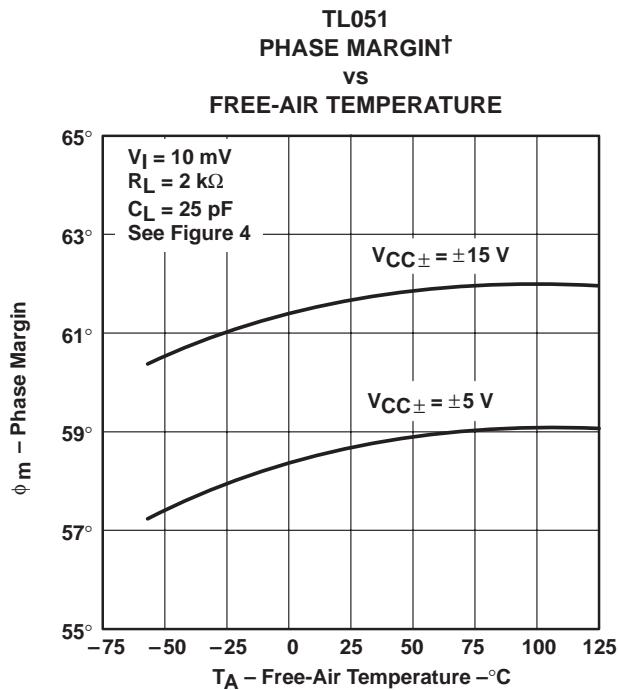


Figure 76

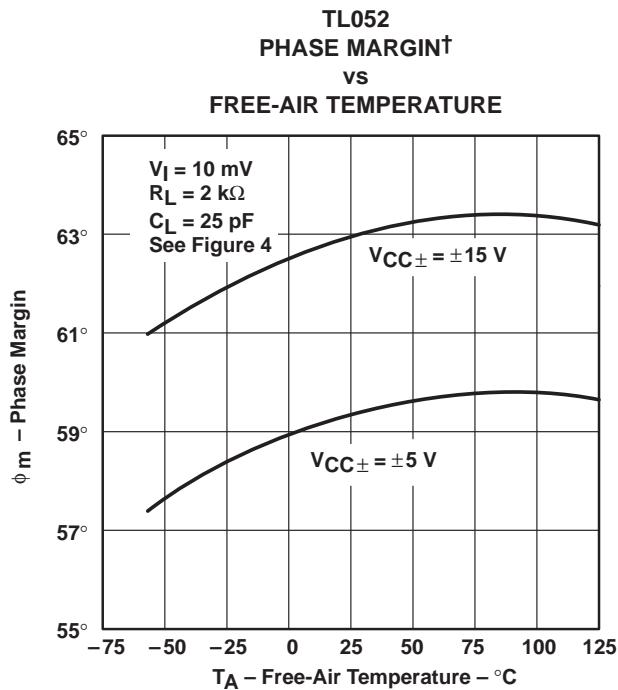


Figure 77

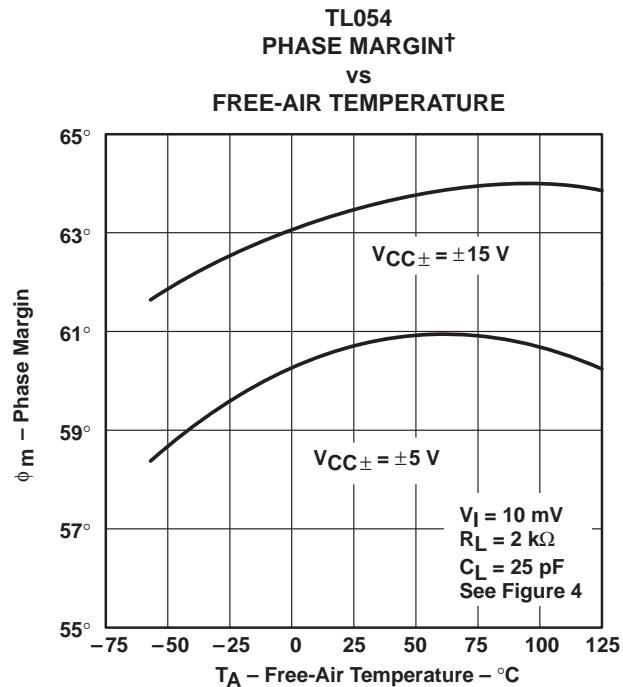


Figure 78

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
 SMALL-SIGNAL
 PULSE RESPONSE

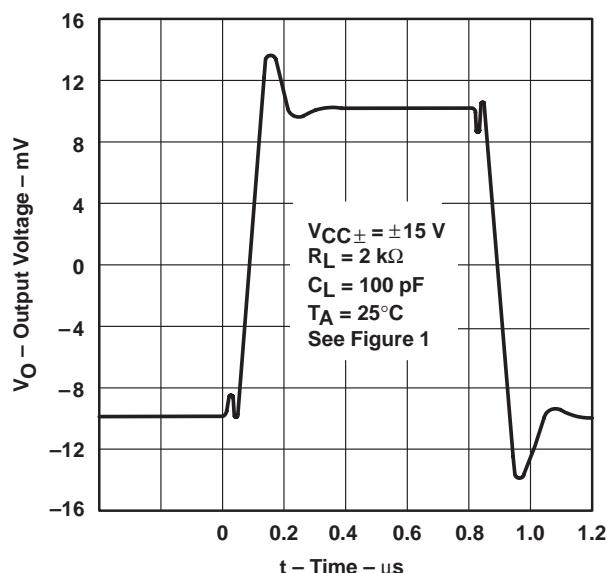


Figure 79

VOLTAGE-FOLLOWER
 LARGE-SIGNAL
 PULSE RESPONSE

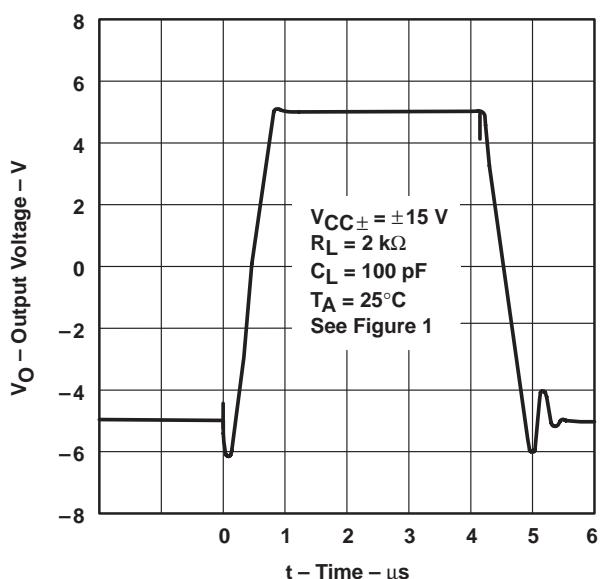


Figure 80

**TL05x, TL05xA, TL05xY
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APPLICATION INFORMATION

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL05x and TL05xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 81 and Figure 82).

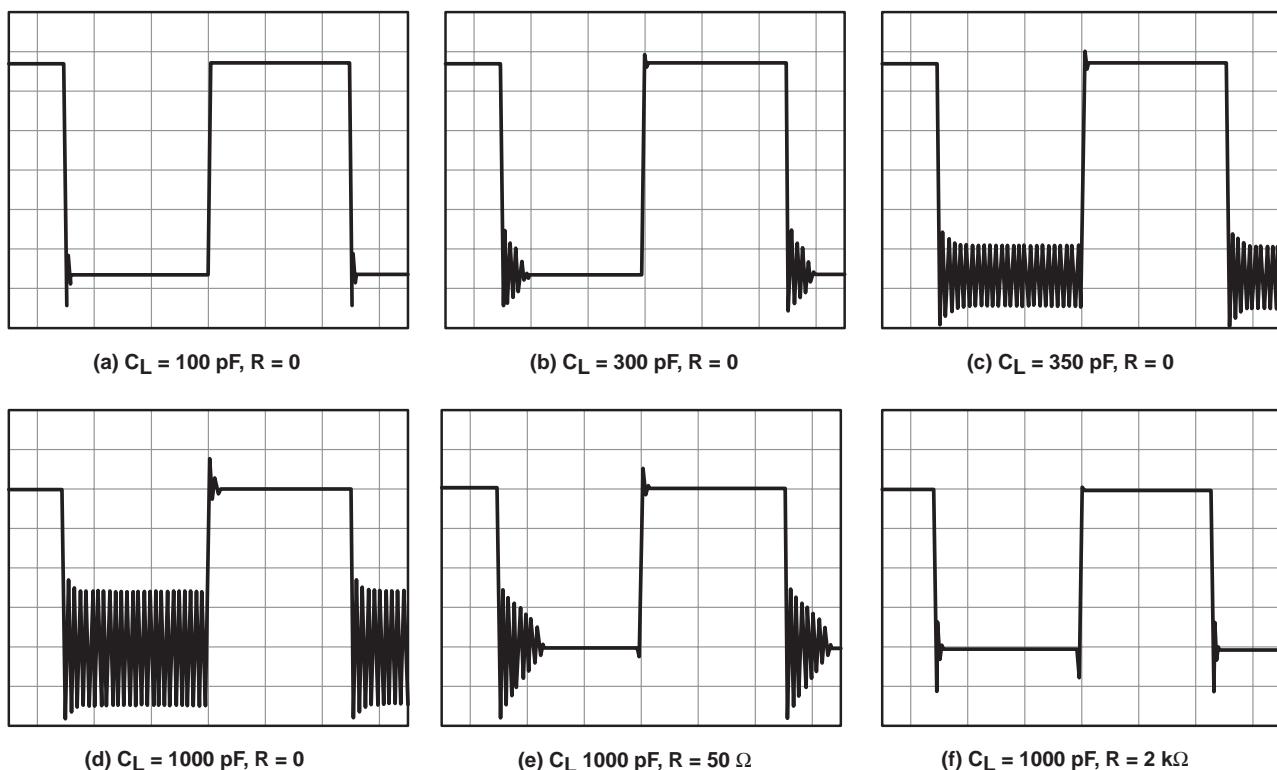


Figure 81. Effect of Capacitive Loads

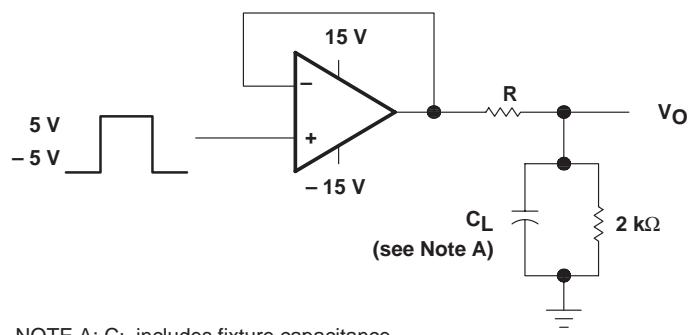


Figure 82. Test Circuit for Output Characteristics

APPLICATION INFORMATION

input characteristics

The TL05x and TL05xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL05x and TL05xA are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 83). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

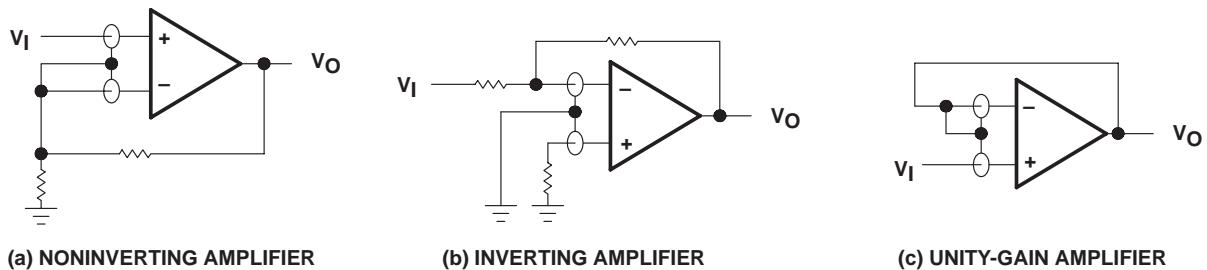


Figure 83. Use of Guard Rings

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL05x and TL05xA result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω .

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APPLICATION INFORMATION

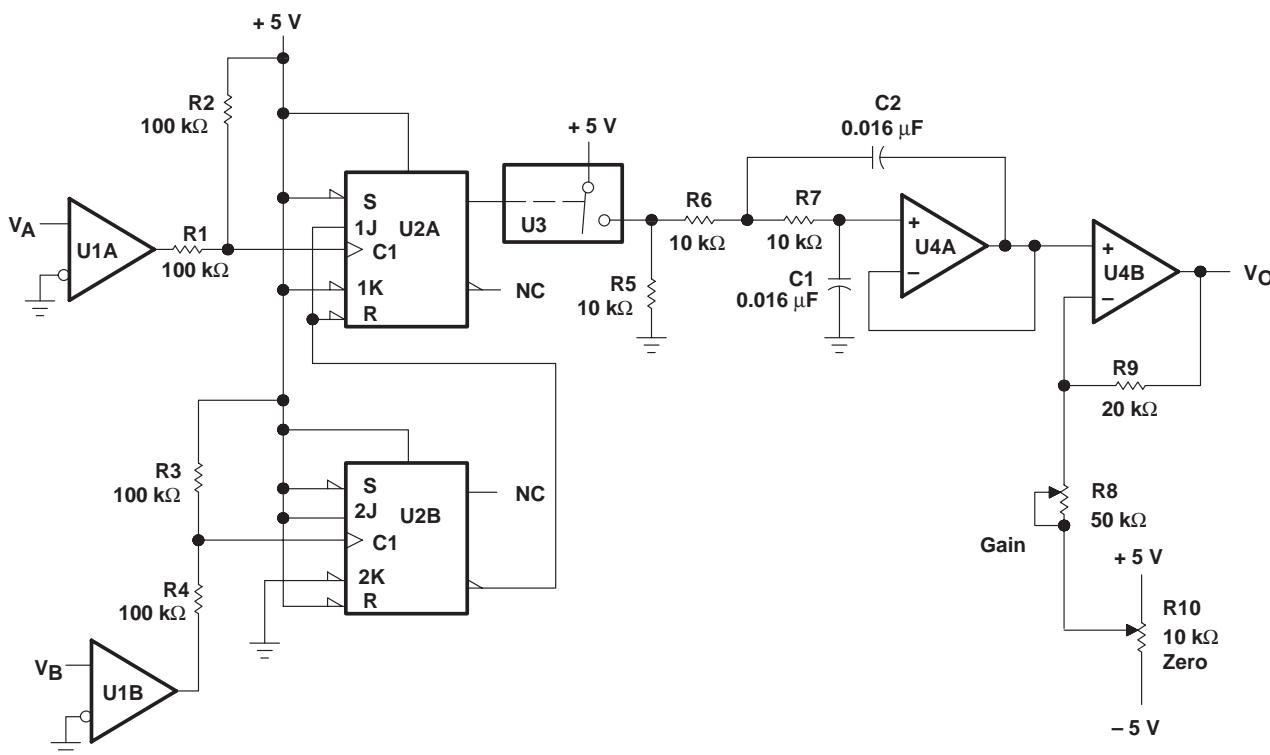
phase meter

The phase meter in Figure 84 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B . The reference signal V_A must be the same frequency as V_B . The TLC3702 comparators (U1) convert these two input sine waves into ± 5 -V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flops.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B . Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL05x (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U4A approximates a square wave and U2A has an output of almost 2.5 V. U4B acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0- to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTE A: U1 = TLC3702; $V_{CC\pm} = \pm 5$ V
U2 = SN74HC109
U3 = TLC4066
U4, U5 = TL05x; $V_{CC\pm} = \pm 5$ V

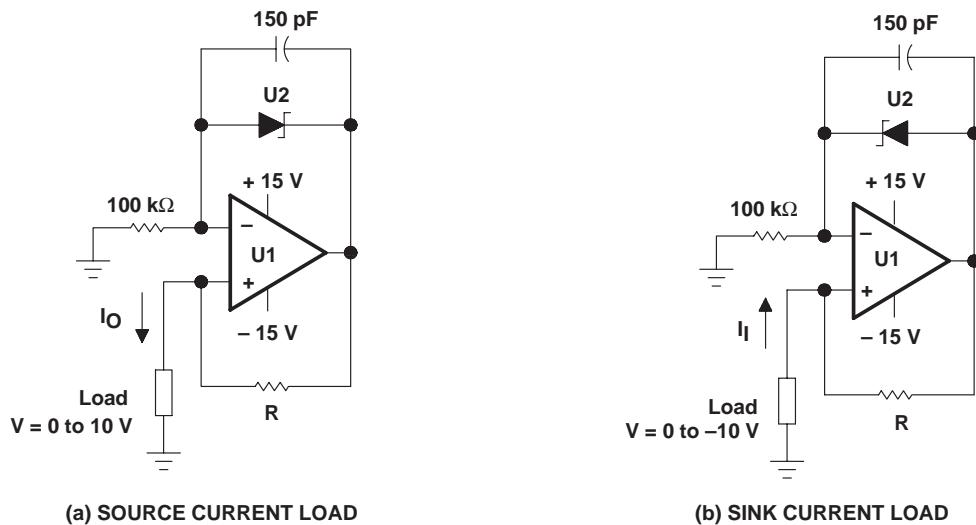
Figure 84. Phase Meter

APPLICATION INFORMATION

precision constant-current source over temperature

A precision current source (see Figure 85) benefits from the high input impedance and stability of Texas Instruments enhanced-JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL05x. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. If the regulator's cathode connects to the operational amplifier output, this circuit sources load current. Similarly, if the cathode connects to the inverting input, the circuit sinks current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split-voltage supplies.



NOTE B: U1 = 1/2 TL05x
 U2 = LM385, LT1004, or LT1009 voltage reference
 $I = \frac{2.5 V}{R}$, R = Low temperature coefficient metal film resistor

Figure 85. Precision Constant-Current Source

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APPLICATION INFORMATION

instrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 86 benefits greatly from the high input impedance and stable input offset voltage of the TL05xA. Amplifiers U1A, U1B, and U2A form the actual instrumentation amplifier, while U2B provides offset null. Potentiometer R1 provides gain adjust. With $R1 = 2\text{ k}\Omega$, the circuit gain equals 100, while with $R1 = 200\text{ k}\Omega$, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

$$A_v = 1 + \left(\frac{R_2 + R_3}{R_1} \right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. If U2B is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL05xA minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_I equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2} \left[\left(1 + \frac{R3}{R1} \right) \left(\frac{R7}{R5 + R7} \right) \left(1 + \frac{R6}{R4} \right) + \frac{R2}{R1} \left(\frac{R6}{R4} \right) \right] - V_{IO1} \left[\frac{R3}{R1} \left(\frac{R7}{R5 + R7} \right) \left(1 + \frac{R6}{R4} \right) + \frac{R6}{R4} \left(1 + \frac{R2}{R1} \right) \right] + V_{IO3} \left(1 + \frac{R6}{R4} \right)$$

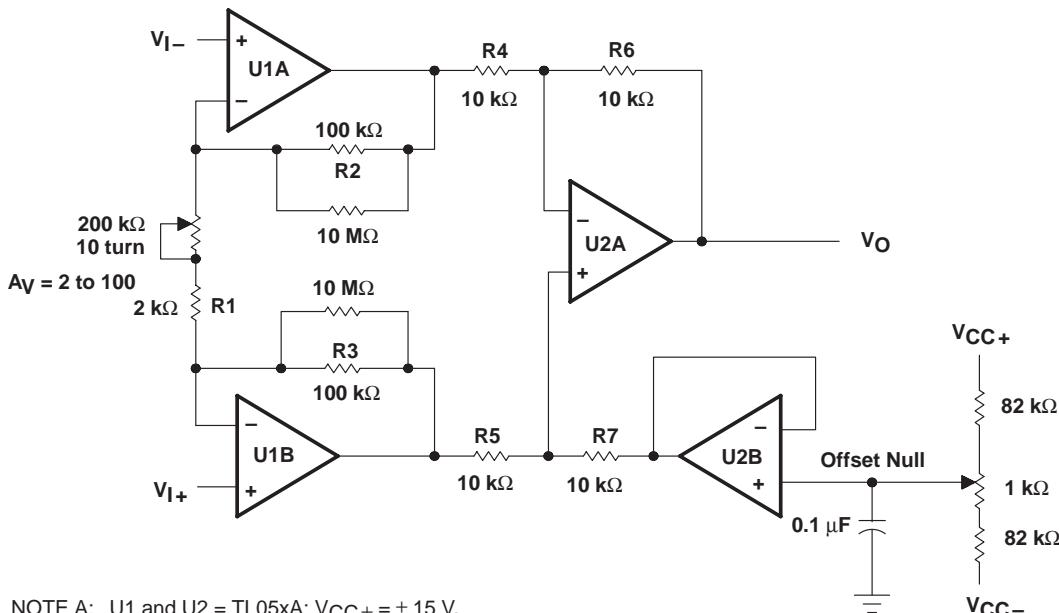


Figure 86. Instrumentation Amplifier



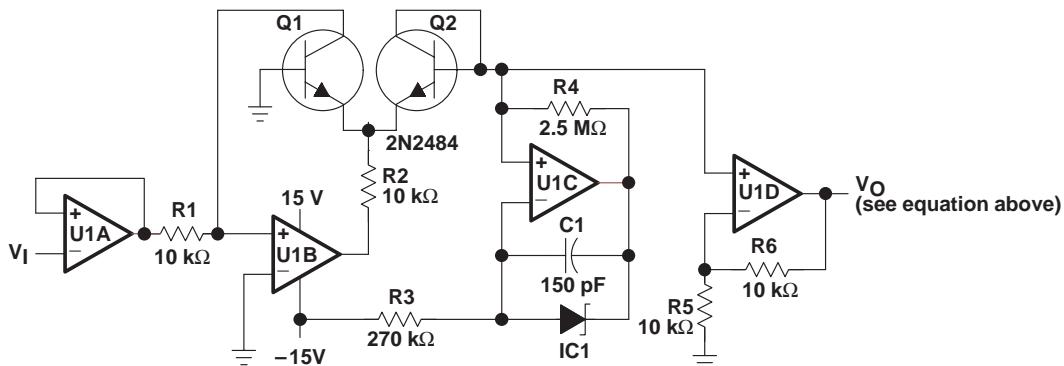
APPLICATION INFORMATION

high input impedance log amplifier

The low input offset voltage and high input impedance of the TL05xA creates a precision log amplifier (see Figure 87). IC1 is a 2.5-V, low-current precision, shunt regulator. Transistors Q1 and Q2 must be a closely matched NPN pair. For best performance over temperature, R4 should be a metal film resistor with a low temperature coefficient.

In this circuit, U1A serves as a high-impedance unity-gain buffer. Amplifier U1B converts the input voltage to a current through R1 and Q1. Amplifier U1C, IC1, and R4 form a 1- μ A temperature-stable current source that sets the base-emitter voltage of Q2. U1D amplifies the difference between the base-emitter voltage of Q1 and Q2 (see Figure 88). The output voltage is given by the following equation:

$$V_O = -\left[1 + \frac{R_6}{R_5}\right] \frac{kT}{q} \left[\ln \frac{V_I}{(R_1 \times 1 \times 10^{-6})} \right] \text{ where } k = 1.38 \times 10^{-23}, q = 1.602 \times 10^{-19}, \text{ and } T \text{ is in degrees kelvin.}$$



NOTE A: U1A through U1D = TL05xA. IC1 = LM385, LT1004, or LT1009 voltage reference.

Figure 87. Log Amplifier

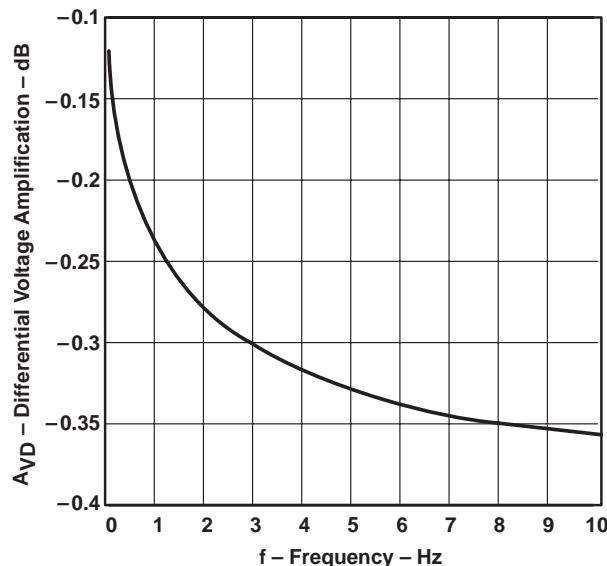


Figure 88. Output Voltage vs Input Voltage for Log Amplifier

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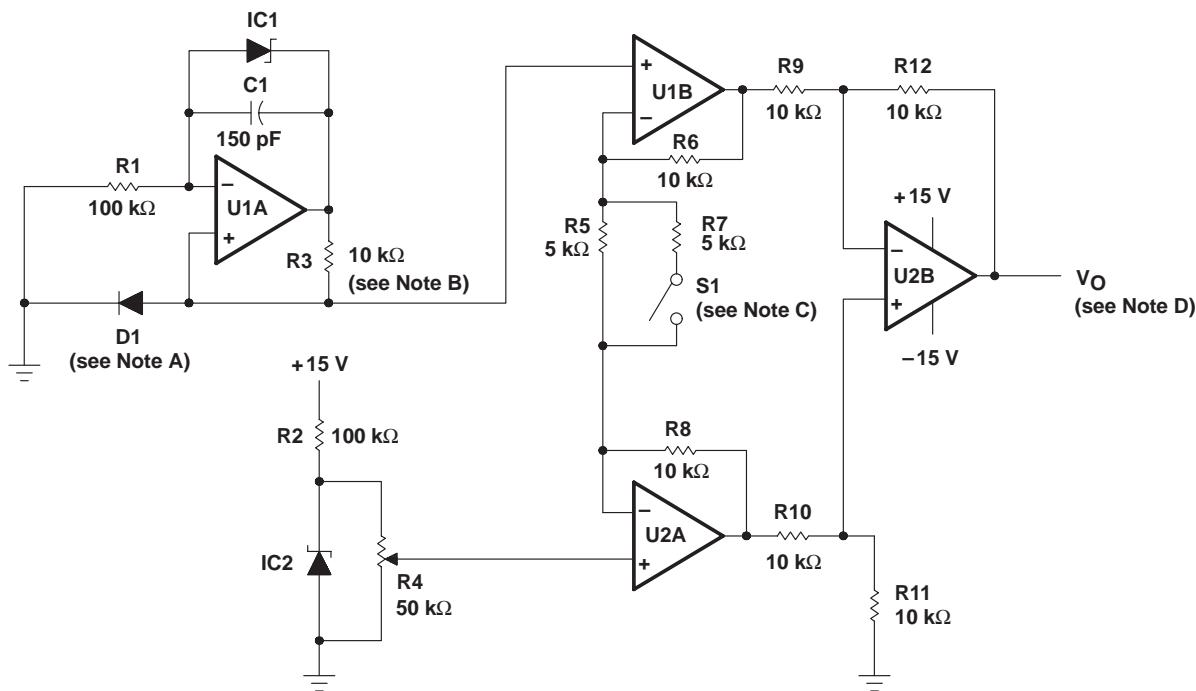
APPLICATION INFORMATION

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 89). Amplifier U1A and IC1 establish a constant current through the temperature-sensing diode D1. For this section of the circuit to operate correctly, the TL05x must use split supplies and R3 must be a metal-film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U2A, and U2B form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5 and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9 and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



- NOTES:
- A. Temperature-sensing diode $\approx -2 \text{ mV}/^\circ\text{C}$
 - B. Metal-film resistor (low temperature coefficient)
 - C. Switch open for ${}^\circ\text{F}$ and closed for ${}^\circ\text{C}$
 - D. $V_O \propto$ temperature; $10 \text{ mV}/^\circ\text{C}$ or $10 \text{ mV}/^\circ\text{F}$
 - E. U1, U2 = TL05x. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference

Figure 89. Analog Thermometer

APPLICATION INFORMATION

voltage-ratio-to-dB converter

The application in Figure 90 measures the amplitude ratio of two signals and then converts the ratio to decibels (see Figure 91). The output voltage provides a resolution of 100 mV/dB. The two inputs can be either dc or sinusoidal ac signals. When using ac signals, both signals should be the same frequency or output glitches will occur. For measuring two input signals of different frequencies, extra filtering should be added after the rectifiers.

The circuit contains three low-offset TL05xA devices. Two of these devices provide the rectification and logarithmic conversion of the inputs. The third TL05xA forms an instrumentation amplifier. The stage performing the logarithmic conversion also requires two well-matched npn transistors.

The input signal first passes through a high impedance unity-gain buffer U1A (U2A). Then U1B (U2B) rectifies the input signal at a gain of 0.5, and U1C (U2C) provides a noninverting gain of 2 so that the system gain is still one. U1D (U2D), R6 (R13), and Q1 (Q2) perform the logarithmic conversion of the rectified input signal. The instrumentation amplifier formed by U3A, U3B, U3D scales the difference of the two logarithmic voltages by a gain of 33.6. As a result, the output voltage equals 100 mV/dB. The 1-k Ω potentiometer on the input of U3C calibrates the zero dB reference level. The following equations are used to derive the relationship between the input voltage ratio expressed in decibels and the output voltage.

$$X \text{ dB} = 20 \log \left[\frac{V_A}{V_B} \right] = 20 \left[\frac{\ln(V_A) - \ln(V_B)}{\ln(10)} \right]$$

$$X \text{ dB} = 8.686 \left[\ln(V_A) - \ln(V_B) \right]$$

$$V_{BE(Q1)} = \frac{kT}{q} \ln \left[\frac{V_A}{R \times I_S} \right] \quad V_{BE(Q2)} = \frac{kT}{q} \ln \left[\frac{V_B}{R \times I_S} \right]$$

$$\Delta V_{BE} = V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q} \left[\ln(V_A) - \ln(V_B) \right]$$

$$X \text{ dB} = \frac{8.686}{kT/q} \left[V_{BE(Q1)} - V_{BE(Q2)} \right] = 336 \left[V_{BE(Q1)} - V_{BE(Q2)} \right] \text{ at } 25^\circ\text{C}$$

where

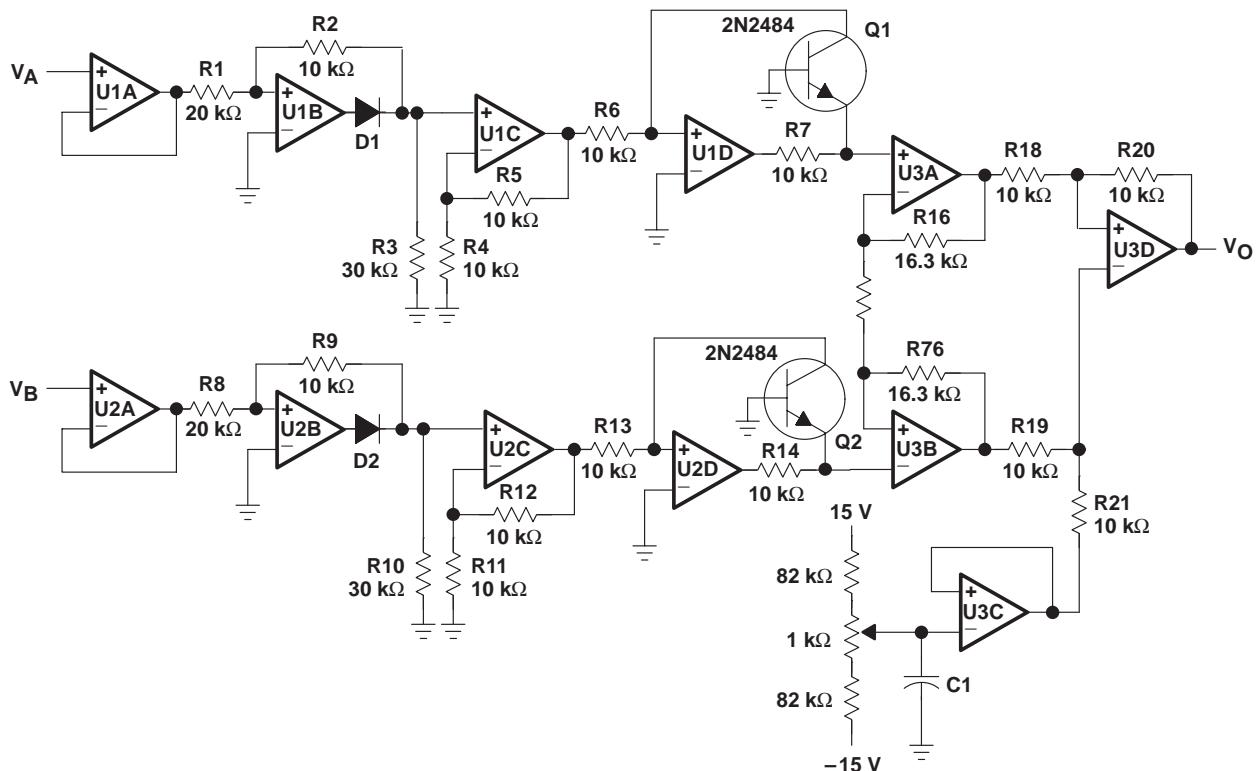
$$k = 1.38 \times 10^{-23}, \quad q = 1.602 \times 10^{-19}, \quad \text{and T is in kelvins.}$$

This would give a resolution of 1 V/dB. Therefore, the gain of the instrumentation amplifier is set at 33.6 to obtain 100 mV/dB.

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APPLICATION INFORMATION



NOTE A: U1A through U3D = TL05xA, $V_{CC\pm} = \pm 15$ V. D1 and D2 = 1N914.

Figure 90. Voltage-Ratio-to-dB Converter

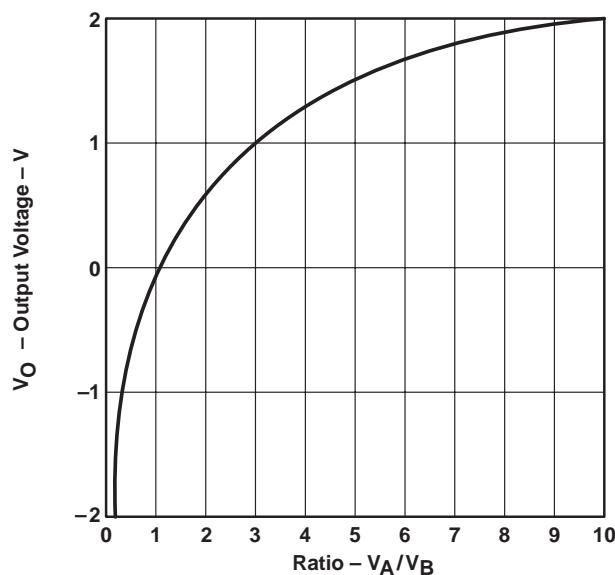


Figure 91. Output Voltage vs the Ratio of the Input Voltages for Voltage-to-dB Converter

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*TM, the model generation software used with Microsim *PSpice*TM. The Boyle macromodel (see Note 5) and subcircuit Figure 92 are generated using the TL05x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

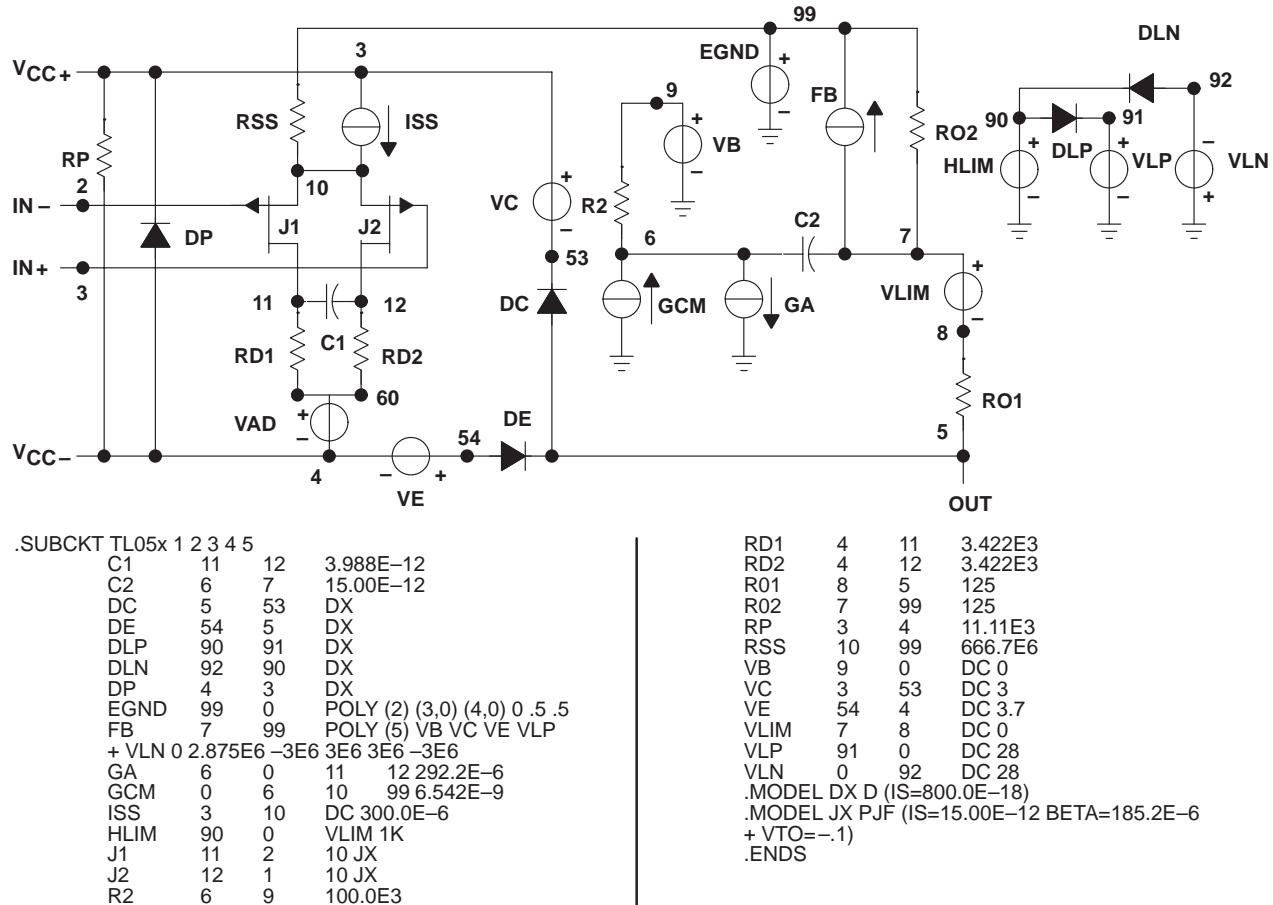


Figure 92. Boyle Macromodel and Subcircuit

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