- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  $T_A = -40°C$ to $85°C$ . . . 2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail and up to $V_{DD} -1$ V at $T_A = 25°C$**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

TLV2322
D OR P PACKAGE
(TOP VIEW)

1OUT	1	8	V_{DD}
1IN−	2	7	2OUT
1IN+	3	6	2IN−
V_{DD}−/GND	4	5	2IN+

TLV2322
PW PACKAGE
(TOP VIEW)

1OUT	1	8	V_{DD+}
1IN−	2	7	2OUT
1IN+	3	6	2IN−
V_{DD}−/GND	4	5	2IN+

TLV2324
D OR N PACKAGE
(TOP VIEW)

1OUT	1	14	4OUT
1IN −	2	13	4IN −
1IN +	3	12	4IN +
V_{DD+}	4	11	V_{DD} −/GND
2IN +	5	10	3IN +
2IN −	6	9	3IN −
2OUT	7	8	3OUT

TLV2324
PW PACKAGE
(TOP VIEW)

1OUT	1	14	4OUT
1IN −			4IN −
1IN +			4IN +
V_{DD+}			V_{DD} −/GND
2IN +			3IN +
2IN −			3IN −
2OUT	7	8	3OUT

description

The TLV232x operational amplifiers are in a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low-power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier specified at only 27 µA over its full temperature range of −40°C to 85°C.
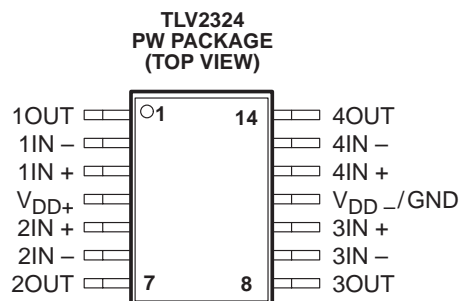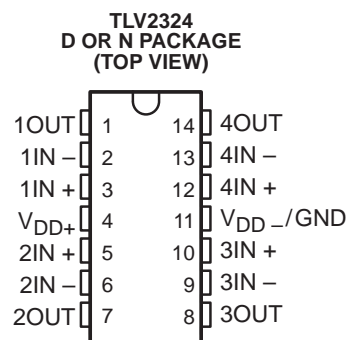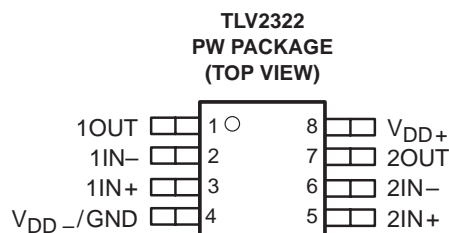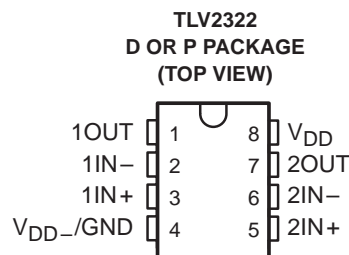
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM§ (Y)
		SMALL OUTLINE† (D)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP‡ (PW)	
−40°C to 85°C	9 mV	TLV2322ID	—	TLV2322IP	TLV2322IPWLE	TLV2322Y
	10 mV	TLV2324ID	TLV2324IN	—	TLV2324IPWLE	TLV2324Y

† The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2322IDR).
‡ The PW package is only available left-end taped and reeled (e.g., TLV2322IPWLE).
§ Chip forms are tested at 25°C only.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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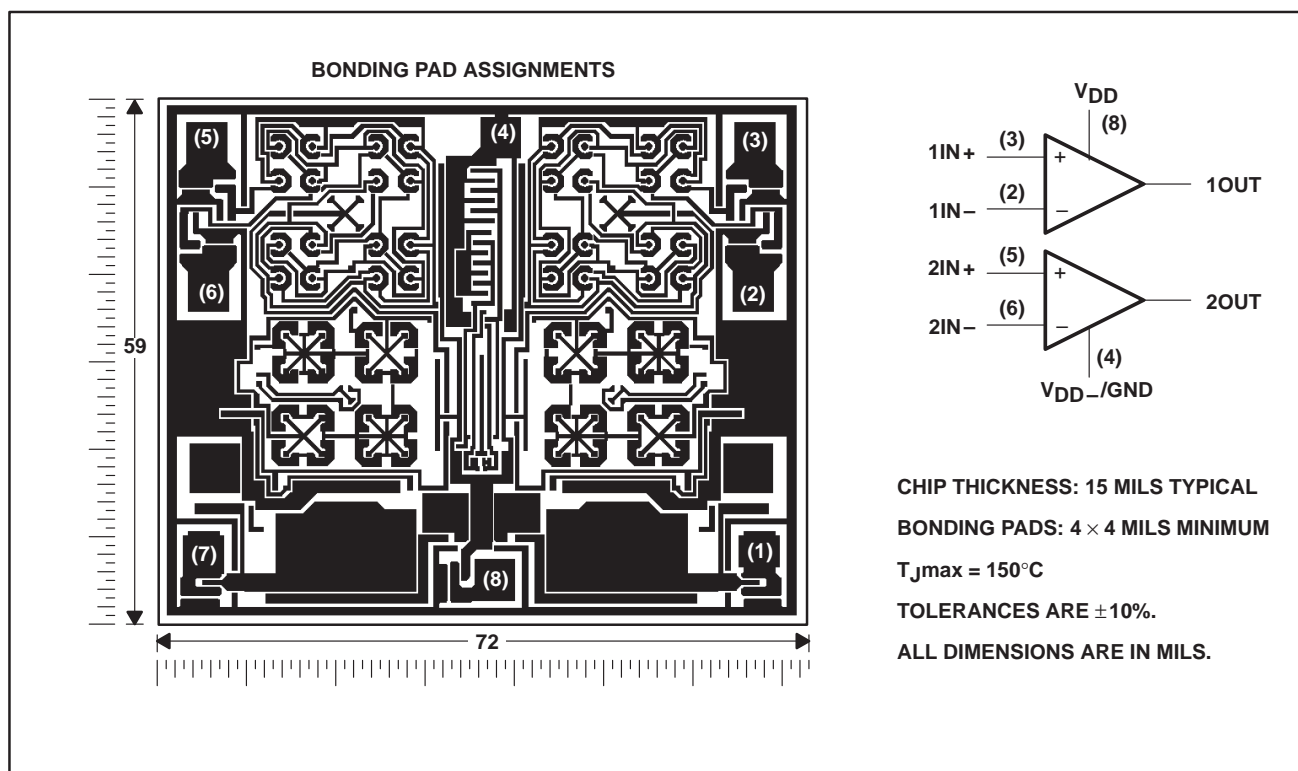
description (continued)

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

To facilitate the design of small portable equipment, the TLV232x is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV232x incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD can result in the degradation of the device parametric performance.

TLV2322Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2322I. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_Jmax = 150°C$

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

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TLV2324Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2324. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.
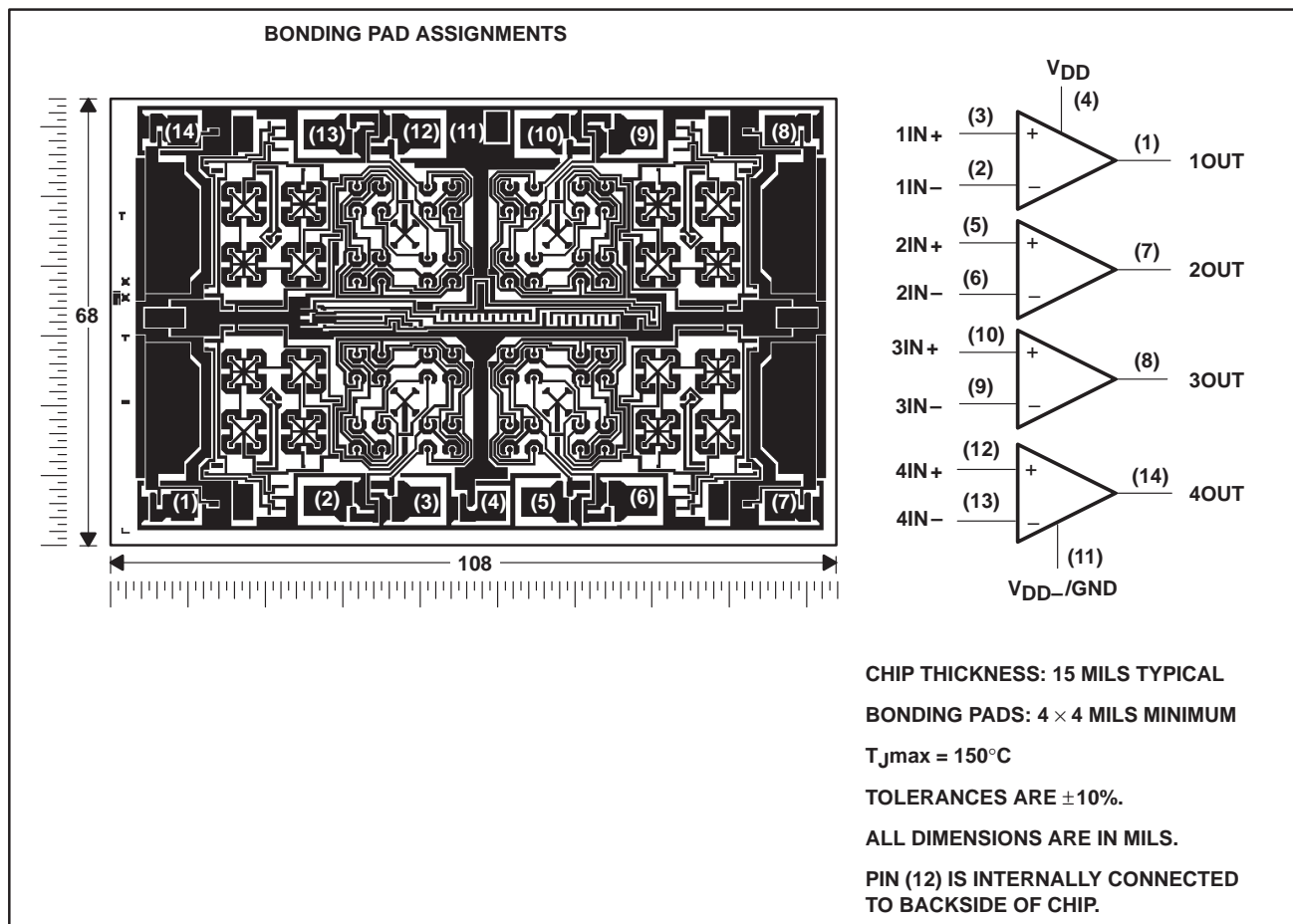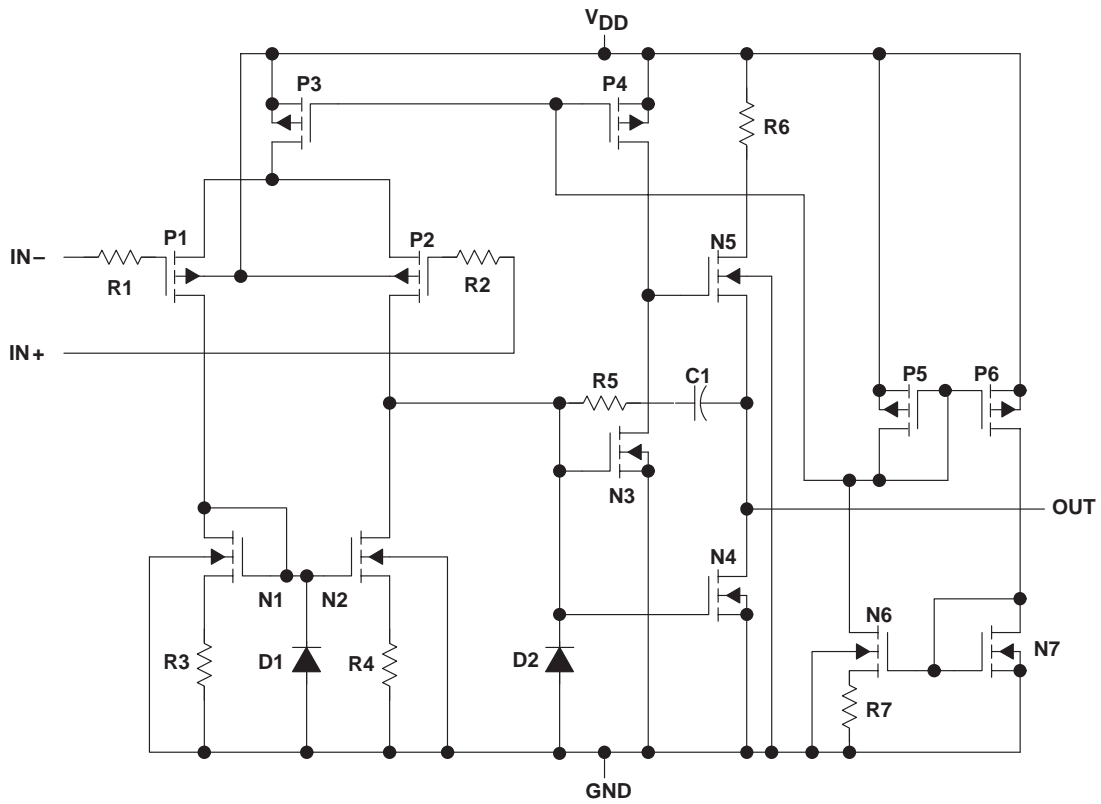
BONDING PAD ASSIGNMENTS

V_{DD} (4)

1IN+ (3) +
1IN− (2) −
(1) 1OUT

2IN+ (5) +
2IN− (6) −
(7) 2OUT

3IN+ (10) +
3IN− (9) −
(8) 3OUT

4IN+ (12) +
4IN− (13) −
(14) 4OUT

(11)
V_{DD-}/GND

CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (12) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)

ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLV2342	TLV2344
Transistors	54	108
Resistors	14	28
Diodes	4	8
Capacitors	2	4

† Includes both amplifiers and all ESD, bias, and trim circuitry.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	$V_{DD}\pm$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O	±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D–8	725 mW	5.8 mW/°C	377 mW
D–14	950 mW	7.6 mW/°C	494 mW
N	1575 mW	12.6 mW/°C	819 mW
P	1000 mW	8.0 mW/°C	520 mW
PW–8	525 mW	4.2 mW/°C	273 mW
PW–14	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

TLV2322 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2322						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = − 100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		12	34		20	34	μA
			Full range			54			54	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
        5. This range also applies to each input individually.
        6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5

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TLV2322 operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 35	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/µs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/$\sqrt{Hz}$
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f= B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

TLV2322 operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 35	$V_{I(PP)}$ = 1 V	25°C		0.03		V/µs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/$\sqrt{Hz}$
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

TLV2324I electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2324I V$_{DD}$ = 3 V MIN	TYP	MAX	TLV2324I V$_{DD}$ = 5 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ,	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V$_{ICR}$min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k$_{SVR}$	Supply-voltage rejection ratio (ΔV$_{DD}$/ΔV$_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		24	68		39	68	µA
			Full range			108			108	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

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TLV2324I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 35	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/µs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f = B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

TLV2324I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 35	$V_{I(PP)}$ = 1 V	25°C		0.03		V/µs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

![Texas Instruments logo]

TLV2322Y electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		V_{DD} = 3 V			V_{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 1$ V, $R_S = 50$ Ω,	$V_{IC} = 1$ V, $R_L = 1$ MΩ		1.1			1.1		mV
I_{IO}	Input offset current (see Note 4)	$V_O = 1$ V,	$V_{IC} = 1$ V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	$V_O = 1$ V,	$V_{IC} = 1$ V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)				−0.3 to 2.3			−0.3 to 4.2		V
V_{OH}	High-level output voltage	$V_{IC} = 1$ V, $I_{OH} = -1$ mA	$V_{ID} = -100$ mV,		1.9			3.8		V
V_{OL}	Low-level output voltage	$V_{IC} = 1$ V, $I_{OL} = 1$ mA	$V_{ID} = 100$ mV,		115			95		mV
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 1$ V, See Note 6	$R_L = 1$ MΩ,		400			520		V/mV
CMRR	Common-mode rejection ratio	$V_O = 1$ V, $R_S = 50$ Ω	$V_{IC} = V_{ICR}$ min,		88			94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{ID}$)	$V_O = 1$ V, $R_S = 50$ Ω	$V_{IC} = 1$ V,		86			86		dB
I_{DD}	Supply current	$V_O = 1$ V, No load	$V_{IC} = 1$ V,		12			20		µA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
       5. This range also applies to each input individually.
       6. At $V_{DD} = 5$ V, $V_O = 0.25$ V to 2 V; at $V_{DD} = 3$ V, $V_O = 0.5$ V to 1.5 V.

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TLV2322Y electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2324Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 1 MΩ		1.1			1.1		mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)				−0.3 to 2.3			−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,		1.9			3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = 100 mV,		115			95		mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 1 MΩ,		400			520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,		88			94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V,		86			86		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		24			39		μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1 – 4
α_{VIO}	Input offset voltage temperature coefficient	Distribution	5 – 8
I_{IB}	Input bias current	vs Free-air temperature	9
I_{IO}	Input offset current	vs Free-air temperature	9
V_{IC}	Common-mode input voltage	vs Supply voltage	10
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Free-air temperature vs Differential input voltage vs Low-level output current	14 15, 16 17 18
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	19 20 21, 22
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	23 24, 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	28
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	29 30
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	31 32 33
	Phase shift	vs Frequency	21, 22
V_n	Equivalent input noise voltage	vs Frequency	34

TEXAS
INSTRUMENTS
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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE**

V_DD = 3 V
T_A = 25°C
P Package

Percentage of Units – %

V_IO – Input Offset Voltage – mV
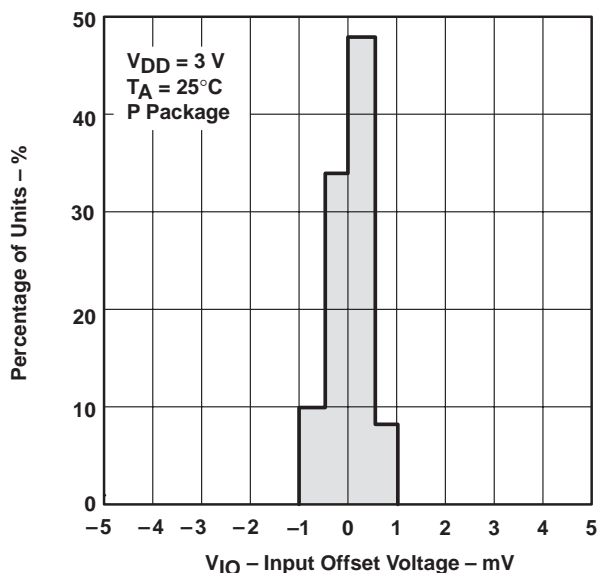
Figure 1

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE**

V_DD = 5 V
T_A = 25°C
P Package

Percentage of Units – %

V_IO – Input Offset Voltage – mV
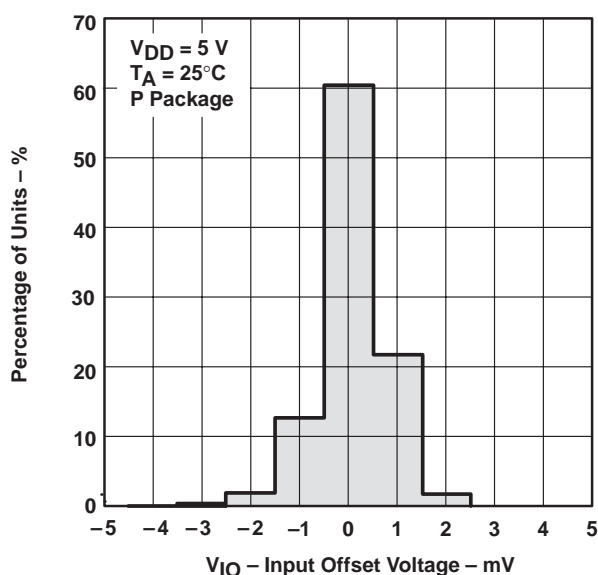
Figure 2

**DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE**

V_DD = 3 V
T_A = 25°C
N Package

Percentage of Units – %

V_IO – Input Offset Voltage – mV
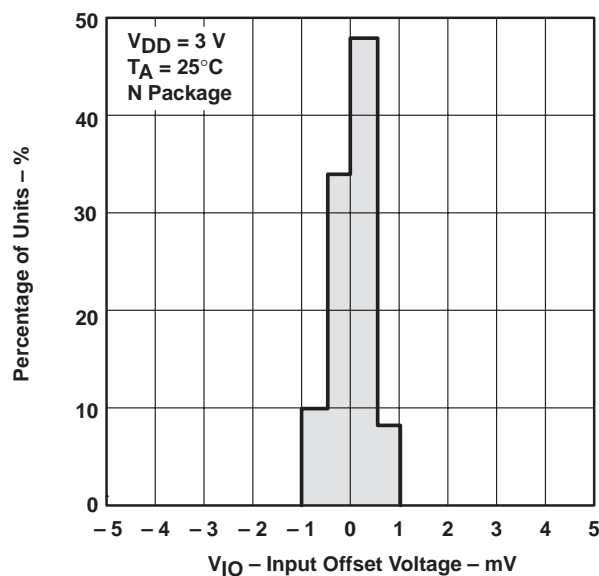
Figure 3

**DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE**
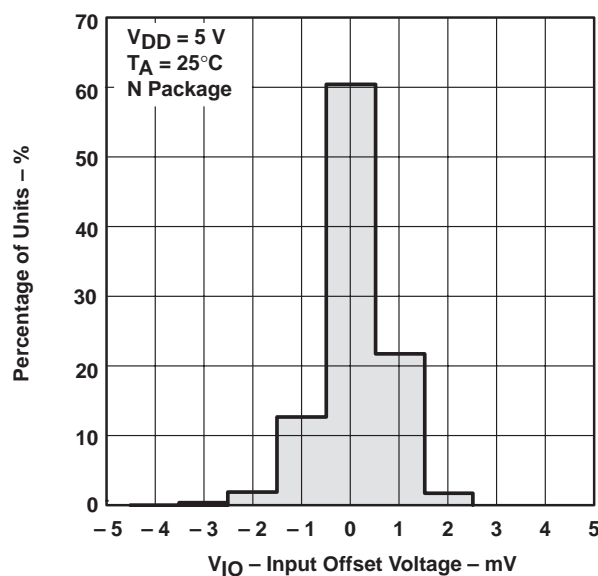
V_DD = 5 V
T_A = 25°C
N Package

Percentage of Units – %

V_IO – Input Offset Voltage – mV

Figure 4

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INSTRUMENTS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

V_{DD} = 3 V
T_A = 25°C to 85°C
P Package
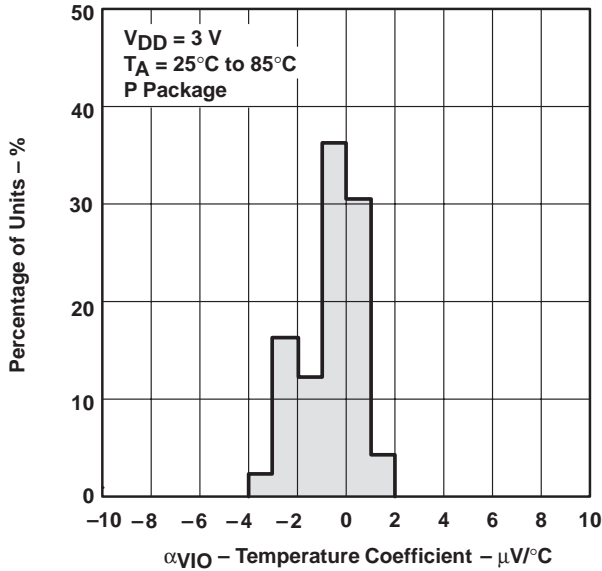
Figure 5

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

V_{DD} = 5 V
T_A = 25°C to 85°C
P Package
Outliers:
(1) 19.2 mV/°C
(1) 12.1 mV/°C
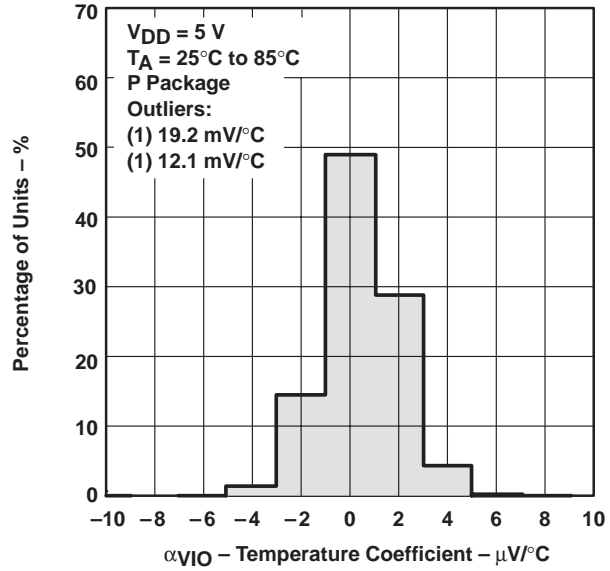
Figure 6

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

V_{DD} = 3 V
T_A = 25°C to 85°C
N Package
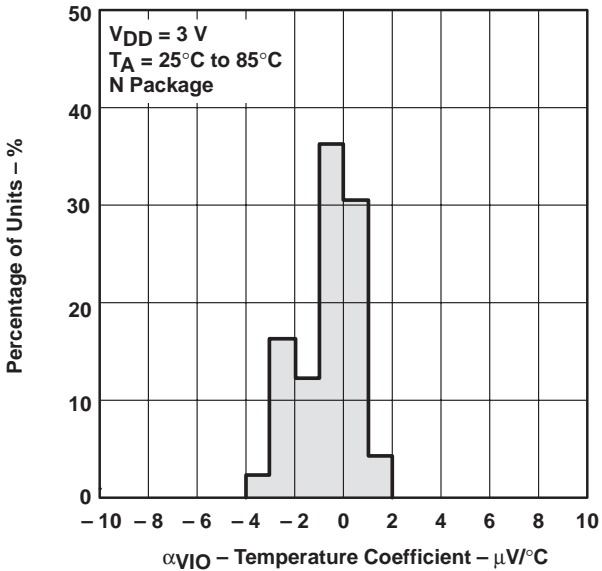
Figure 7

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

V_{DD} = 5 V
T_A = 25°C to 85°C
N Package Outliers:
(1) 19.2 mV/°C
(1) 12.1 mV/°C

Figure 8

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INSTRUMENTS

TYPICAL CHARACTERISTICS

**INPUT BIAS CURRENT AND INPUT OFFSET
CURRENT
vs
FREE-AIR TEMPERATURE**

V_{DD} = 3 V
V_{IC} = 1 V
See Note A

I_{IB}

I_{IO}
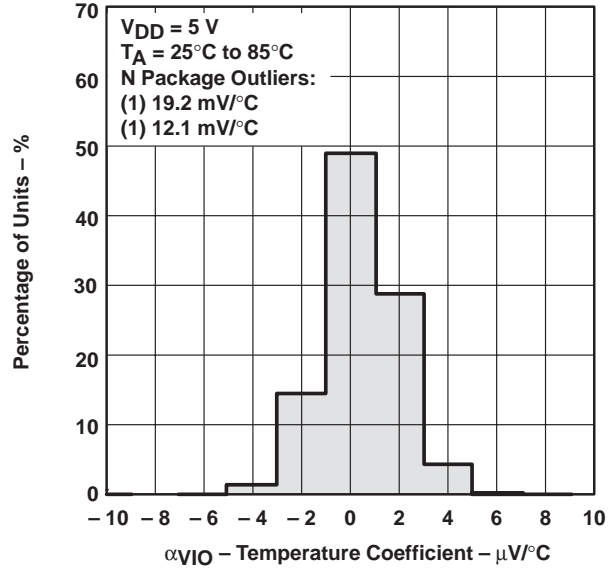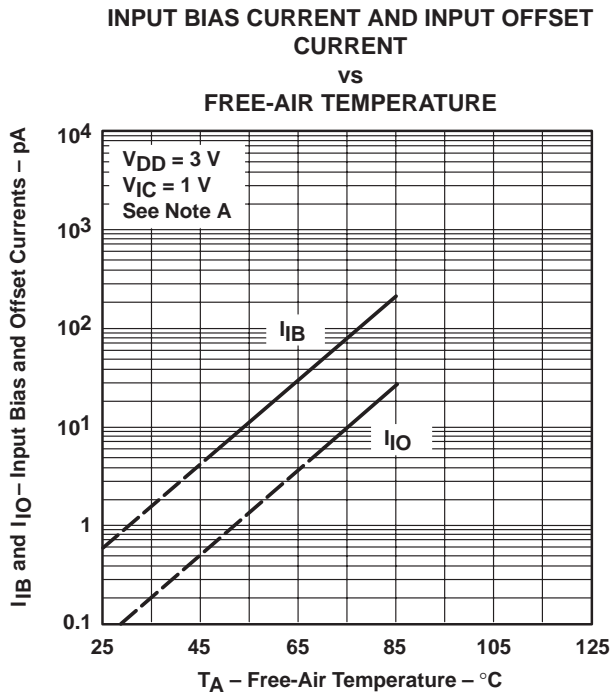
NOTE A: The typical values of input bias current and input offset
current below 5 pA were determined mathematically.

Figure 9

**COMMON-MODE INPUT VOLTAGE
vs
SUPPLY VOLTAGE**

T_A = 25°C
Positive Limit

Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

V_{IC} = 1 V
V_{ID} = 100 mV
T_A = 25°C

V_{DD} = 5 V

V_{DD} = 3 V

Figure 11

**HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE**

V_{IC} = 1 V
V_{ID} = 100 mV
R_L = 1 MΩ
T_A = 25°C
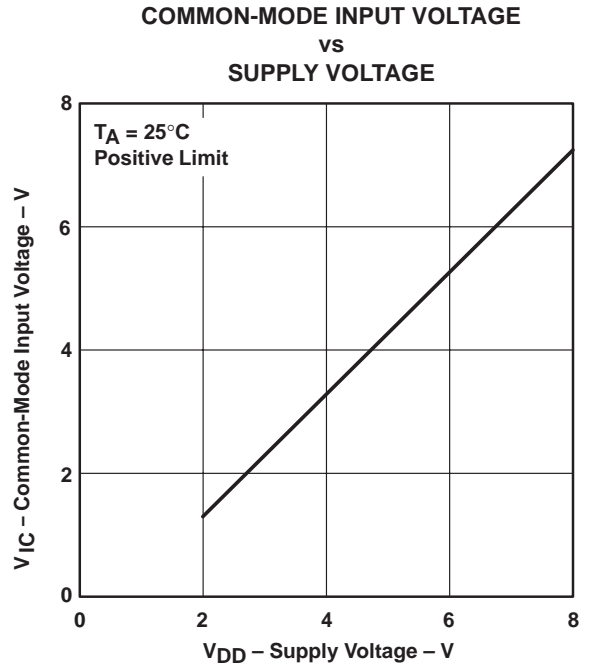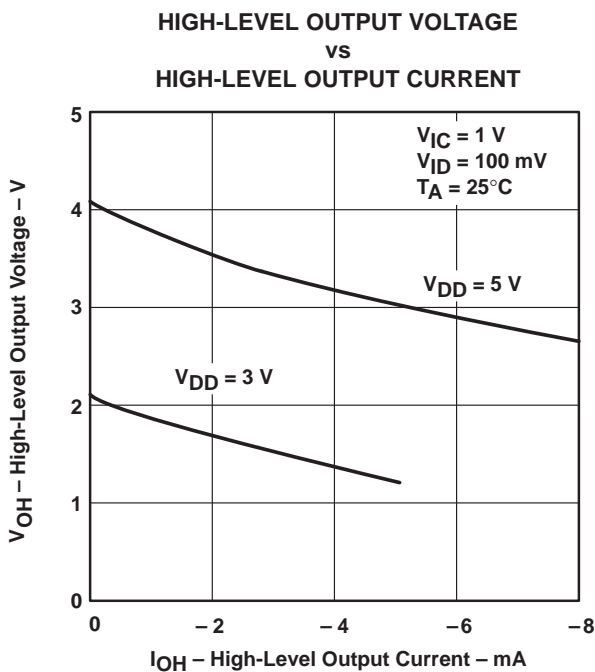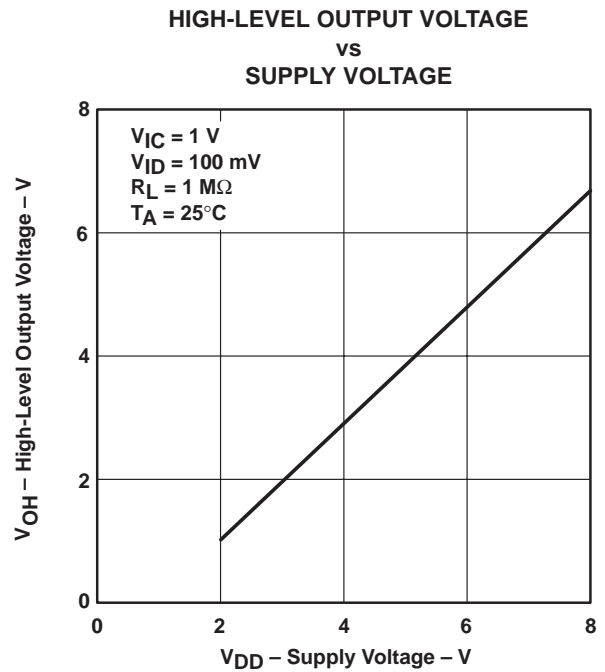
Figure 12

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE
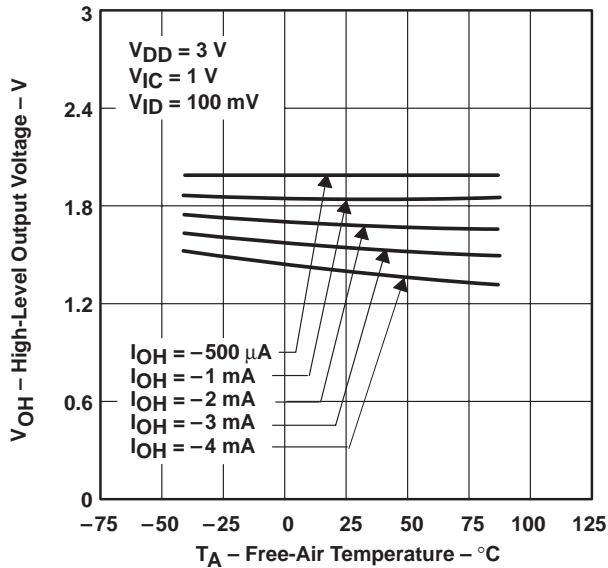
Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE
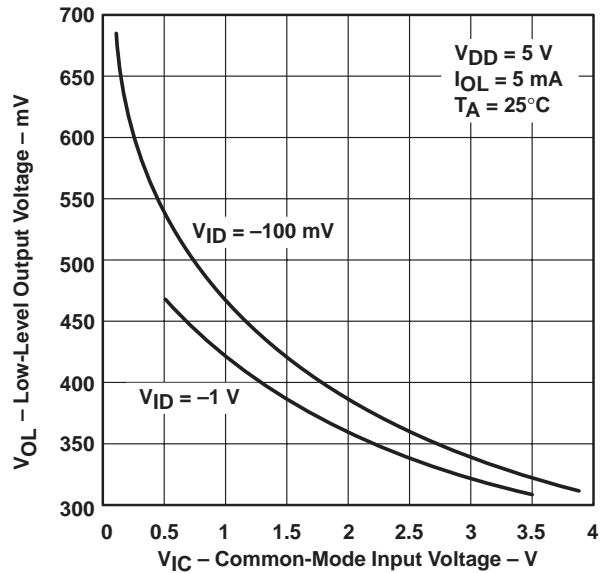
Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE
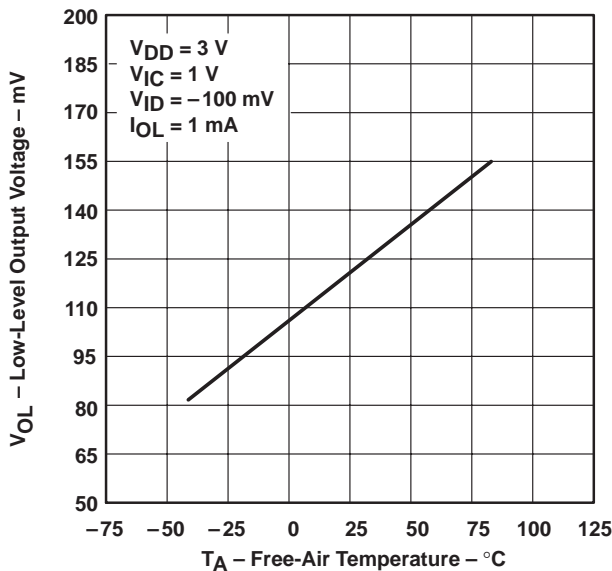
Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE
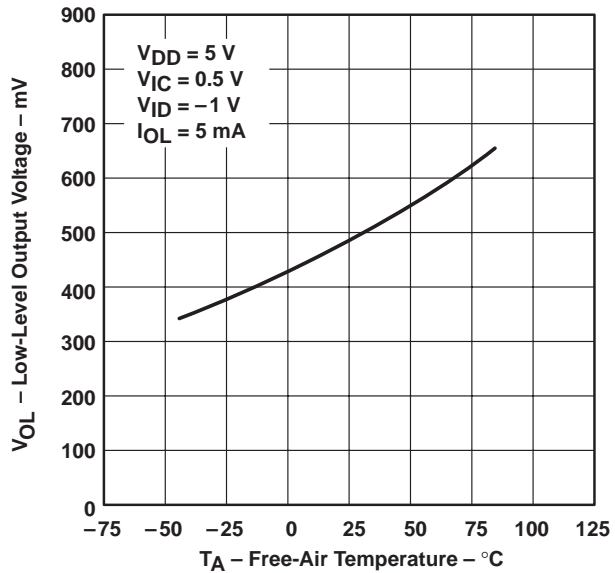
Figure 16

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TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 17

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 18

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

Figure 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 20

![Texas Instruments logo] **TEXAS INSTRUMENTS**
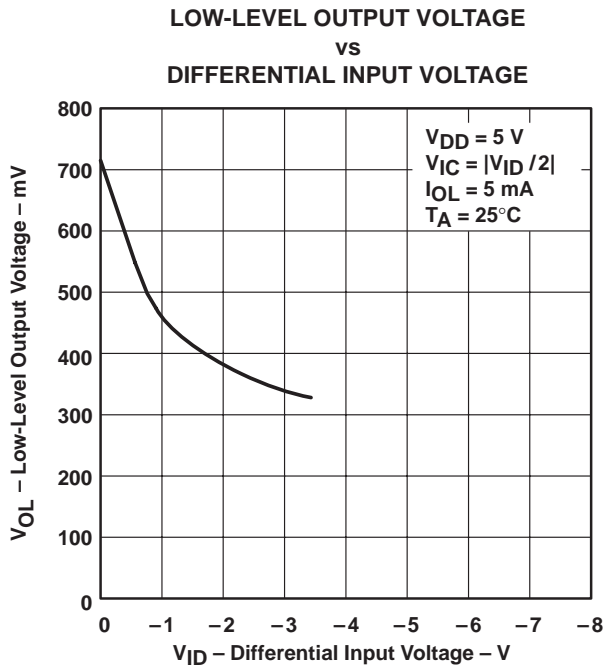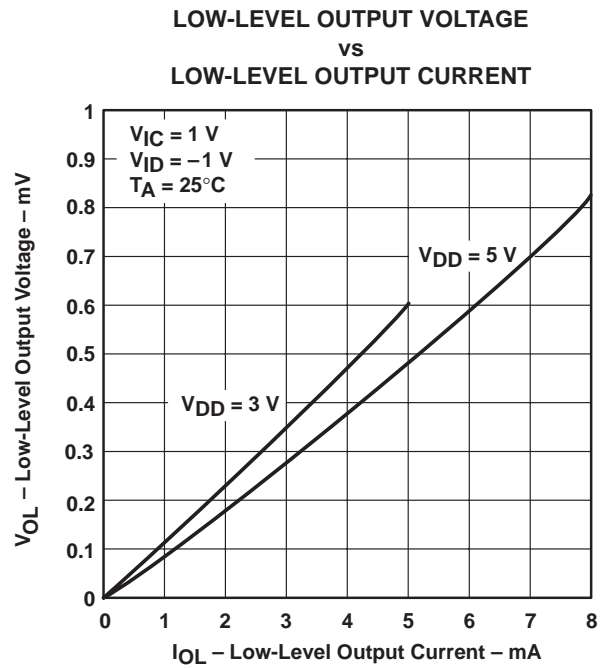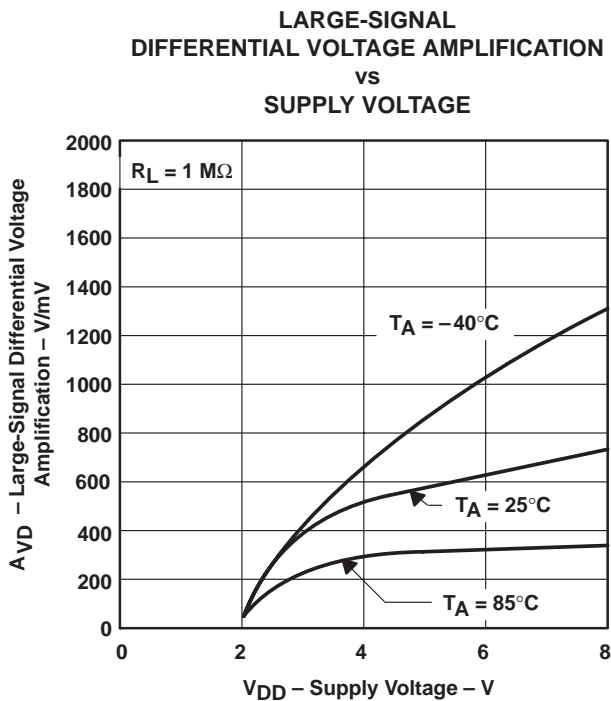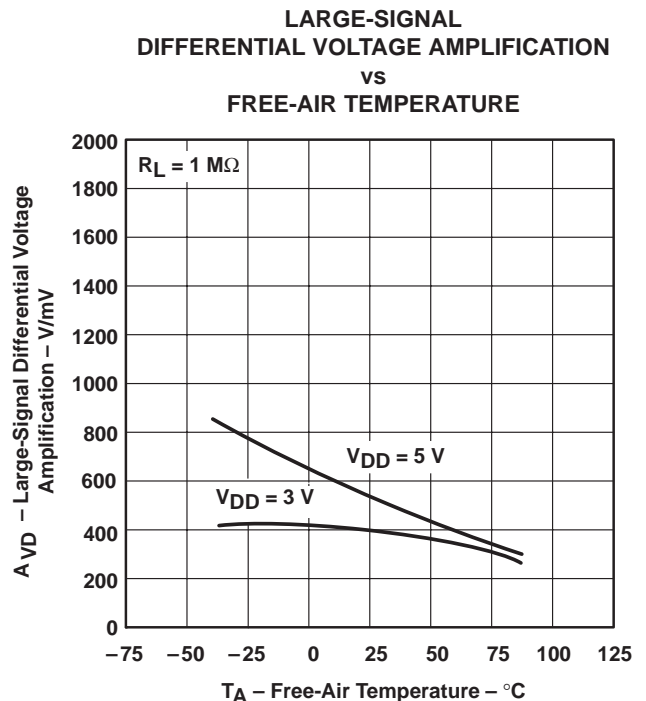
TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY
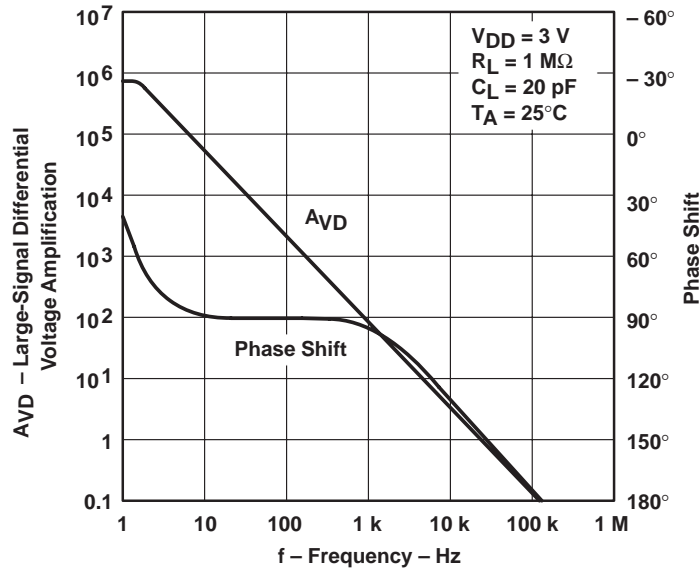
Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

Figure 22

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TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

V_{IC} = 1 V
V_O = 1 V
No Load

T_A = –40°C
T_A = 25°C
T_A = 85°C

I_{DD} – Supply Current – μA

V_{DD} – Supply Voltage – V

Figure 23

**TLV2322
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

V_{IC} = 1 V
V_O = 1 V
No Load

V_{DD} = 5 V
V_{DD} = 3 V

I_{DD} – Supply Current – μA

T_A – Free-Air Temperature – °C

Figure 24

**TLV2324
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

V_{IC} = 1 V
V_O = 1 V
No Load

V_{DD} = 5 V
V_{DD} = 3 V

I_{DD} – Supply Current – μA

T_A – Free-Air Temperature – °C

Figure 25

**SLEW RATE
vs
SUPPLY VOLTAGE**

V_{IC} = 1 V
$V_{I(PP)}$ = 1 V
A_V = 1
R_L = 1 MΩ
C_L = 20 pF
T_A = 25°C

SR – Slew Rate – V/μs

V_{DD} – Supply Voltage – V

Figure 26

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TYPICAL CHARACTERISTICS

**SLEW RATE
vs
FREE-AIR TEMPERATURE**

Figure 27

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

Figure 28

**UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE**

Figure 29

**UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE**

Figure 30

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TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

V_I = 10 mV
R_L = 1 MΩ
C_L = 20 pF
T_A = 25°C

ϕ_m – Phase Margin

V_{DD} – Supply Voltage – V

Figure 31

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

V_{DD} = 3 V

V_{DD} = 5 V

V_I = 10 mV
R_L = 1 MΩ
C_L = 20 pF

ϕ_m – Phase Margin

T_A – Free-Air Temperature – °C

Figure 32

PHASE MARGIN
vs
LOAD CAPACITANCE

V_{DD} = 3 V

V_{DD} = 5 V

V_I = 10 mV
R_L = 1 MΩ
T_A = 25°C

ϕ_m – Phase Margin

C_L – Load Capacitance – pF

Figure 33

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

V_{DD} = 3 V, 5 V
R_S = 20 Ω
T_A = 25°C

V_n – Equivalent Input Noise Voltage – nV/√Hz

f – Frequency – Hz

Figure 34

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV232x is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

(a) SINGLE SUPPLY

(b) SPLIT SUPPLY
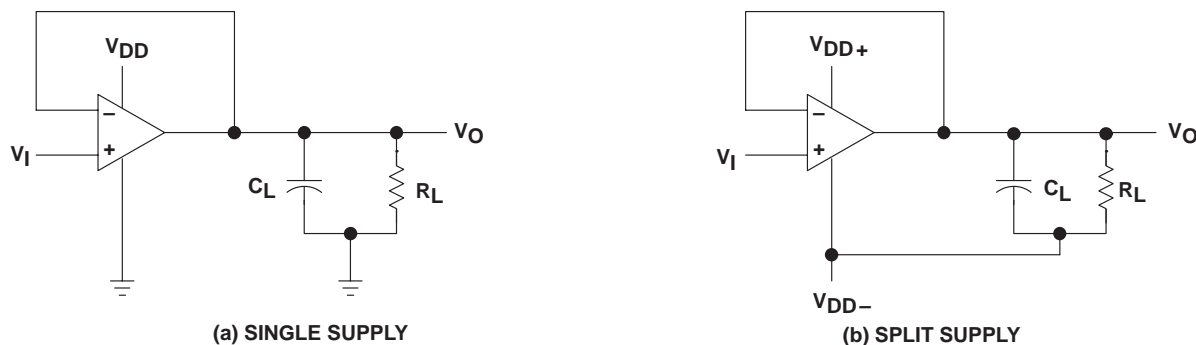
Figure 35. Unity-Gain Amplifier

(a) SINGLE SUPPLY

(b) SPLIT SUPPLY
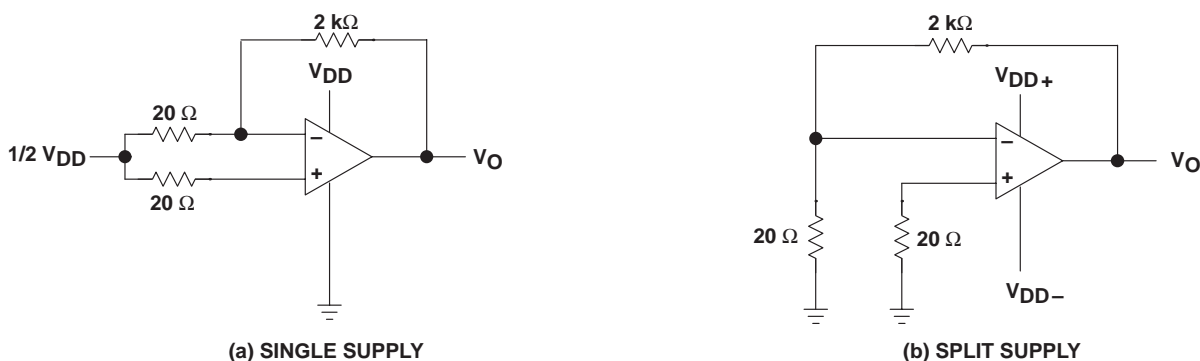
Figure 36. Noise-Test Circuits

(a) SINGLE SUPPLY

(b) SPLIT SUPPLY
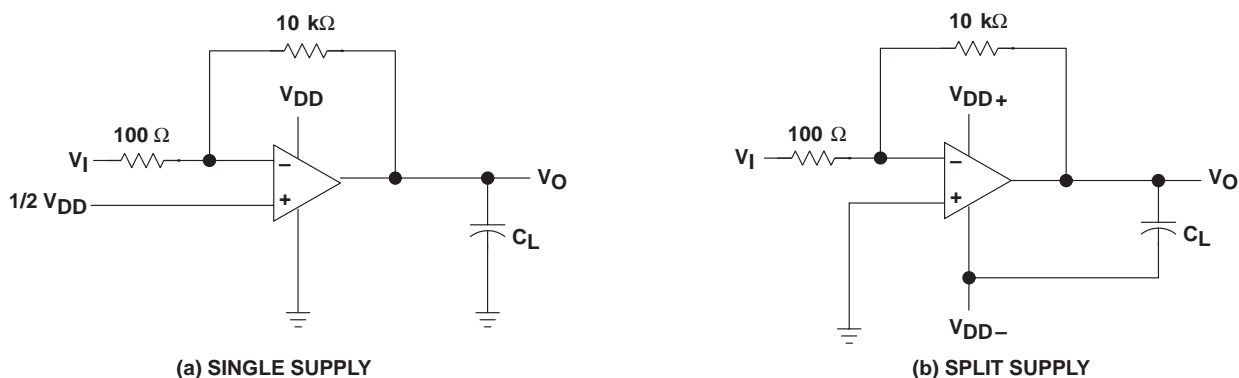
Figure 37. Gain-of-100 Inverting Amplifier

TEXAS
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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV232x operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 38). Leakages that would otherwise flow to the inputs are shunted away.

- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.
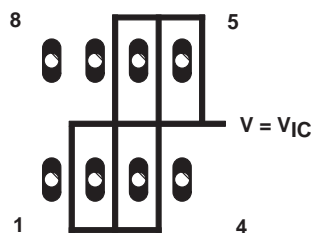

Figure 38. Isolation Metal Around Device Inputs
(P package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance that can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 35. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 39). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.
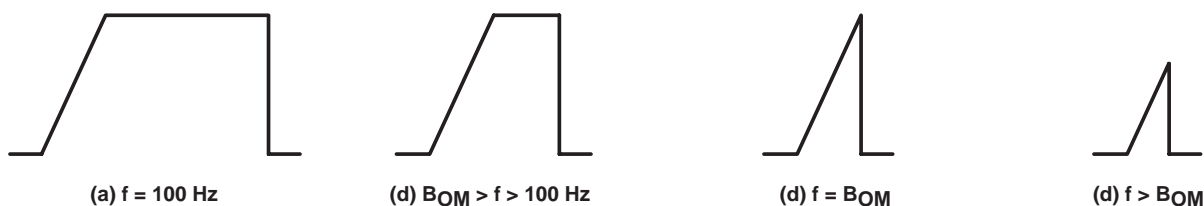

| (a) f = 100 Hz | (d) $B_{OM} > f > 100$ Hz | (d) $f = B_{OM}$ | (d) $f > B_{OM}$ |

Figure 39. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV232x performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426 (see Figure 40). The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.
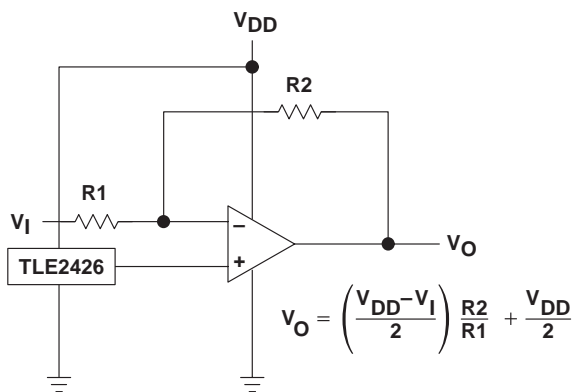

$$V_O = \left(\frac{V_{DD}-V_I}{2}\right)\frac{R2}{R1} + \frac{V_{DD}}{2}$$

Figure 40. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV232x works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 41); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.

- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

(a) COMMON-SUPPLY RAILS

(b) SEPARATE-BYPASSED SUPPLY RAILS (preferred)
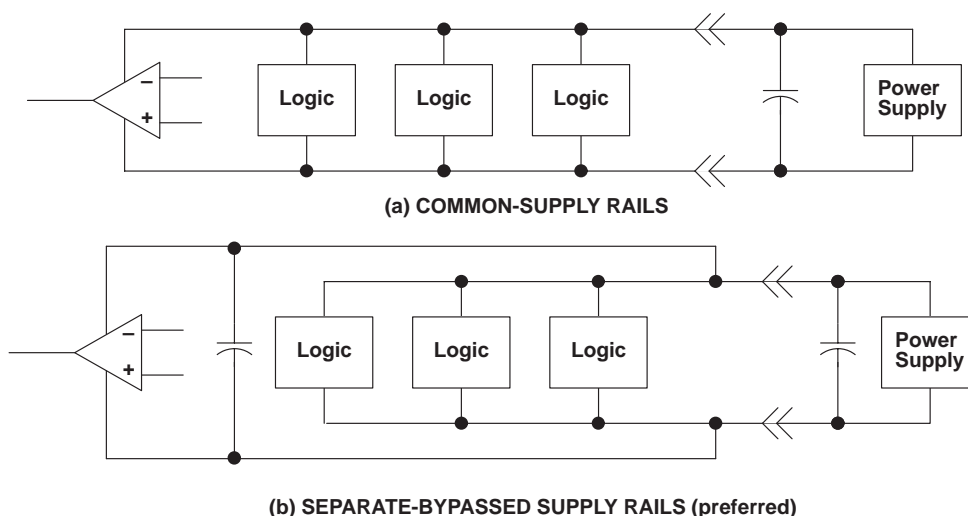
Figure 41. Common Versus Separate Supply Rails

input characteristics

The TLV232x is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower the range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV232x very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV232x is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 38 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 42).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

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APPLICATION INFORMATION

input characteristics (continued)

(a) NONINVERTING AMPLIFIER   (b) INVERTING AMPLIFIER   (c) UNITY-GAIN AMPLIFIER
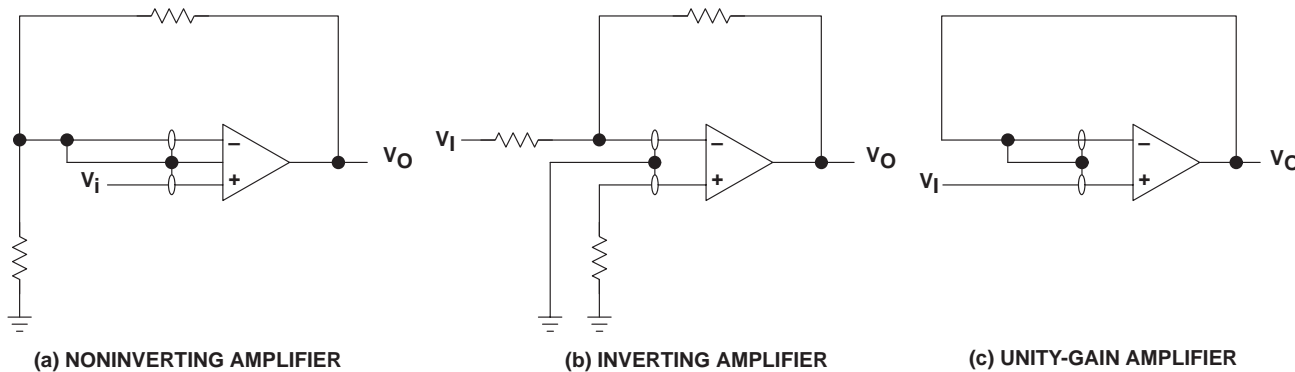
Figure 42. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV232x result in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.
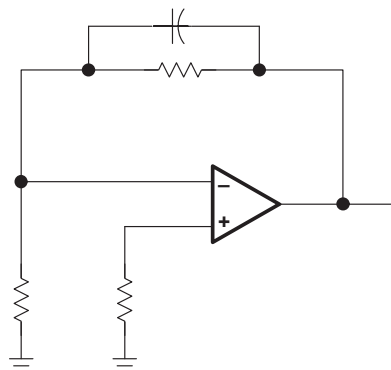
Figure 43. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV232x incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD can result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV232x inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal-protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage

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TEXAS INSTRUMENTS

APPLICATION INFORMATION

by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV232x is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV232x possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 44). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV232x are measured using a 20-pF load. The device drives

$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup Current
Required by the
Operational Amplifier
(typically 500 µA)

Figure 44. Resistive Pullup to Increase V_{OH}

$T_A = 25°C$
$f = 1 kHz$
$V_{I(PP)} = 1 V$
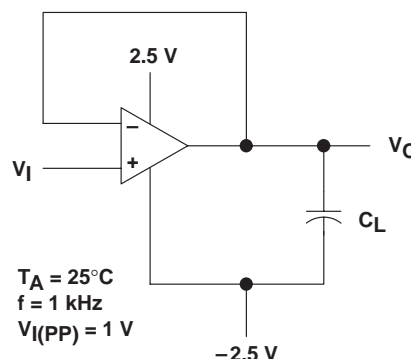
Figure 45. Test Circuit for Output Characteristics

higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 45 and Figure 46). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.
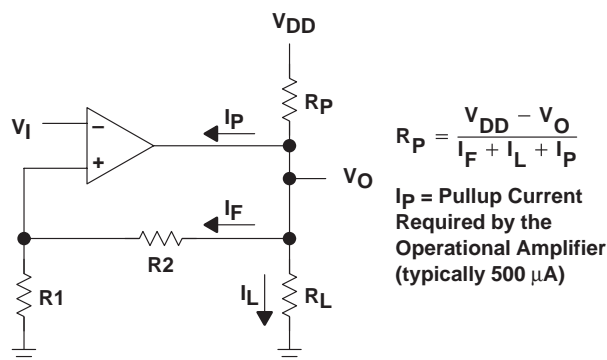
APPLICATION INFORMATION

output characteristics (continued)

(a) C$_L$ = 20 pF, R$_L$ = NO LOAD   (b) C$_L$ = 260 pF, R$_L$ = NO LOAD   (c) C$_L$ = 310 pF, R$_L$ = NO LOAD
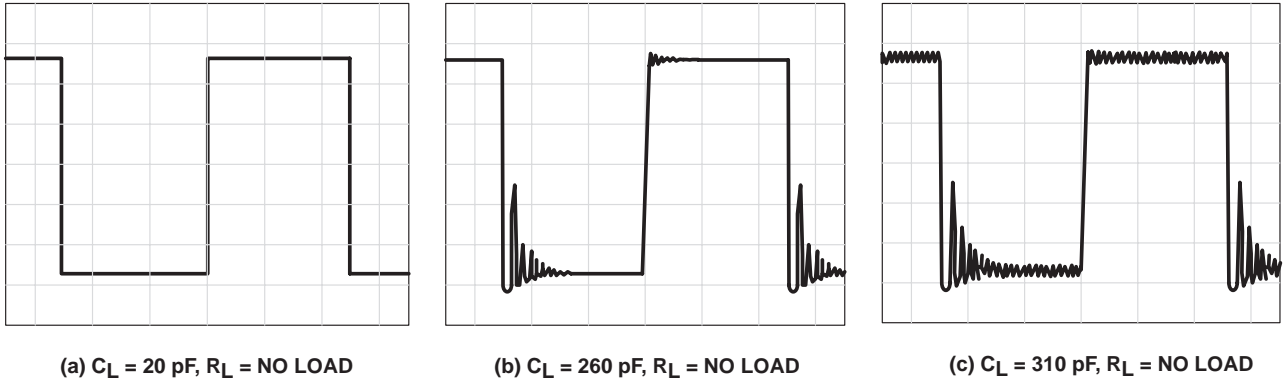
Figure 46. Effect of Capacitive Loads

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MECHANICAL INFORMATION

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE
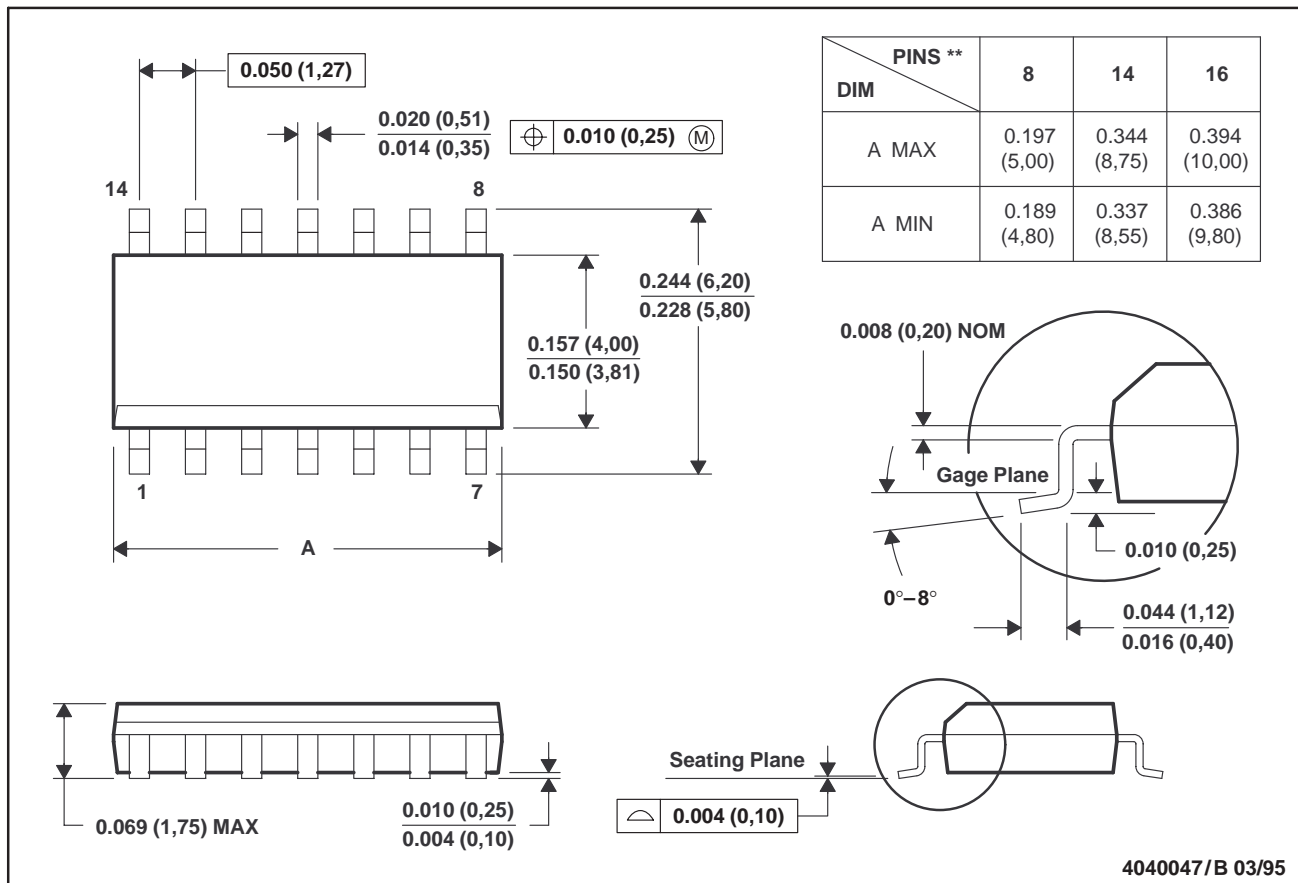
14 PIN SHOWN

PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.014\ (0,35)}$

⌖ 0.010 (0,25) Ⓜ

14 8

$\dfrac{0.244\ (6,20)}{0.228\ (5,80)}$

$\dfrac{0.157\ (4,00)}{0.150\ (3,81)}$

1 7

A

0.008 (0,20) NOM

Gage Plane

0°–8°

0.010 (0,25)

$\dfrac{0.044\ (1,12)}{0.016\ (0,40)}$

0.069 (1,75) MAX

$\dfrac{0.010\ (0,25)}{0.004\ (0,10)}$

Seating Plane

△ 0.004 (0,10)

4040047 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
   D. Four center pins are connected to die mount pad.
   E. Falls within JEDEC MS-012

MECHANICAL INFORMATION

N (R-PDIP-T**)   **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN
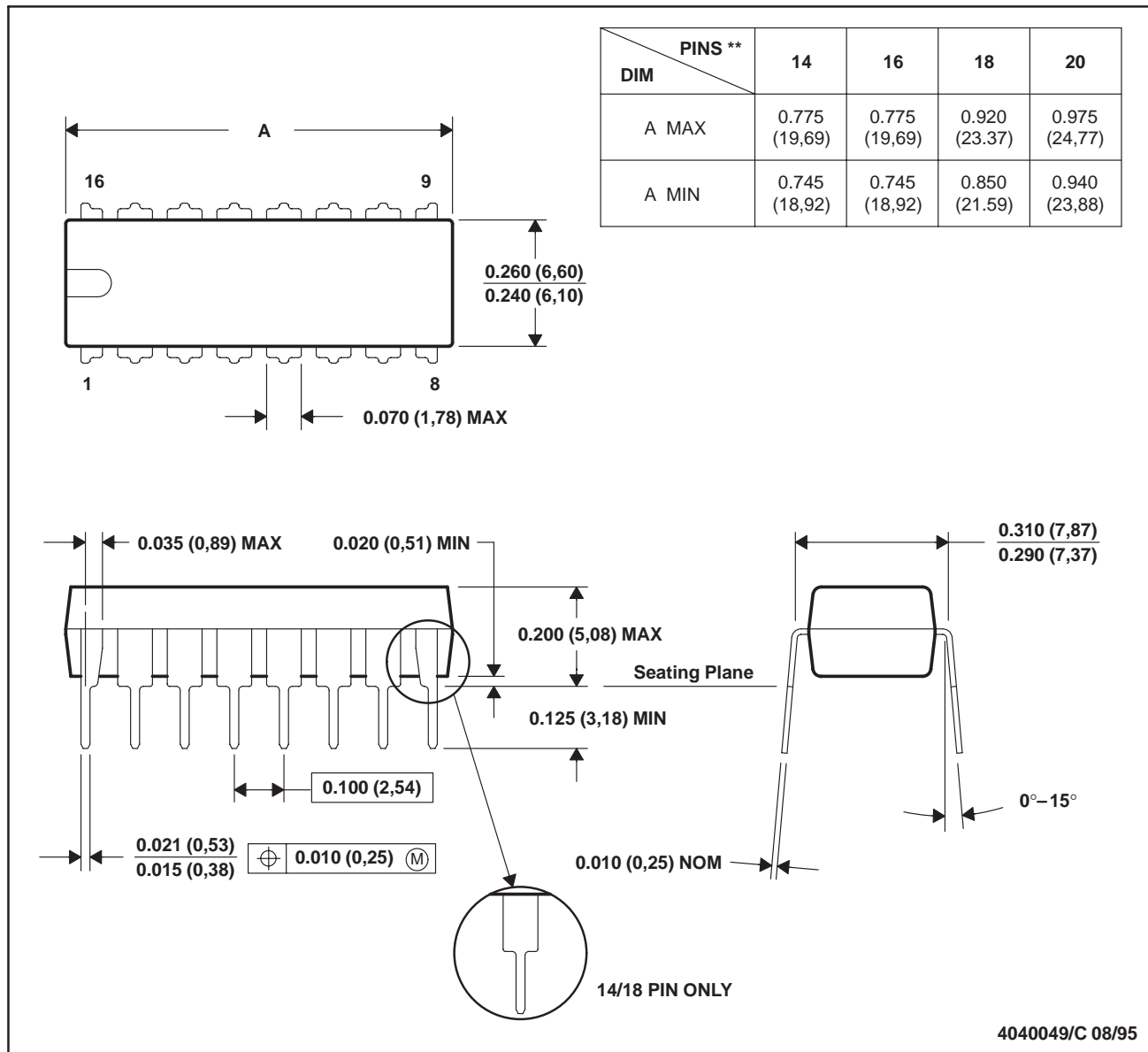
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

0.260 (6,60)
0.240 (6,10)

0.070 (1,78) MAX

0.035 (0,89) MAX   0.020 (0,51) MIN

0.310 (7,87)
0.290 (7,37)

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ | 0.010 (0,25) (M)

0°–15°

0.010 (0,25) NOM

14/18 PIN ONLY

4040049/C 08/95

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

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MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**
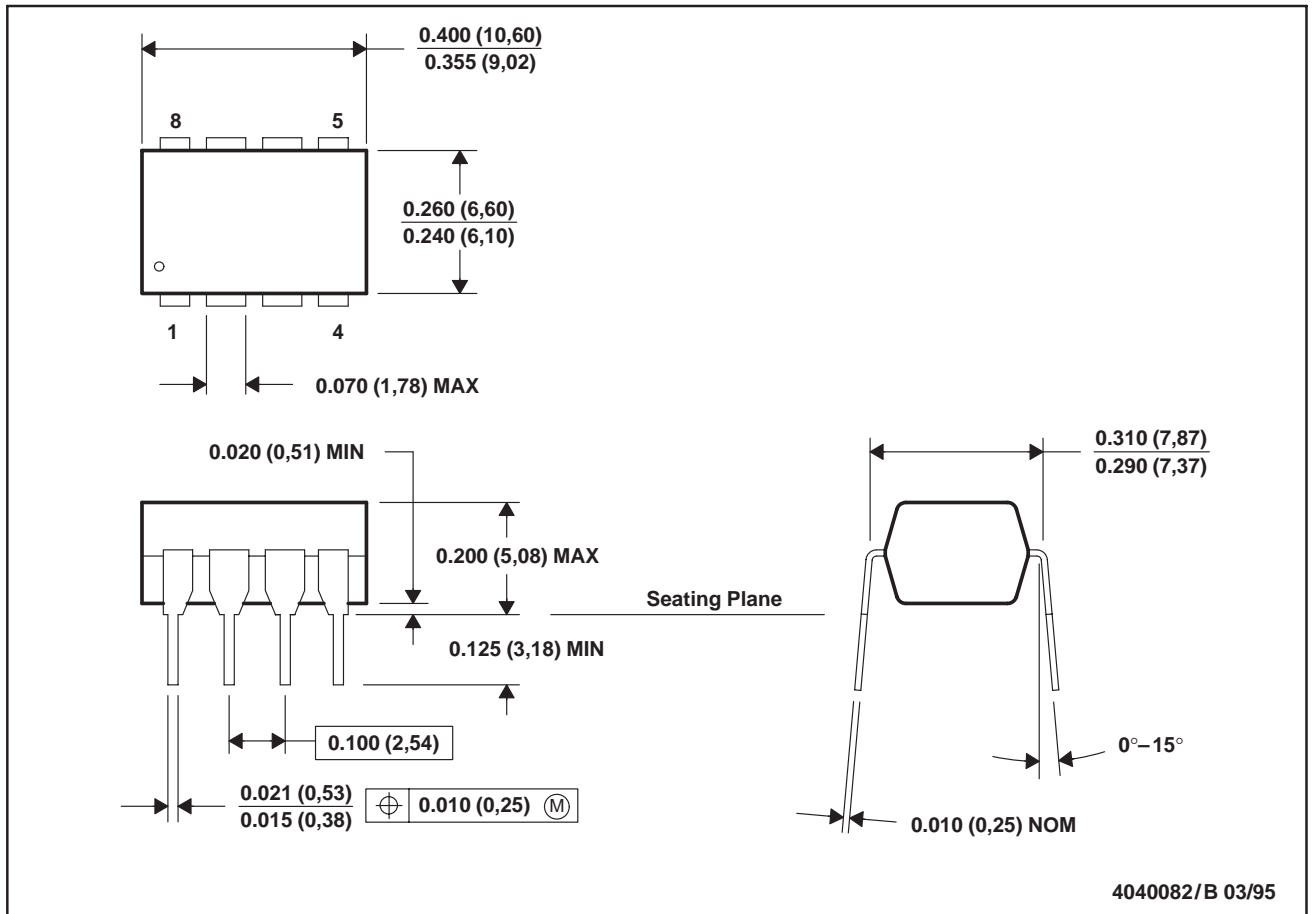
4040082/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
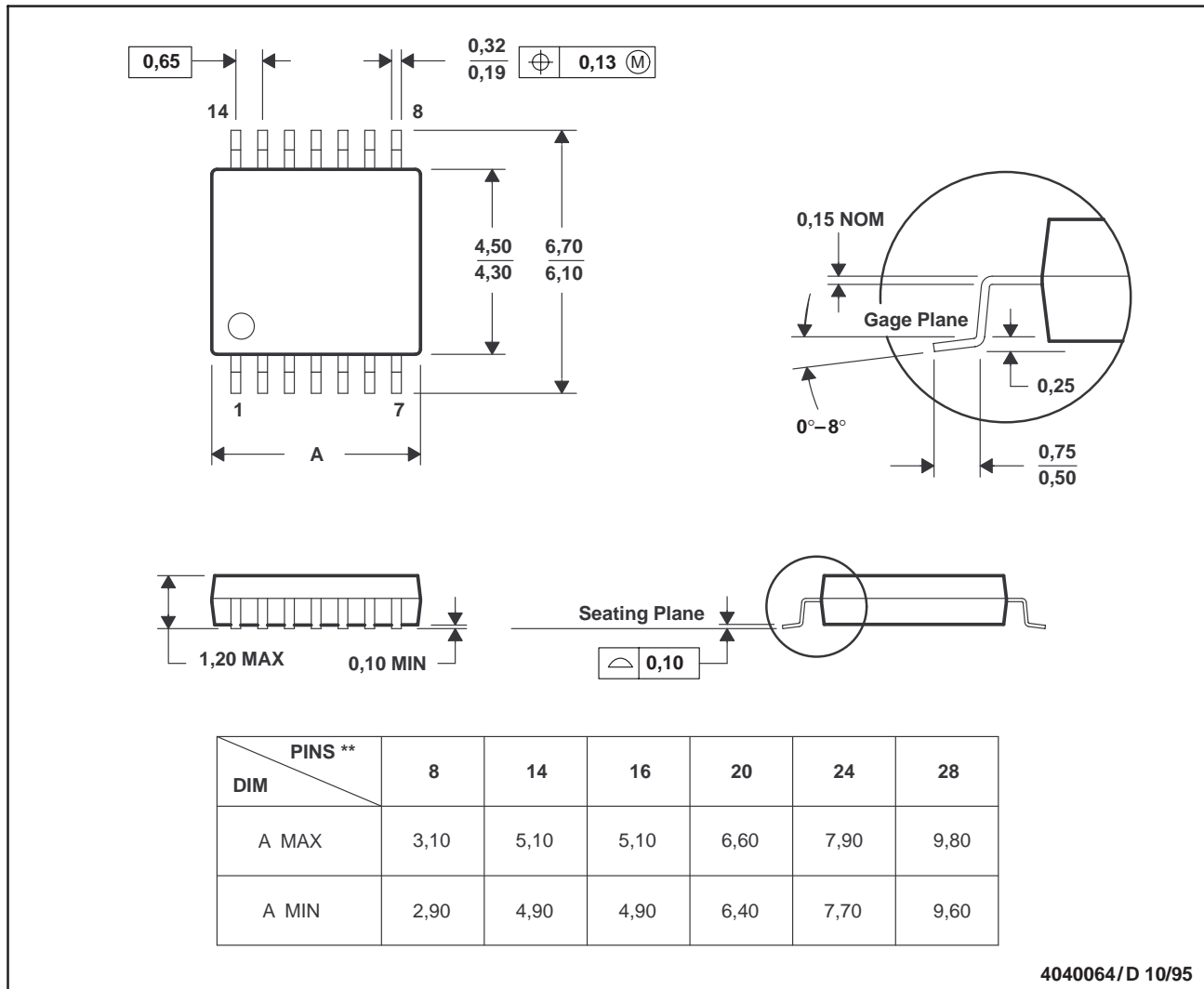
4040064 / D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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