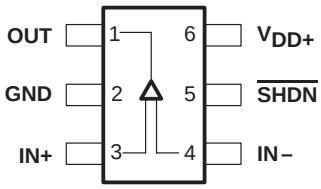
- **Supply Current . . . 23 μA/Channel**
- **Gain-Bandwidth Product . . . 220 kHz**
- **Output Drive Capability . . . ±10 mA**
- **Input Offset Voltage . . . 20 μV (typ)**
- **V_{DD} Range . . . 2.7 V to 6 V**
- **Power Supply Rejection Ratio . . . 106 dB**
- **Ultra-Low Power Shutdown Mode**
  I_{DD} . . . 16 nA/ch
- **Rail-To-Rail Input/Output (RRIO)**
- **Ultra-Small Packaging**
  - **5 or 6 Pin SOT-23 (TLV2450/1)**
  - **8 or 10 Pin MSOP (TLV2452/3)**

TLV2450
DBV† PACKAGE
(TOP VIEW)



† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

description

The TLV245x is a family of rail-to-rail input/output operational amplifiers that set a new performance point for supply current and ac performance. These devices consume a mere 23 μA/channel while offering 220 kHz of gain bandwidth product; much higher than competitive devices with similar supply current levels. Along with increased ac performance, the amplifier provides high output drive capability, solving a major shortcoming of older micropower rail-to-rail input/output operational amplifiers. The TLV245x can swing to within 250 mV of each supply rail while driving a 2.5-mA load. Both the inputs and outputs swing rail-to-rail for increased dynamic range in low-voltage applications. This performance makes the TLV245x family ideal for portable medical equipment, patient monitoring systems, and data acquisition circuits.

Three members of the family (TLV2450/3/5) offer a shutdown terminal for conserving battery life in portable applications. During shutdown, the outputs are placed in a high-impedance state and the amplifier consumes only 16 nA/channel. The family is fully specified at 3 V and 5 V across an expanded industrial temperature range (–40°C to 125°C). The singles and duals are available in the SOT23 and MSOP packages, while the quads are available in TSSOP. The TLV2450 offers an amplifier with shutdown functionality all in a 6-pin SOT23 package, making it perfect for high density circuits.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2450	1	8	8	6‡	—	—	Yes	UNIV-OPAMP–2
TLV2451	1	8	8	5	—	—	—	UNIV-OPAMP–1
TLV2452	2	8	8	—	—	8	—	UNIV-OPAMP–1
TLV2453	2	14	14	—	—	10	Yes	UNIV-OPAMP–2
TLV2454	4	14	14	—	14	—	—	—
TLV2455	4	16	16	—	16	—	Yes	—

‡ This device is in the Product Preview stage of development. Contact your local TI sales office for availability.

TLV2450 and TLV2451 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	SOT-23		PLASTIC DIP (P)	
		(DBV)†	SYMBOL		
0°C to 70°C	TLV2450CD§ TLV2451CD	TLV2450CDBV TLV2451CDBV	VAQC VARC	TLV2450CP TLV2451CP	TLV2450Y TLV2451Y
–40°C to 125°C	TLV2450ID§ TLV2451ID	TLV2450IDBV TLV2451IDBV	VAQI VARI	TLV2450IP TLV2451IP	— —
	TLV2450AID TLV2451AID	— —	— —	TLV2450AIP TLV2451AIP	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2450CDR).
‡ Chip forms are tested at T_A = 25°C only.
§ This device is in the Prodauct Preview stage of development. Contacat your local TI sales office for availability.

TLV2452 and TLV2453 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES							CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)	
		(DGK)†	SYMBOL§	(DGS)†	SYMBOL§			
0°C to 70°C	TLV2452CD TLV2453CD	TLV2452CDGK —	xxTIABI —	— TLV2453CDGS	— xxTIABK	— TLV2453CN	TLV2452CP —	TLV2452Y TLV2453Y
–40°C to 125°C	TLV2452ID TLV2453ID	TLV2452IDGK —	xxTIABJ —	— TLV2453IDGS	— xxTIABL	— TLV2453IN	TLV2452IP —	— —
	TLV2452AID TLV2453AID	— —	— —	— —	— —	— TLV2453AIN	TLV2452AIP —	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2452CDR).
‡ Chip forms are tested at T_A = 25°C only.
§ xx represents the device date code.

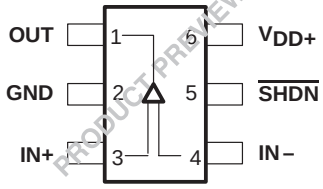
TLV2454 and TLV2455 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PW)†	
0°C to 70°C	TLV2454CD TLV2455CD	TLV2454CN TLV2455CN	TLV2454CPW TLV2455CPW	TLV2454Y TLV2455Y
–40°C to 125°C	TLV2454ID TLV2455ID	TLV2454IN TLV2455IN	TLV2454IPW TLV2455IPW	— —
	TLV2454AID TLV2455AID	TLV2454AIN TLV2455AIN	TLV2454AIPW TLV2455AIPW	— —

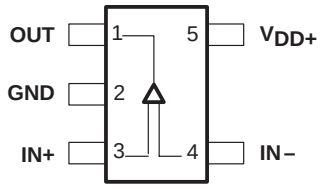
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2454CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV245x PACKAGE PINOUTS

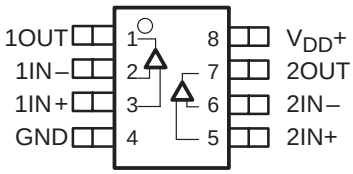
TLV2450
DBV PACKAGE
(TOP VIEW)



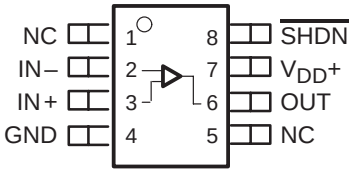
TLV2451
DBV PACKAGE
(TOP VIEW)



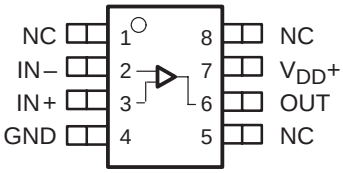
TLV2452
D, DGN, OR P PACKAGE
(TOP VIEW)



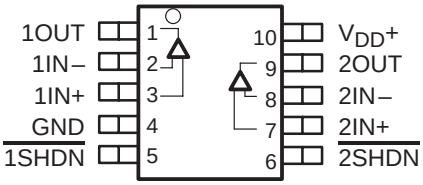
TLV2450
D OR P PACKAGE
(TOP VIEW)



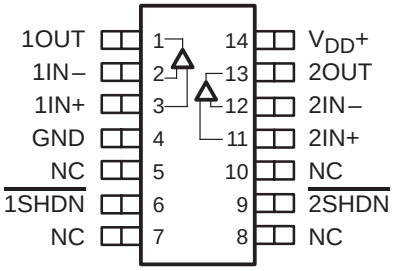
TLV2451
D OR P PACKAGE
(TOP VIEW)



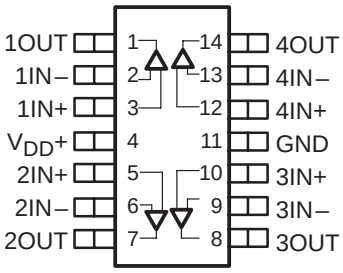
TLV2453
DGS PACKAGE
(TOP VIEW)



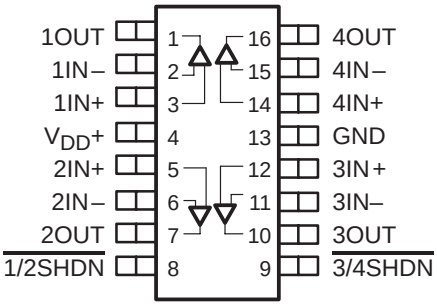
TLV2453
D OR N PACKAGE
(TOP VIEW)



TLV2454
D, N, OR PW PACKAGE
(TOP VIEW)



TLV2455
D, N, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Differential input voltage, V_{ID} . . . . . $\pm V_{DD}$
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 125°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to V_{DD-}.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGK (8)	54.2	259.9	481 mW
DGS (10)	54.1	257.7	485 mW
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW
PW (16)	28.7	161.4	774 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		V_{DD-}	V_{DD+}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV245x	V_{DD} = ±1.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		20	1500	μV
					Full range			2000	
		TLV245xA			25°C		20	1000	
					Full range			1300	
α_{VIO}	Temperature coefficient of input offset voltage						0.3		μV/°C
I_{IO}	Input offset current				25°C		0.3	4.5	nA
					Full range			5.5	
I_{IB}	Input bias current				25°C		0.9	5	nA
					Full range			7	
V_{ICR}	Common-mode input voltage range		CMRR > 70 dB	R_S = 50 Ω	25°C	0 to 3			V
			CMRR > 52 dB	R_S = 50 Ω	Full range	0 to 3			
V_{OH}	High-level output voltage		V_{IC} = 1.5 V,	I_{OH} = –500 μA	25°C	2.85	2.95		V
					Full range	2.83			
V_{OL}	Low-level output voltage		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		0.09	0.16	V
					Full range			0.2	
I_{OS}	Short-circuit output current		Sourcing		25°C	4	12		mA
					Full range	3			
			Sinking		25°C	2	7		
					Full range	1			
I_O	Output current		V_O = 0.5 V from rail		25°C		±4		mA
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)}$ = 1 V,	R_L = 10 kΩ	25°C	96	110		dB
					Full range	91			
$r_{i(d)}$	Differential input resistance				25°C		10^9		Ω
C_{IC}	Common-mode input capacitance		f = 10 kHz		25°C		4.5		pF
z_o	Closed-loop output impedance		f = 10 kHz,	A_V = 10	25°C		80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 3 V, R_S = 50 Ω	TLV245xC	Full range	60			dB
				TLV245xI		52			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	76	89		dB
					Full range	74			
			V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	88	106		
					Full range	84			

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load		25°C		23	35	μA
			TLV245xC	Full range			40	
			TLV245xI	Full range			45	
$V_{(ON)}$	Turnon voltage level	A_V = 1		25°C		1.73		V
$V_{(OFF)}$	Turnoff voltage level	A_V = 1		25°C		1.45		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)	$\overline{SHDN}$ = < 1.45 V		25°C		12	70	nA
			TLV245xC	Full range			70	
			TLV245xI	Full range			80	

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	0.05	0.11		V/μs
				Full range	0.02			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		49		nV/√Hz
		f = 1 kHz		25°C		51		
I_n	Equivalent input noise current	f = 1 kHz		25°C		3.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 1.5 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.04%		
			A_V = 10			0.3%		
			A_V = 100			1.5%		
$t_{(on)}$	Amplifier turnon time	A_V = 5, Measured at 50% point	R_L = OPEN,	25°C		59		μs
$t_{(off)}$	Amplifier turnoff time			25°C		836		ns
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		200		kHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		26		μs
			0.01%			31		
		$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 56 pF, R_L = 10 kΩ	0.1%			26		
			0.01%			31		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		56°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		7		dB

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV245x	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		20	1500	μV
					Full range			2000	
		TLV245xA			25°C		20	1000	
					Full range			1300	
α_{VIO}	Temperature coefficient of input offset voltage						0.3		μV/°C
I_{IO}	Input offset current				25°C		0.3	4.5	nA
					Full range			5.5	
I_{IB}	Input bias current				25°C		0.5	5	nA
					Full range			7	
V_{ICR}	Common-mode input voltage range		CMRR > 70 dB	R_S = 50 Ω	25°C	0 to 5			V
			CMRR > 52 dB	R_S = 50 Ω	Full range	0 to 5			
V_{OH}	High-level output voltage		V_{IC} = 2.5 V,	I_{OH} = –500 μA	25°C	4.87	4.97		V
					Full range	4.85			
V_{OL}	Low-level output voltage		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.07	0.15	V
					Full range			0.16	
I_{OS}	Short-circuit output current		Sourcing		25°C	20	32		mA
					Full range	18			
			Sinking		25°C	12	18		
					Full range	10			
I_O	Output current		V_O = 0.5 V from rail		25°C		±10		mA
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)}$ = 3 V,	R_L = 10 kΩ	25°C	96	103		dB
					Full range	91			
$r_{i(d)}$	Differential input resistance				25°C		10^9		Ω
C_{IC}	Common-mode input capacitance		f = 10 kHz		25°C		4.5		pF
z_o	Closed-loop output impedance		f = 10 kHz,	A_V = 10	25°C		45		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 5 V, R_S = 50 Ω	TLV245xC	Full range	66			dB
				TLV245xI		52			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	76	89		dB
					Full range	74			
			V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	88	106		
					Full range	84			

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load		25°C		23	42	μA
			TLV245xC	Full range			44	
			TLV245xI	Full range			46	
$V_{(ON)}$	Turnon voltage level	A_V = 1		25°C		1.73		V
$V_{(OFF)}$	Turnoff voltage level	A_V = 1		25°C		1.45		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)	$\overline{SHDN}$ = < 1.45 V		25°C		16	65	nA
			TLV245xC	Full range			65	
			TLV245xI	Full range			80	

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 150 pF, R_L = 10 kΩ		25°C	0.05	0.11		V/μs
				Full range	0.02			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		49		nV/√Hz
		f = 1 kHz		25°C		52		
I_n	Equivalent input noise current	f = 1 kHz		25°C		3.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.18%		
			A_V = 100			0.9%		
$t_{(on)}$	Amplifier turnon time	A_V = 5, Measured at 50% point	R_L = OPEN,	25°C		59		μs
$t_{(off)}$	Amplifier turnoff time			25°C		836		ns
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		220		kHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		24		μs
			0.01%			30		
		$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 56 pF, R_L = 10 kΩ	0.1%			25		
			0.01%			30		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		56°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		7		dB

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IO}	Input offset current	vs Common-mode input voltage vs Free-air temperature	3, 4 7, 8
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5, 6 7, 8
A_{VD}	Differential voltage amplification	vs Frequency	9, 10
	Phase	vs Frequency	9, 10
V_{OL}	Low-level output voltage	vs Low-level output current	11, 13
V_{OH}	High-level output voltage	vs High-level output current	12, 14
Z_o	Output impedance	vs Frequency	15, 16
CMRR	Common-mode rejection ratio	vs Frequency	17
PSRR	Power supply rejection ratio	vs Frequency	18
I_{DD}	Supply current	vs Supply voltage	19
I_{DD}	Supply current	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD + N	Total harmonic distortion plus noise	vs Frequency	22, 23
ϕ_m	Phase margin	vs Load capacitance	24
	Gain-bandwidth product	vs Supply voltage	25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	28
	Crosstalk	vs Frequency	29, 30
	Small-signal follower pulse response	vs Time	31, 33
	Large-signal follower pulse response	vs Time	32, 34
	Shutdown on supply current	vs Time	35
	Shutdown off supply current	vs Time	36
	Shutdown supply current	vs Free-air temperature	37
	Shutdown supply current	vs Time	38 – 41
	Shutdown pulse	vs Time	38 – 41
	Shutdown off pulse response	vs Time	42, 43
	Shutdown on pulse response	vs Time	44, 45
	Shutdown reverse isolation	vs Frequency	46
	Shutdown forward isolation	vs Frequency	47

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

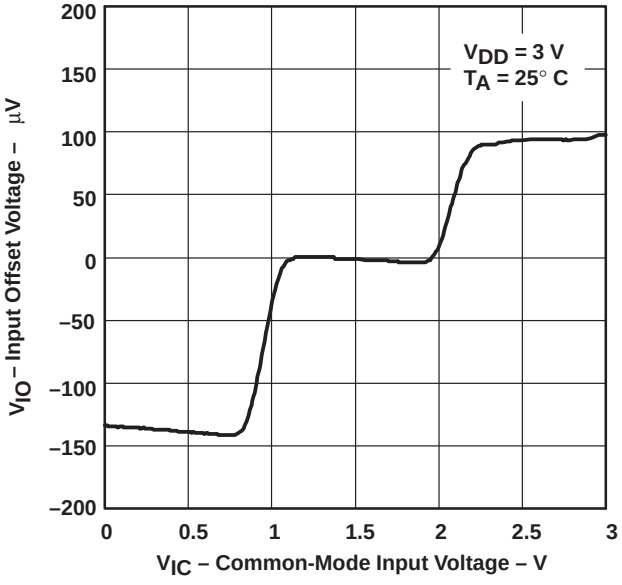


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

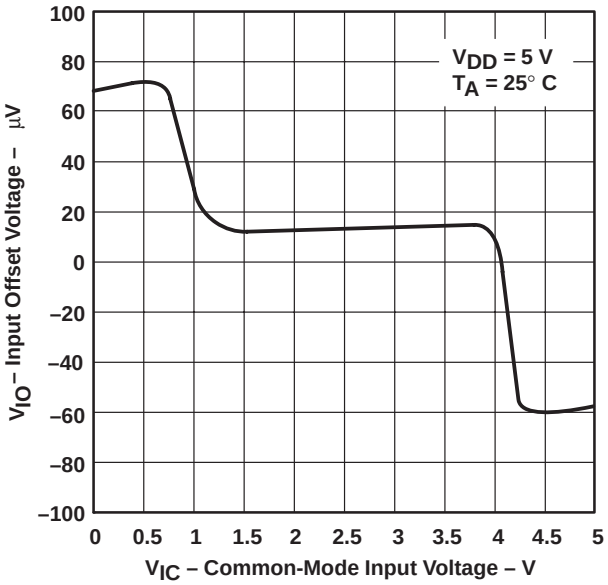


Figure 2

INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

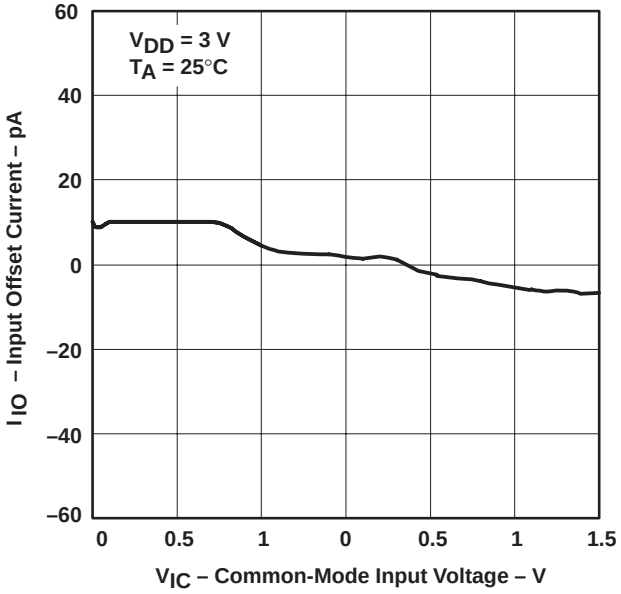


Figure 3

INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

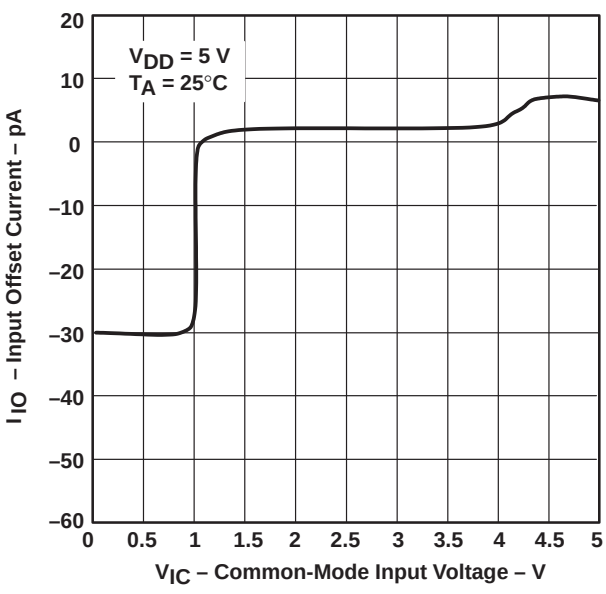


Figure 4

TYPICAL CHARACTERISTICS

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

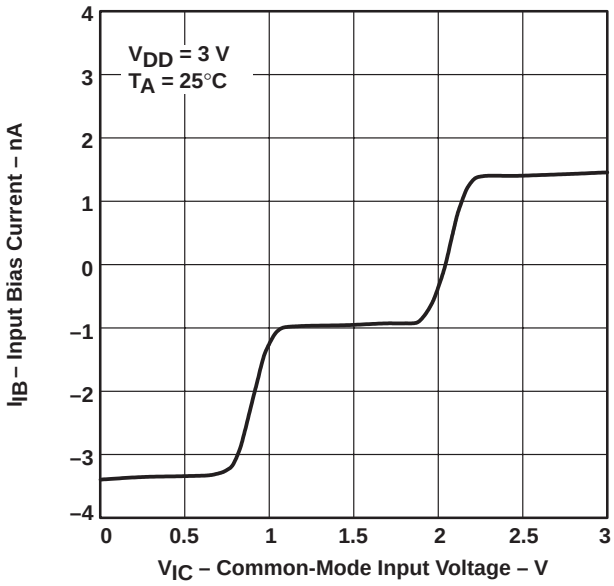


Figure 5

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

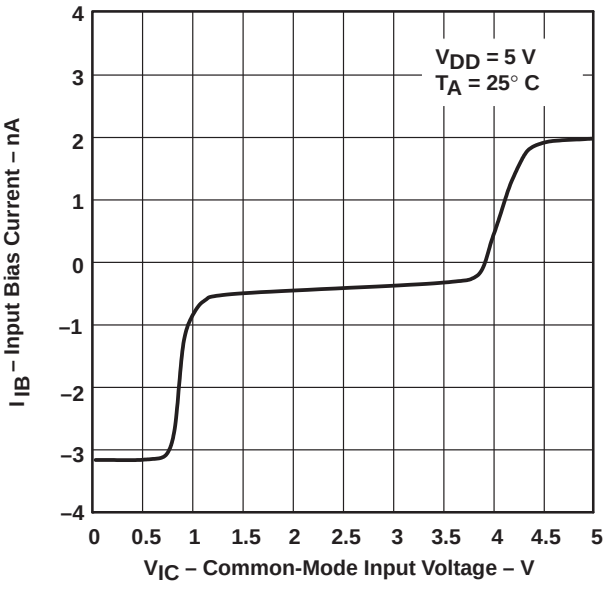


Figure 6

**INPUT OFFSET CURRENT
AND INPUT BIAS CURRENT
vs
FREE–AIR TEMPERATURE**

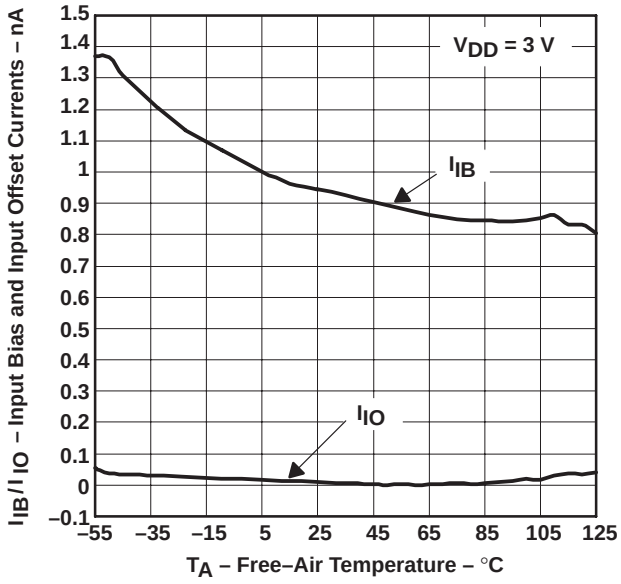


Figure 7

**INPUT OFFSET CURRENT
AND INPUT BIAS CURRENT
vs
FREE–AIR TEMPERATURE**

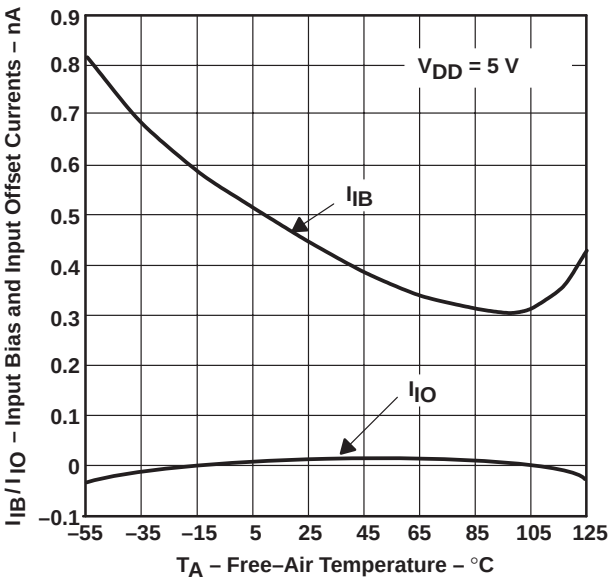


Figure 8

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY

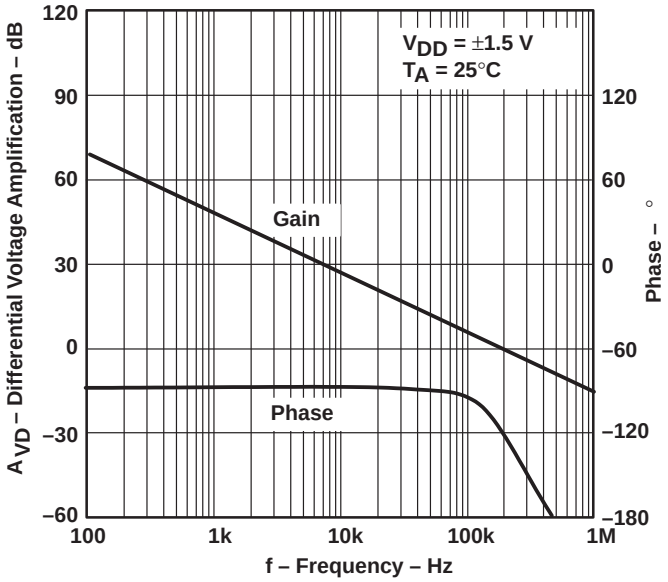


Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY

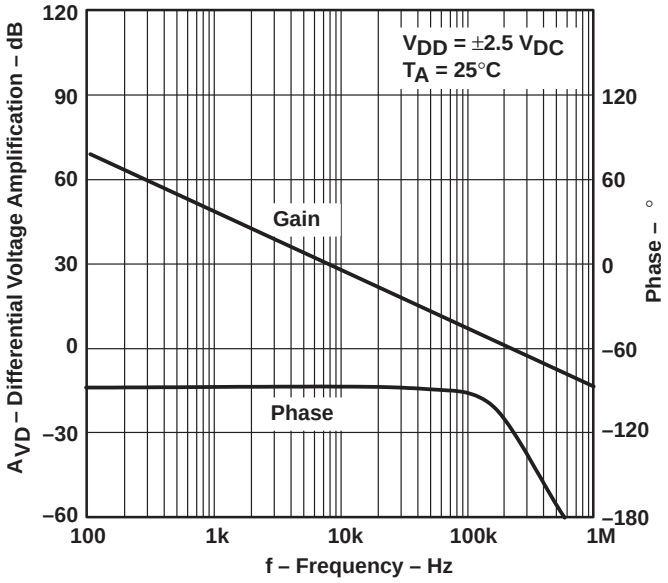


Figure 10

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

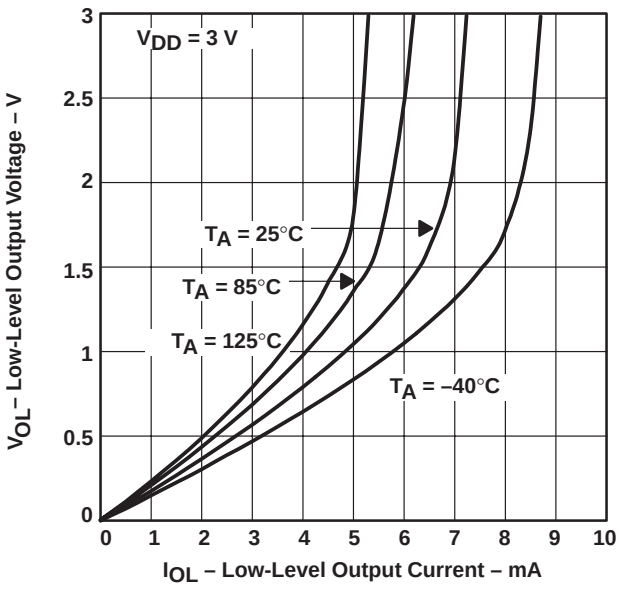


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

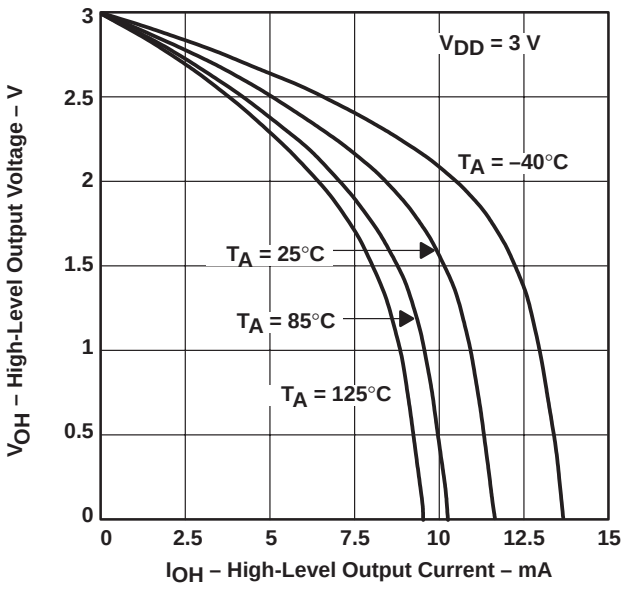


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

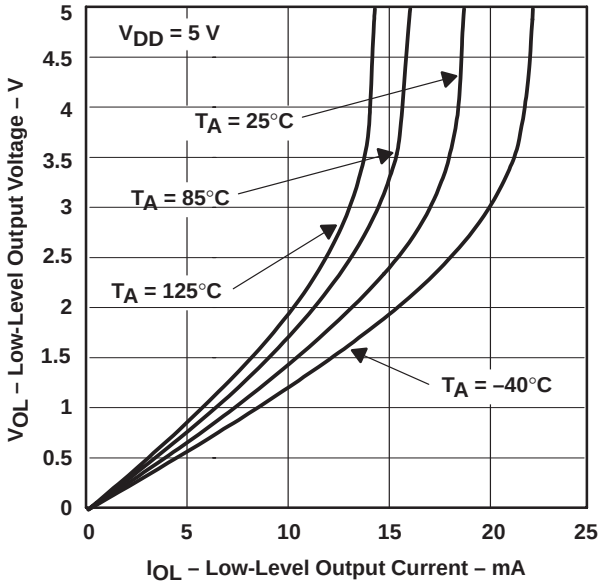


Figure 13

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

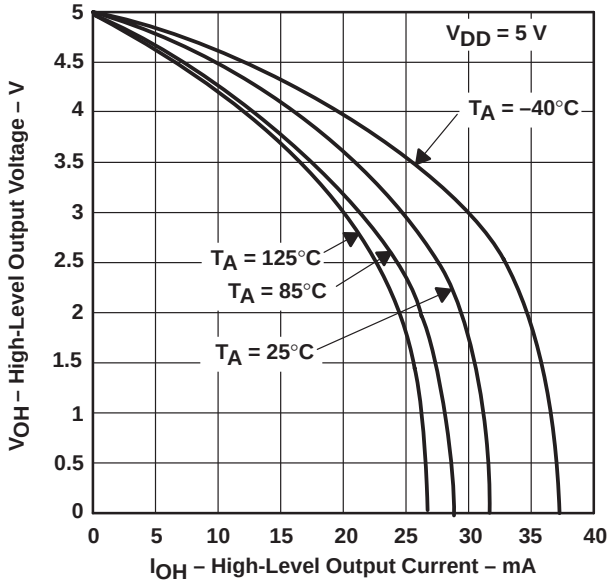


Figure 14

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

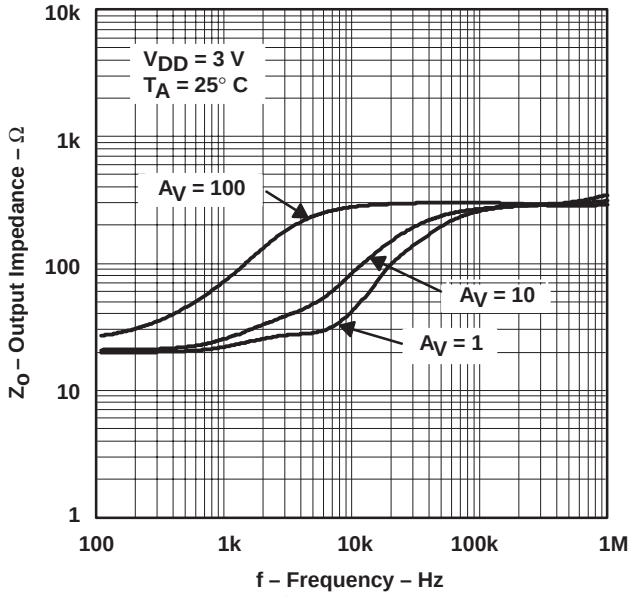


Figure 15

OUTPUT IMPEDANCE vs FREQUENCY

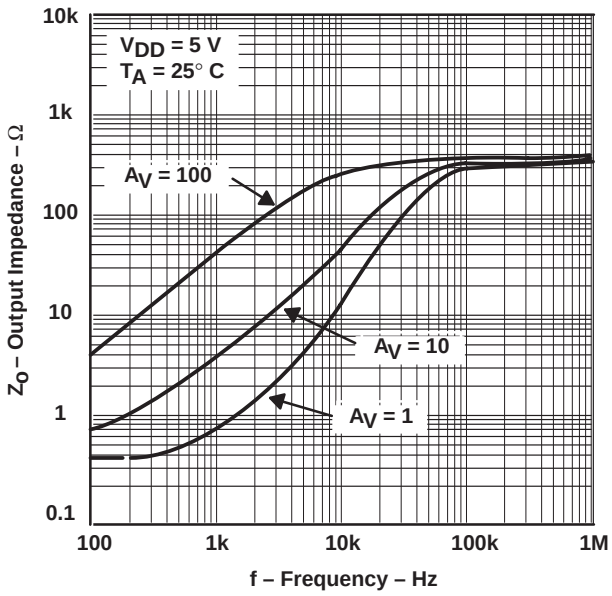


Figure 16

COMMON-MODE REJECTION RATIO vs FREQUENCY

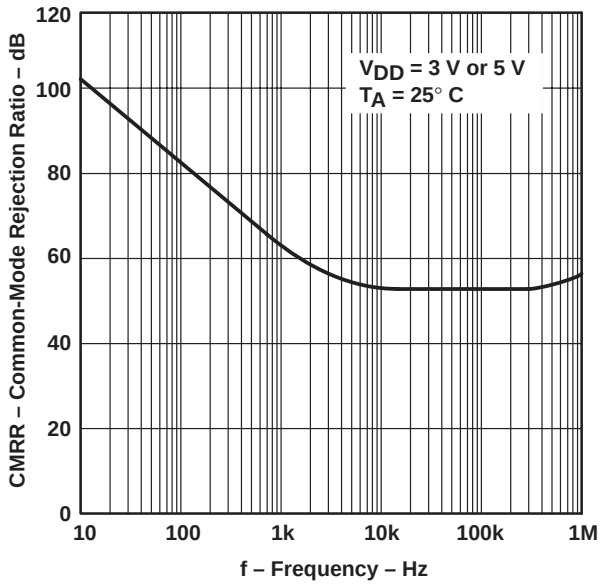


Figure 17

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO vs FREQUENCY

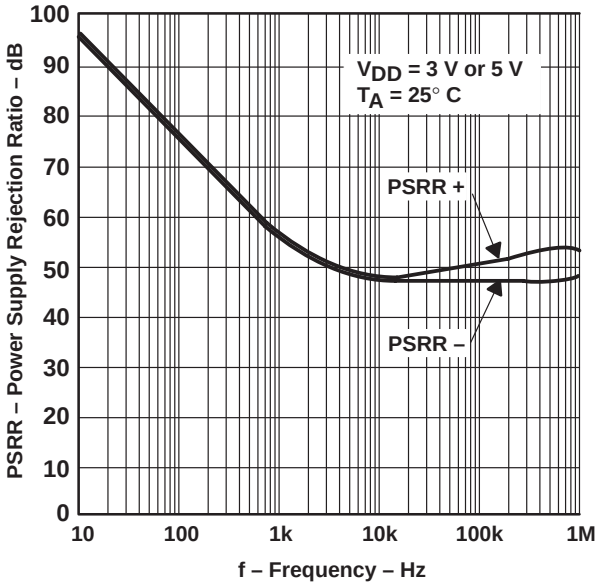


Figure 18

SUPPLY CURRENT vs SUPPLY VOLTAGE

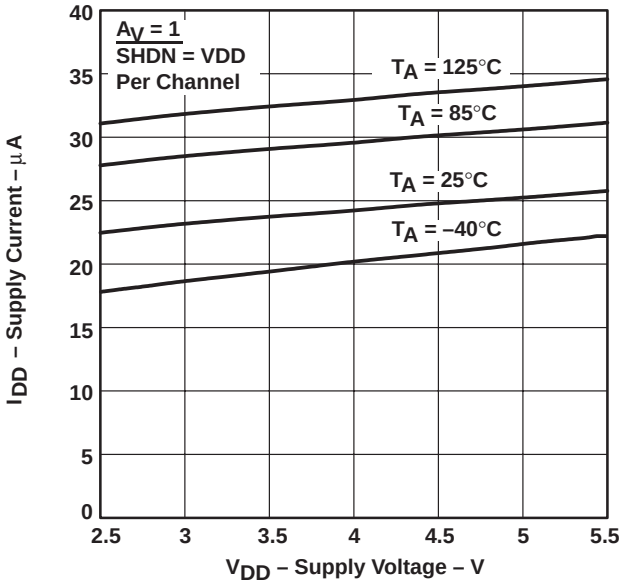


Figure 19

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

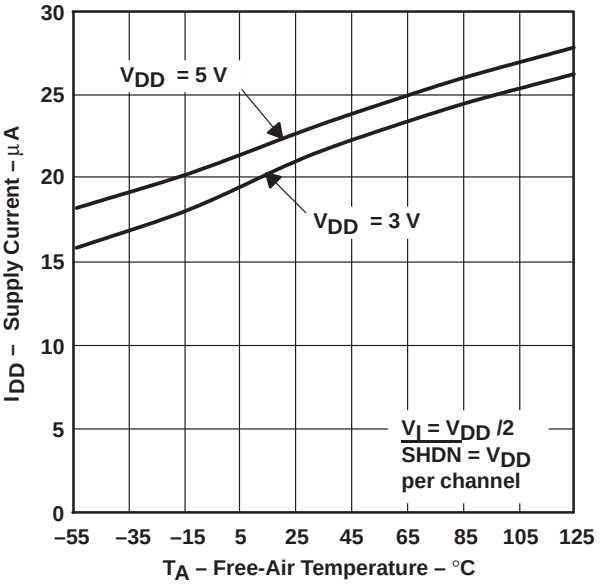


Figure 20

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

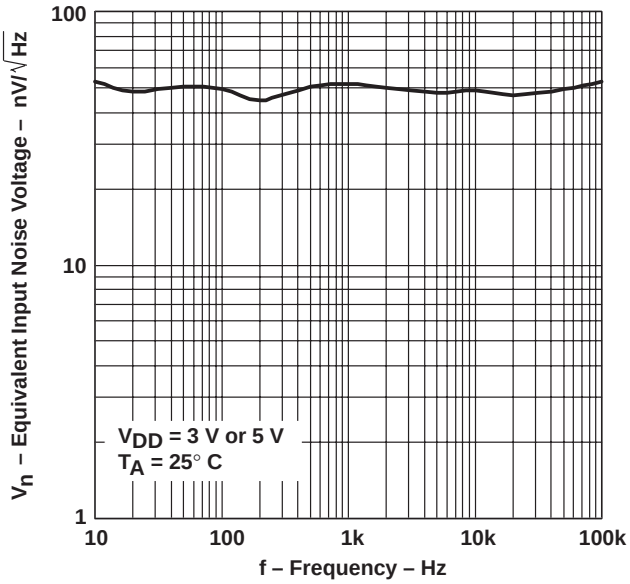


Figure 21

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

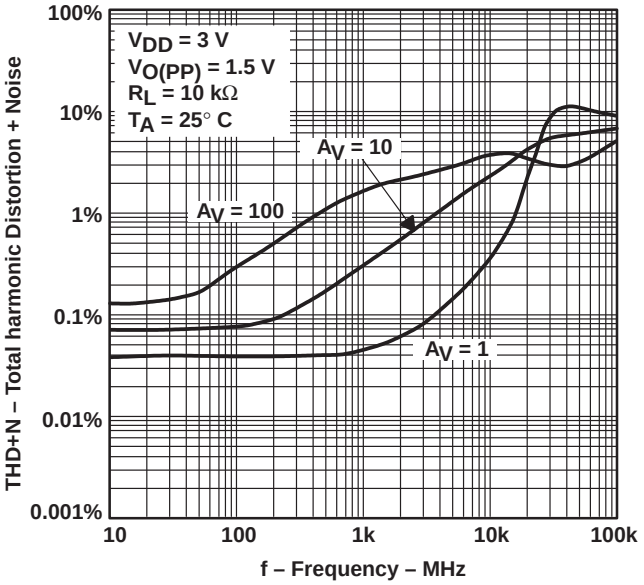


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

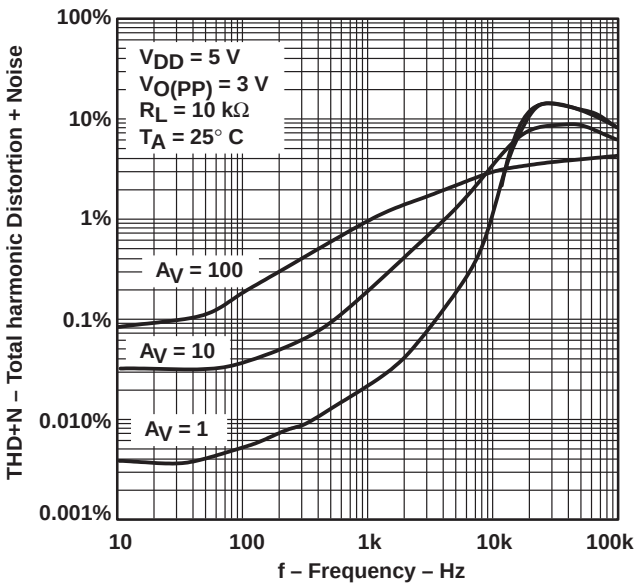


Figure 23

PHASE MARGIN vs LOAD CAPACITANCE

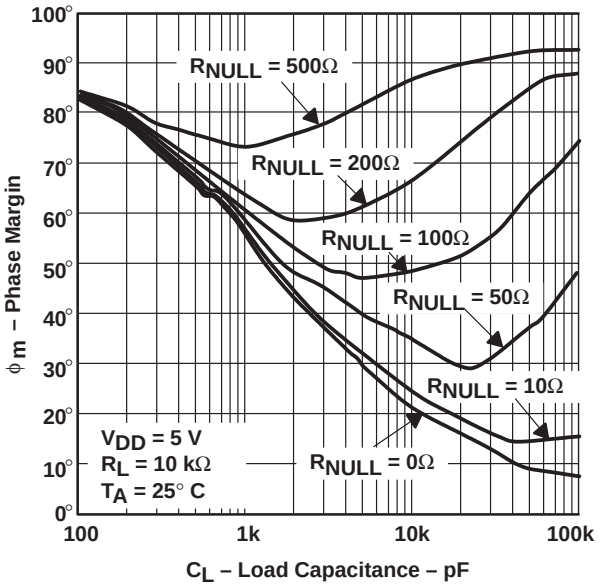


Figure 24

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

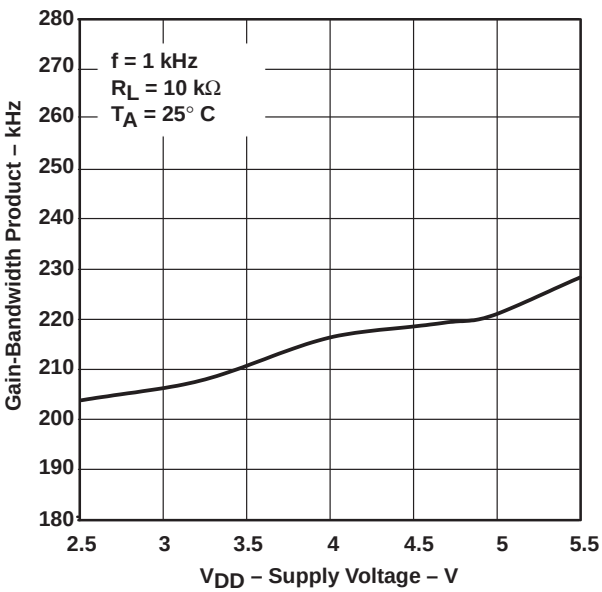


Figure 25

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

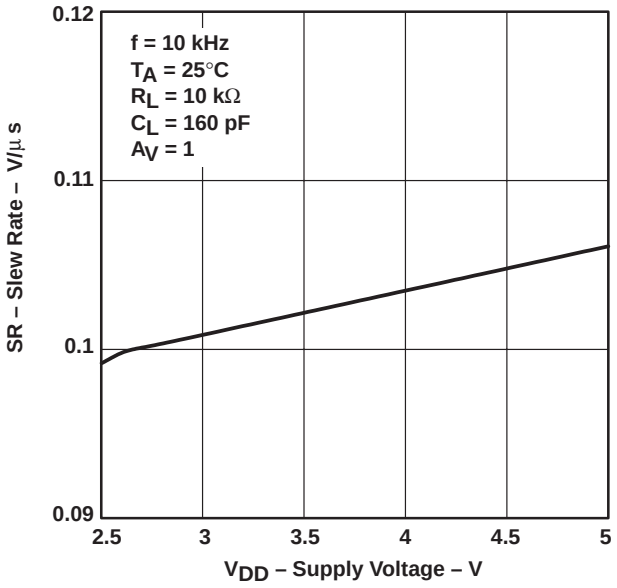


Figure 26

SLEW RATE vs FREE-AIR TEMPERATURE

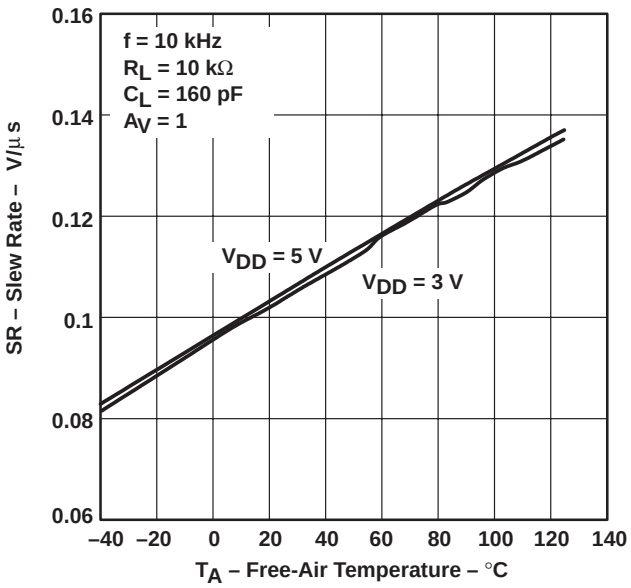


Figure 27

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

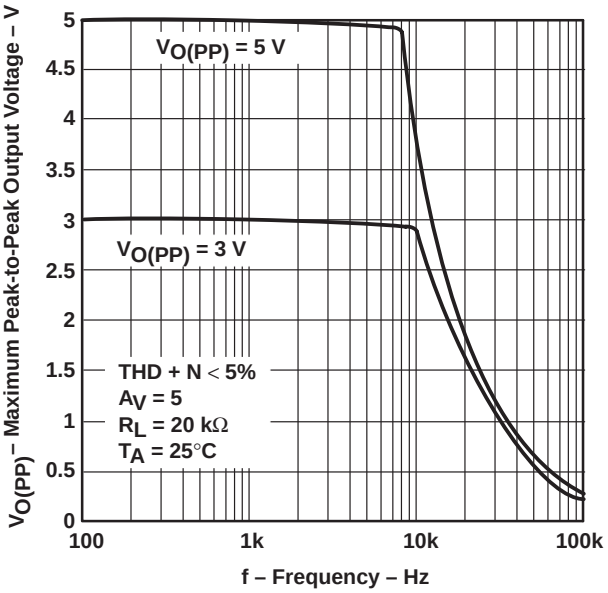


Figure 28

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

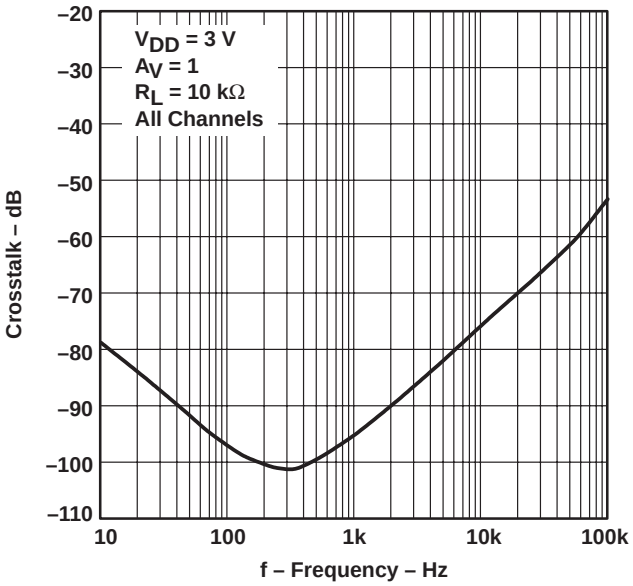


Figure 29

CROSSTALK vs FREQUENCY

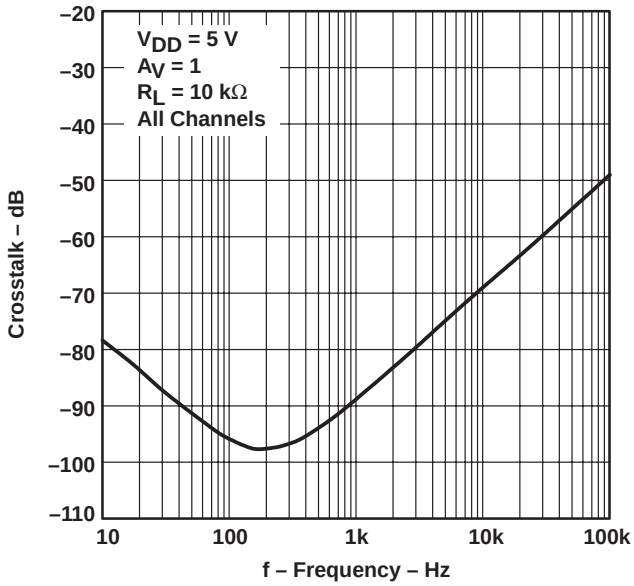


Figure 30

SMALL-SIGNAL FOLLOWER PULSE RESPONSE vs TIME

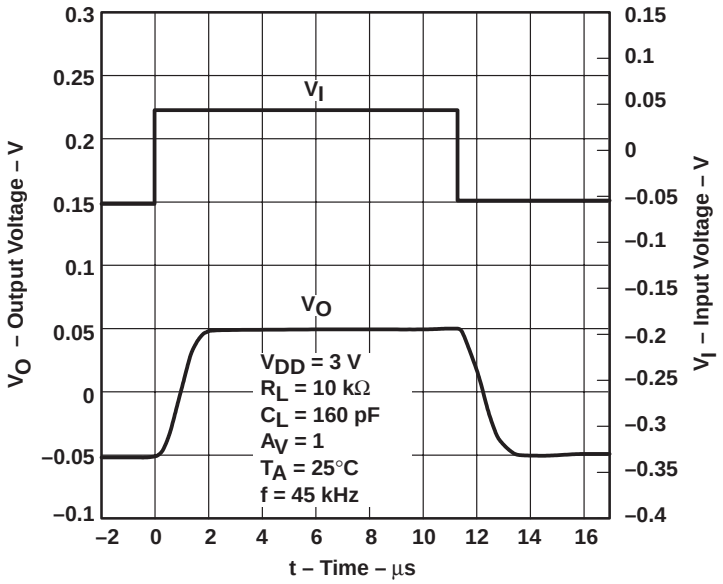


Figure 31

TYPICAL CHARACTERISTICS

LARGE-SIGNAL FOLLOWER PULSE RESPONSE vs TIME

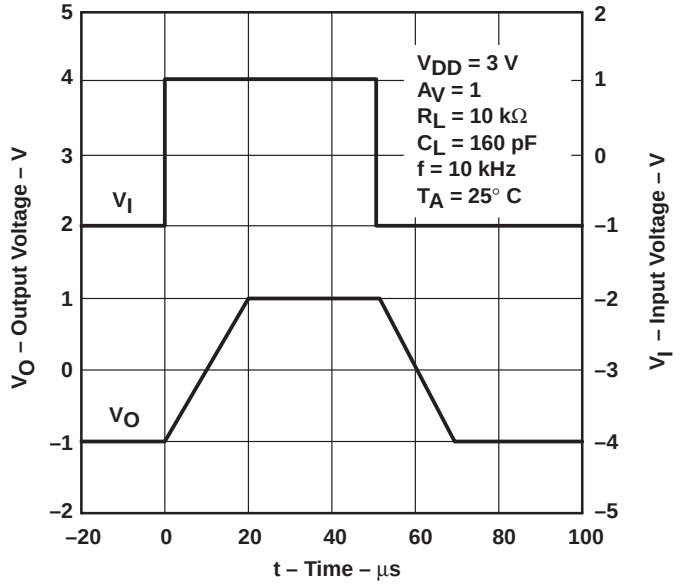


Figure 32

SMALL-SIGNAL FOLLOWER PULSE RESPONSE vs TIME

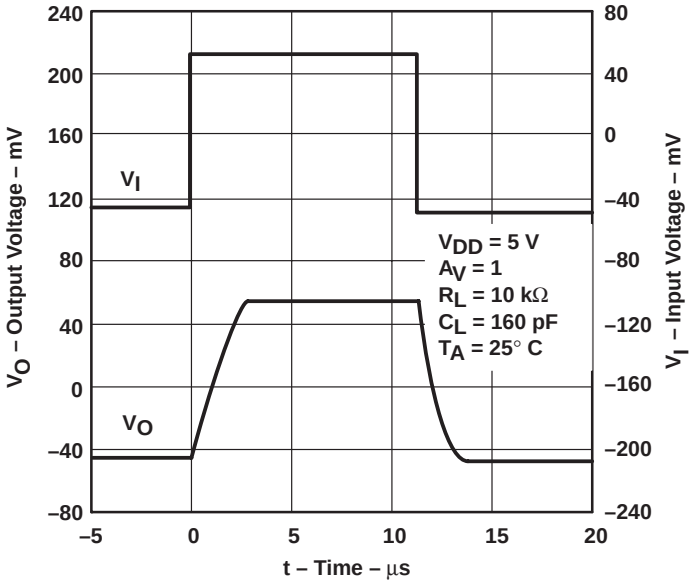


Figure 33

TYPICAL CHARACTERISTICS

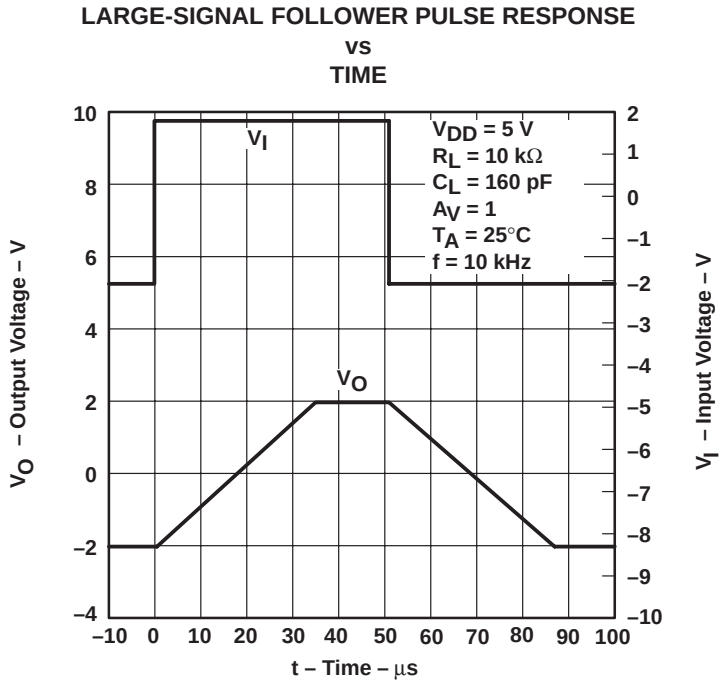


Figure 34

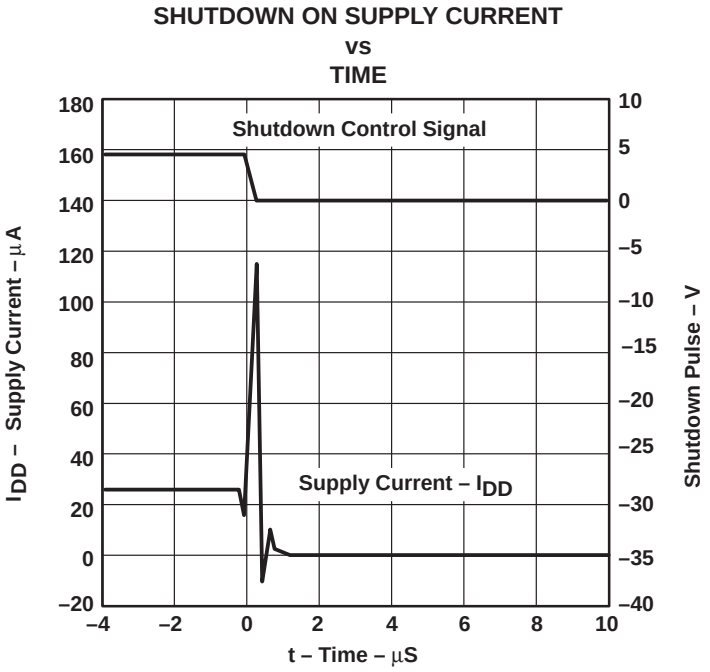


Figure 35

TYPICAL CHARACTERISTICS

SHUTDOWN OFF SUPPLY CURRENT vs TIME

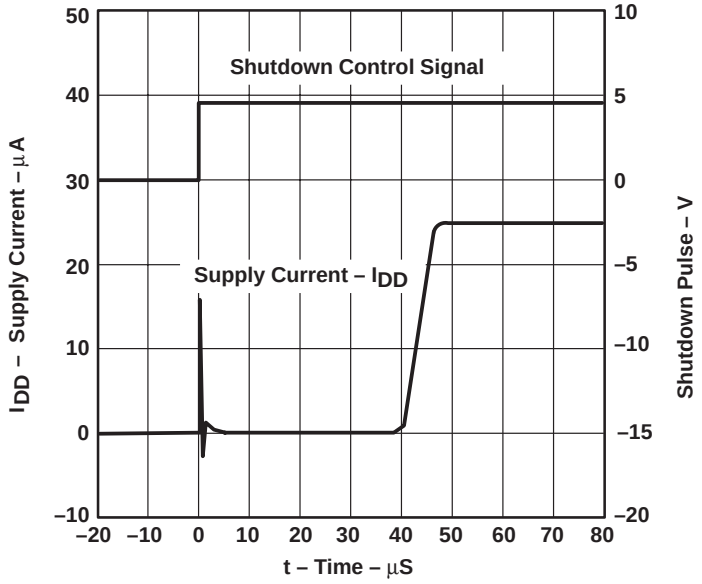


Figure 36

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

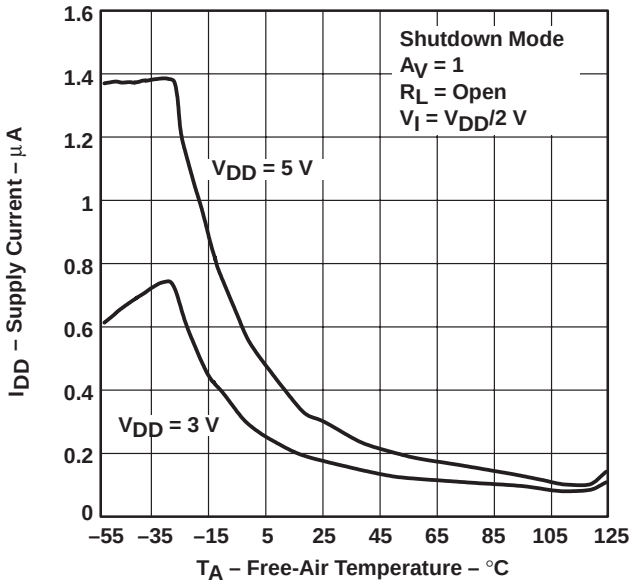


Figure 37

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE vs TIME

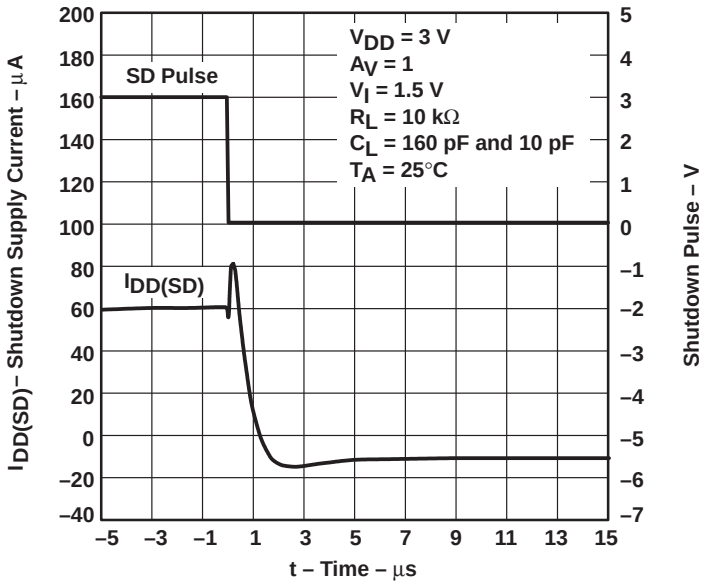


Figure 38

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE vs TIME

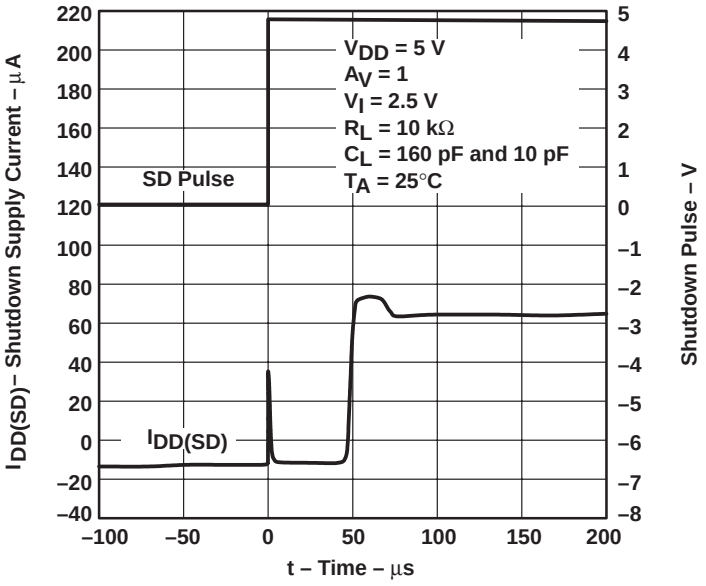


Figure 39

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE vs TIME

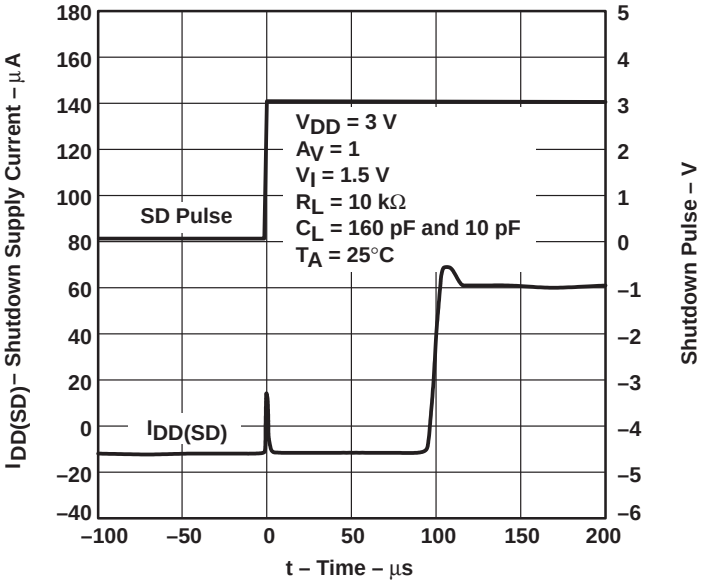


Figure 40

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE vs TIME

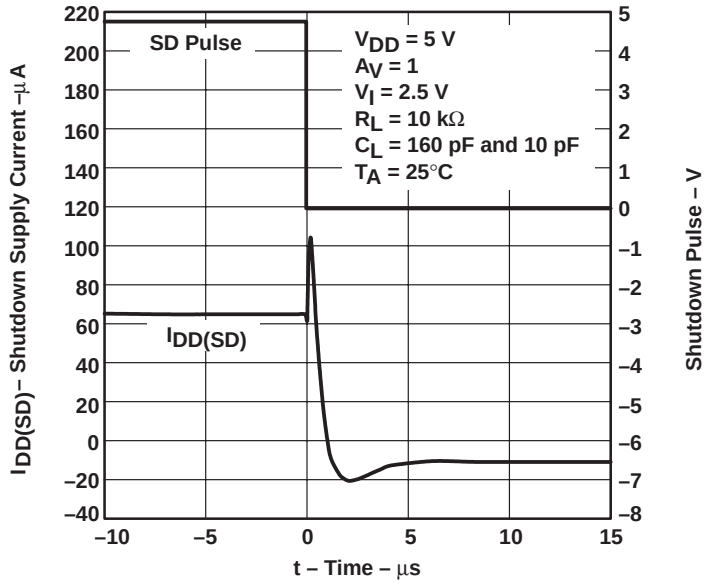


Figure 41

TYPICAL CHARACTERISTICS

SHUTDOWN OFF PULSE RESPONSE vs TIME

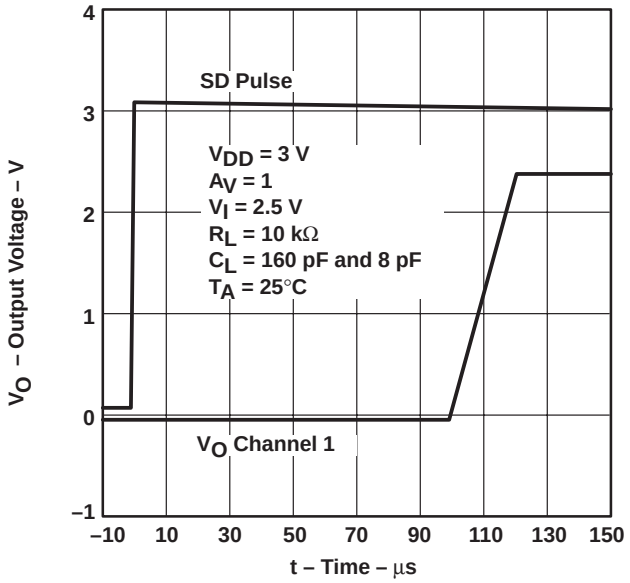


Figure 42

SHUTDOWN OFF PULSE RESPONSE vs TIME

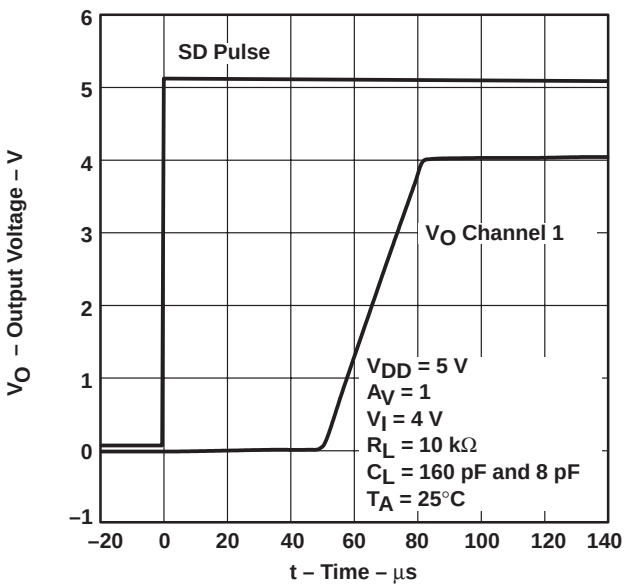


Figure 43

SHUTDOWN ON PULSE RESPONSE vs TIME

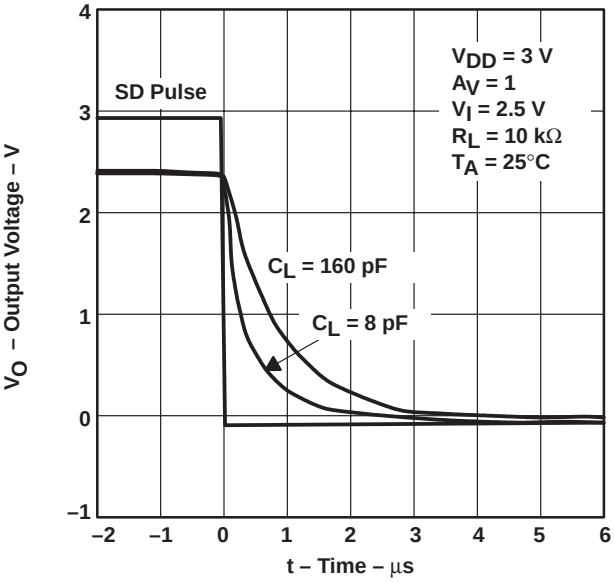


Figure 44

SHUTDOWN ON PULSE RESPONSE vs TIME

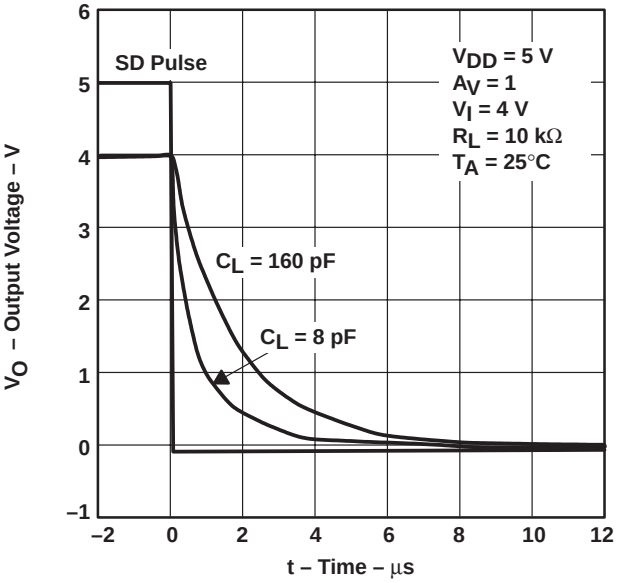


Figure 45

TYPICAL CHARACTERISTICS

SHUTDOWN REVERSE ISOLATION vs FREQUENCY

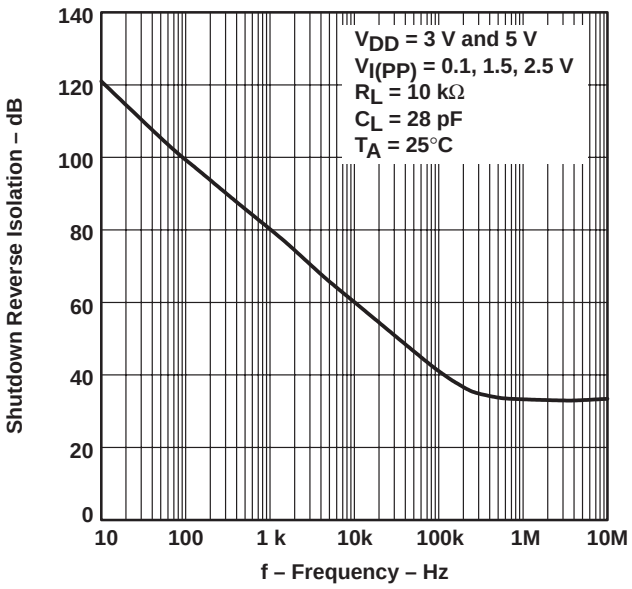


Figure 46

SHUTDOWN FORWARD ISOLATION vs FREQUENCY

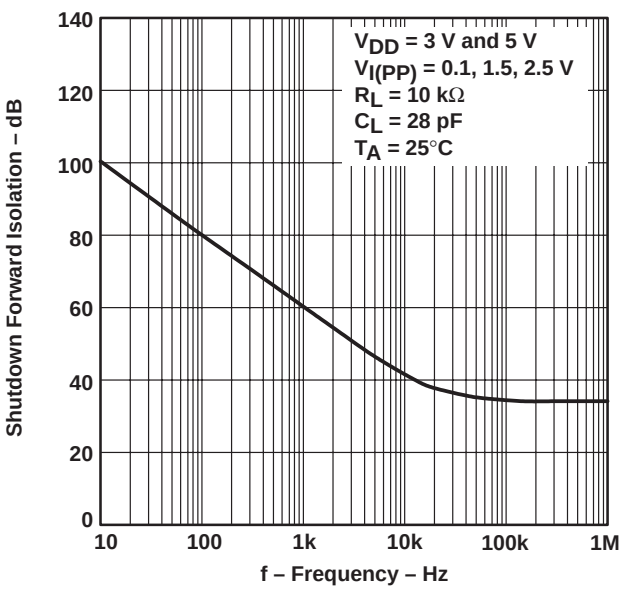


Figure 47

APPLICATION INFORMATION

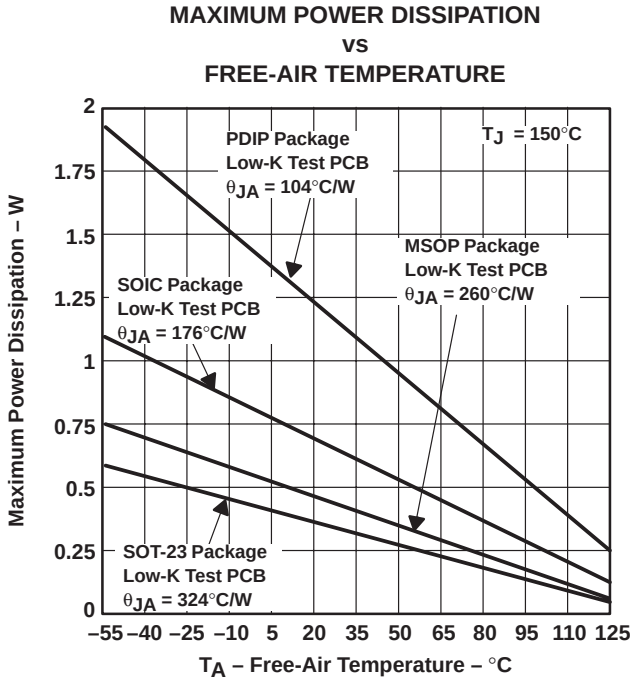
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 48 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV245x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 48. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

shutdown function

Three members of the TLV245x family (TLV2450/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 16 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}–$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 42, 43, 44, and 45. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 46 and 47 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35-V supplies and configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency using 0.1-V_{PP}, 1.5-V_{PP}, and 2.5-V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.5-V_{PP} input signal with a supply voltage of ±1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 49 are generated using the TLV245x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).

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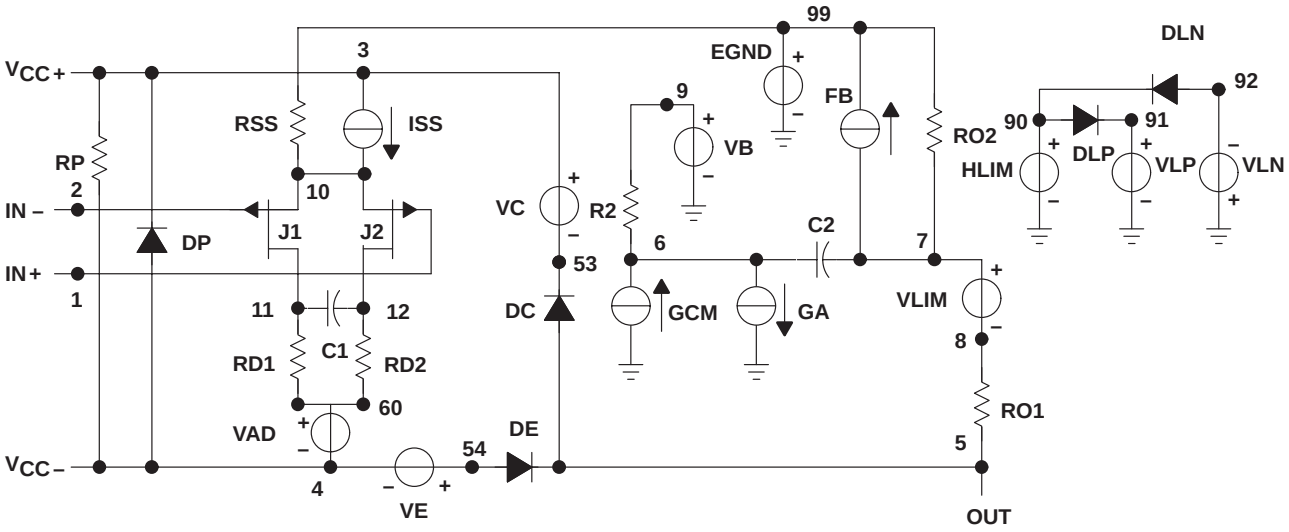
APPLICATION INFORMATION




```
* AMP_TLV2450–X operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 10/12/98 at 11:06
* Parts is a MicroSim product.
*
* connections:   non–inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt AMP_TLV2450–X 1 2 3 4 5
*
c1          11      12      354.48E–15
c2          6       7       7.5000E–12
cee         10      99      42.237E–15
dc          5       53      dy
de          54      5       dy
dlp         90      91      dx
dln         92      90      dx
dp          4       3       dx
egnd        99      0       poly(2) (3,0) (4,0) 0 .5 .5
fb          7       99      poly(5) vb vc ve vlp vln 0
+ 207.31E6 –1E3 1E3 210E6 –210E6
ga          6       0       11      12 15.254E–6
gcm         0       6       10      99 48.237E–12
iee         10      4       dc      938.61E–9
hlim        90      0       vlim 1K
q1          11      2       13 qx1
q2          12      1       14 qx2
r2          6       9       100.00E3
rc1         3       11      65.557E3
rc2         3       12      65.557E3
re1         13      10      10.367E3
re2         14      10      10.367E3
ree         10      99      213.08E6
ro1         8       5       10
ro2         7       99      10
rp          3       4       147.06
vb          9       0       dc 0
vc          3       53      dc .82
ve          54      4       dc .82
vlim        7       8       dc 0
vlp         91      0       dc 38
vln         0       92      dc 38
.model      dx      D(Is=800.00E–18)
.model      dy      D(Is=800.00E–18 Rs=1m Cjo=10p)
.model      qx1     NPN(Is=800.00E–18 Bf=843.08)
.model      qx2     NPN(Is=800.0000E–18 Bf=843.08)
.ends
```

```
* Schematics Subcircuit *
.subckt TLV2450_ver1 Vout Vdd GND V+ V– SD
*
S_S2        $N_0001 GND SD GND S2
RS_S2       SD GND 1G
.MODEL S2 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
+  Von=1.0
S_S1        $N_0002 VDD SD GND S1
RS_S1       SD GND 1G
.MODEL S1 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
+  Von=1.0
S_S3        Vout $N_0003 SD GND S3
RS_S3       SD GND 1G
.MODEL S3 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
+  Von=1.0
X_SUB_U1        V+ V– $N_0002 $N_003
+ AMP_TLV2450–X
.ENDS       tlv2450_ver1
```

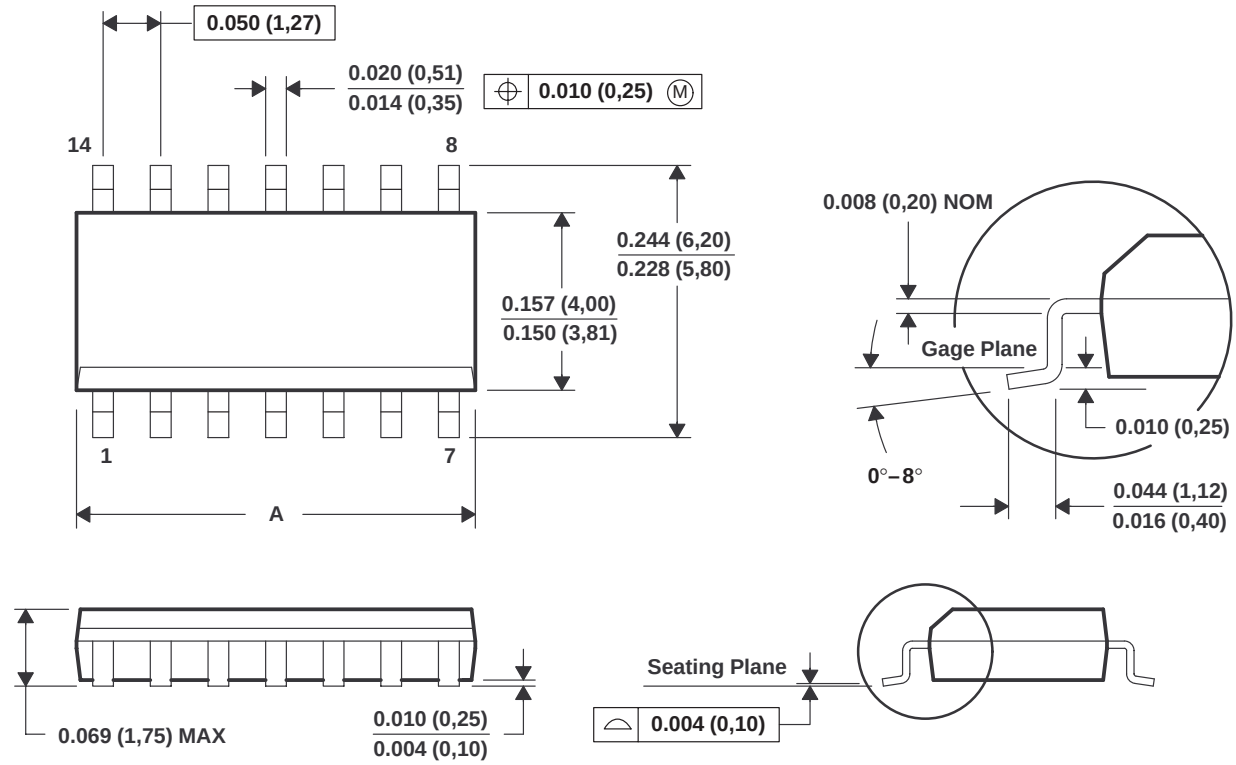
```
* Schematics Subcircuit *
.subckt TLV2451_ver1 V+ V– Vout Vdd GND
*
X_SUB_U1        V+ V– GND Vout AMP_TLV2450–X
.ENDS       tlv2451_ver1
```

Figure 49. Boyle Macromodel and Subcircuit

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



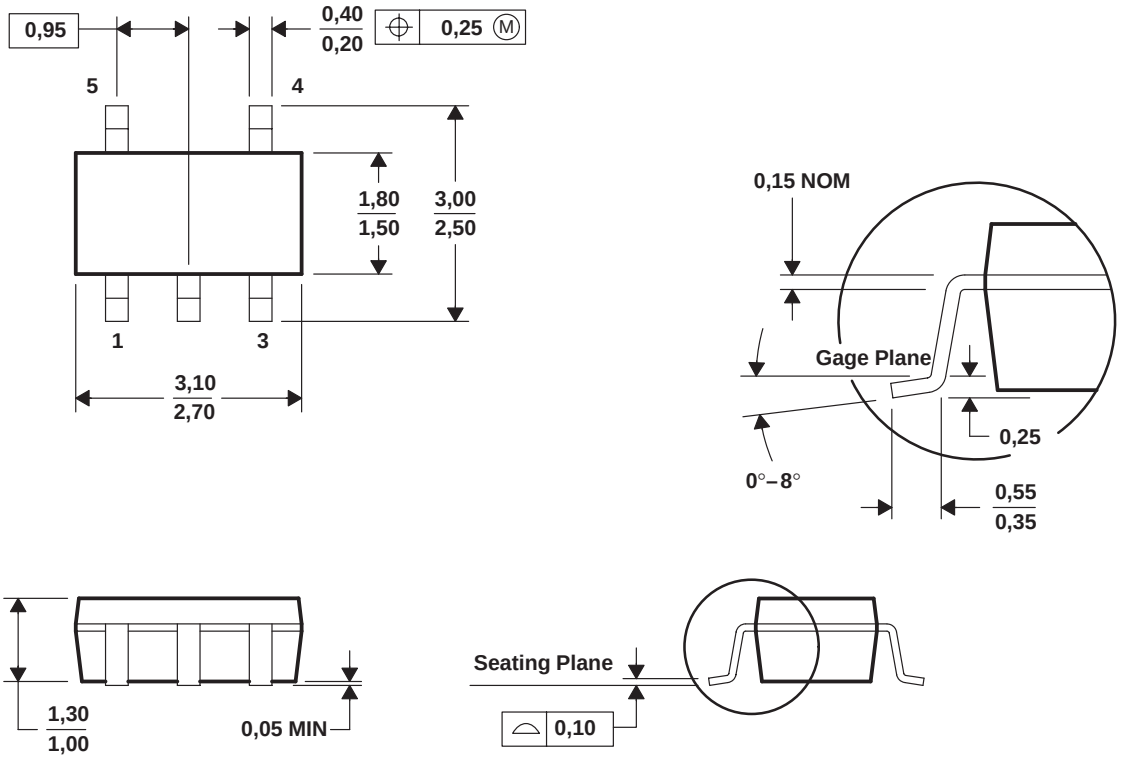
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: B. All linear dimensions are in inches (millimeters).
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
E. Falls within JEDEC MS-012

MECHANICAL INFORMATION

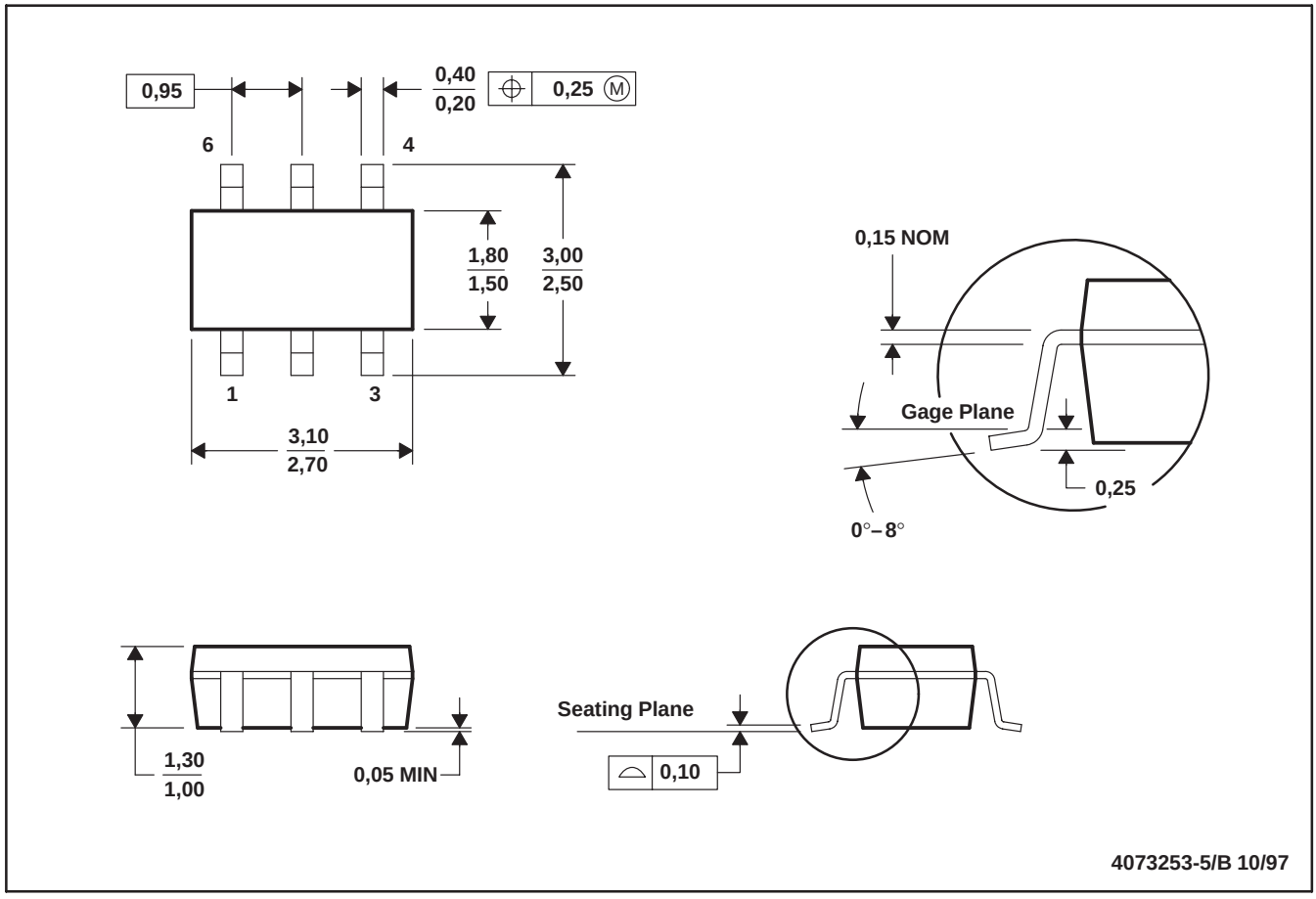
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

MECHANICAL INFORMATION

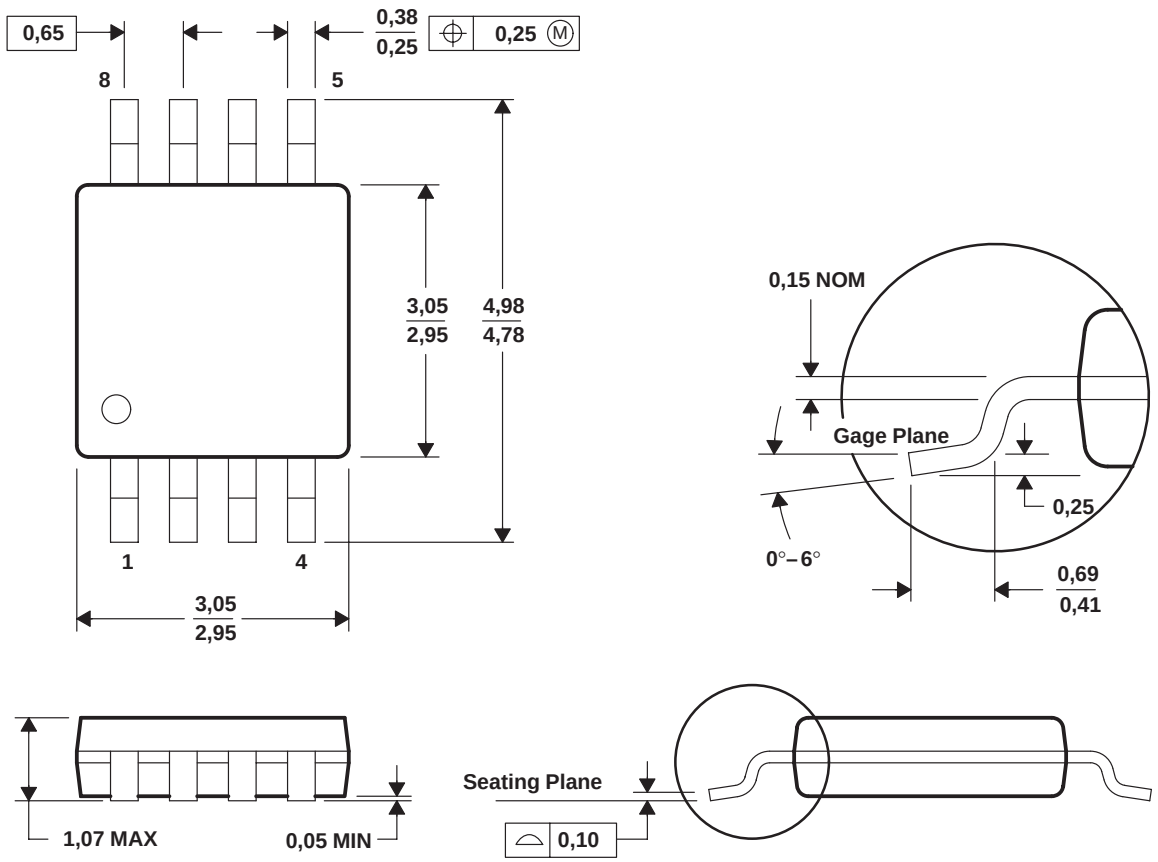
DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

MECHANICAL INFORMATION

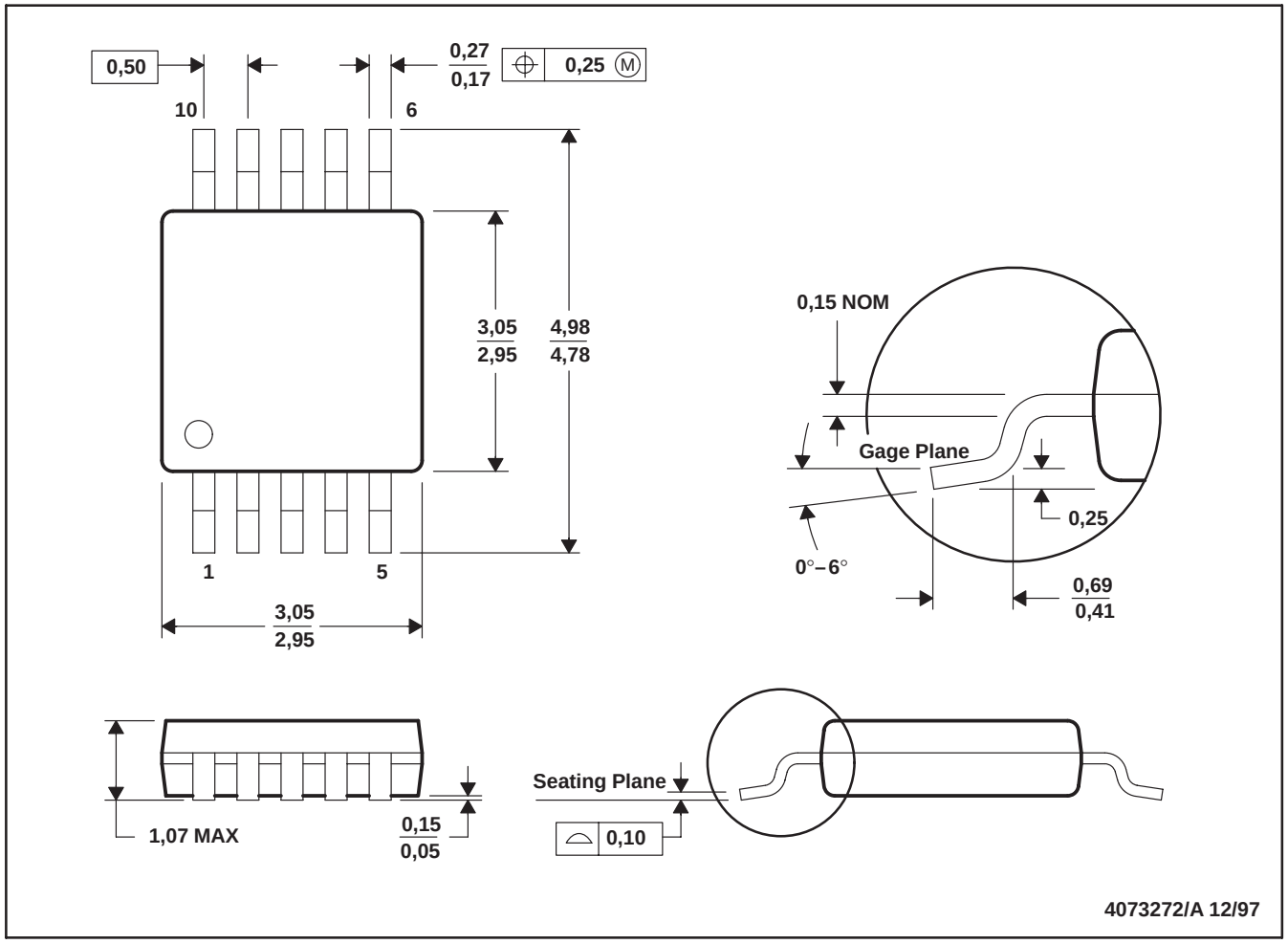
DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



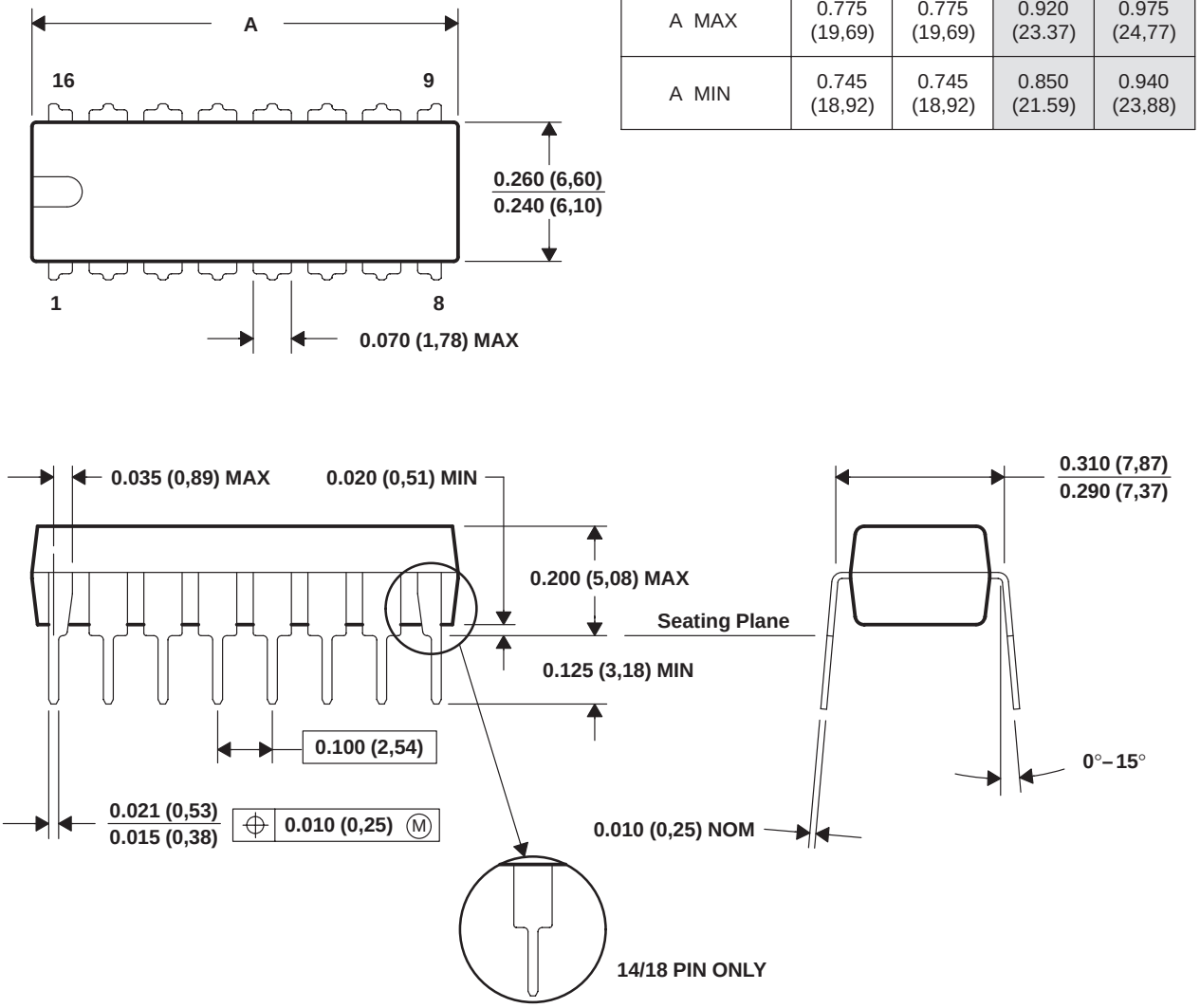
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

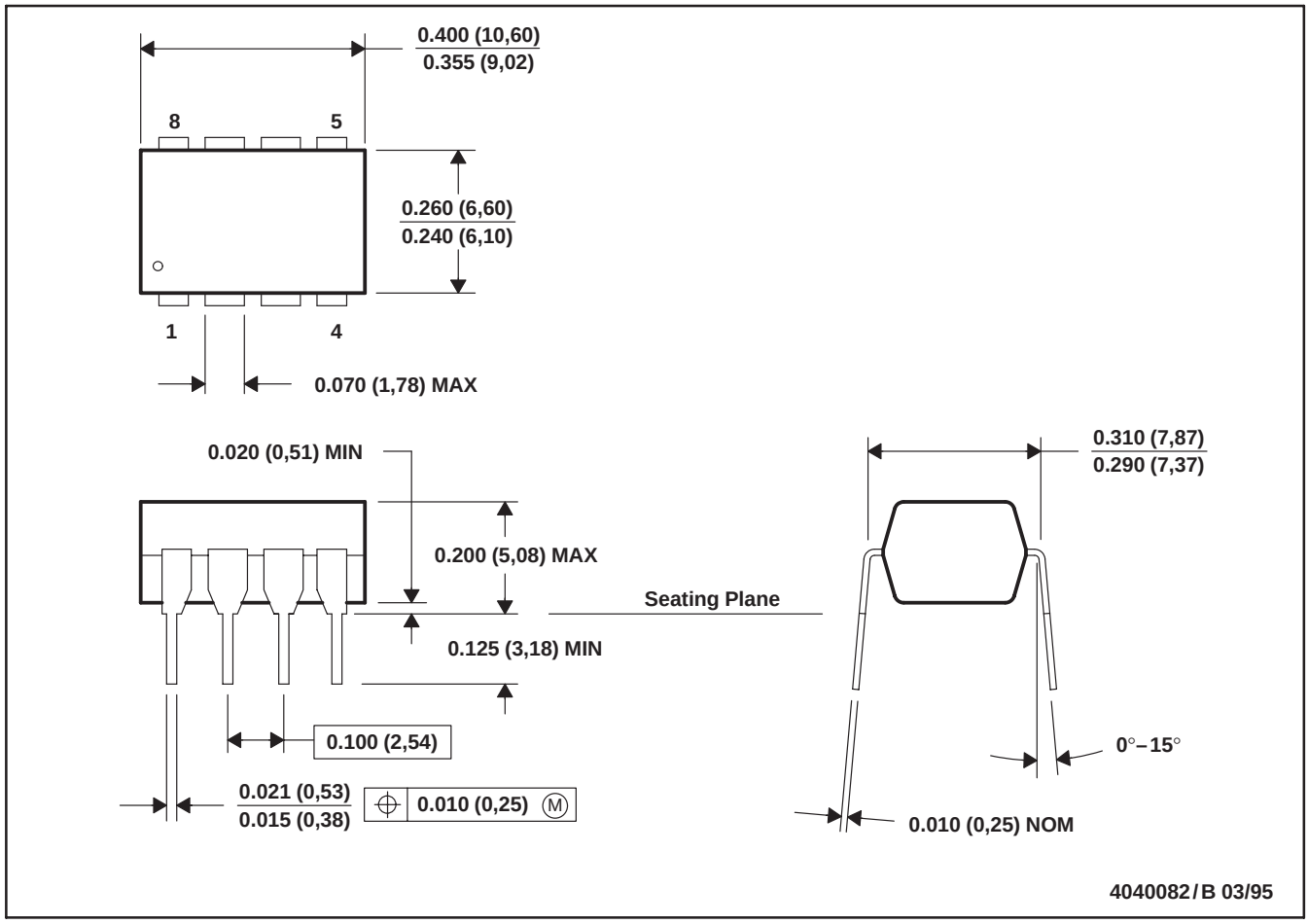
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

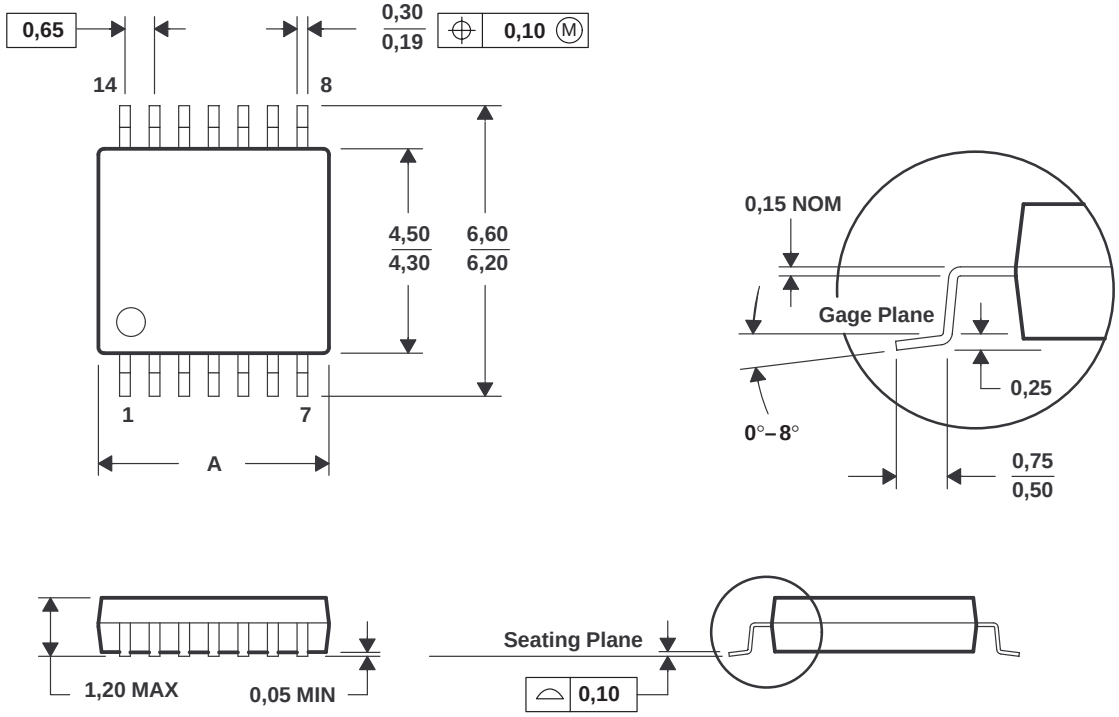


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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