

SN74CBT16292

12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS053C – MARCH 1998 – REVISED FEBRUARY 1999

- 4-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

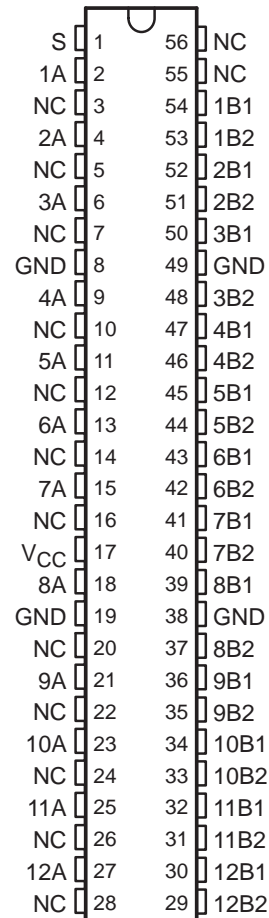
description

The SN74CBT16292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/ demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1 and R_{INT} is connected to port B2. When S is high, port A is connected to port B2 and R_{INT} is connected to port B1.

The SN74CBT16292 is characterized for operation from -40°C to 85°C .

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = V_{CC}$ or GND			±5	μA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			3	μA
ΔI_{CC}^\ddagger	Control input	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control input	$V_I = 3\text{ V}$ or 0			3		pF
C_{io}		$V_{CC} = 0$,	$V_O = 3\text{ V}$ or 0		8		pF
r_{on}^\S		$V_{CC} = 4\text{ V}$, TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$		10	20	Ω
			$I_I = 64\text{ mA}$		3	7	
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$		3	7	
			$I_I = 30\text{ mA}$		3	7	
		$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$		5	15	

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^{\parallel}	A or B	B or A	0.5		0.25		ns
t_{en}	S	A or B	6.8		1	6	ns
t_{dis}	S	A or B	7		1	6.3	ns

\parallel The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
$t_{mbb}^\#$	Make-before-break time	0	2	0	2	ns

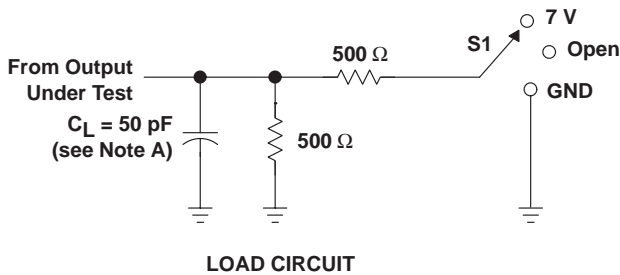
$\#$ The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



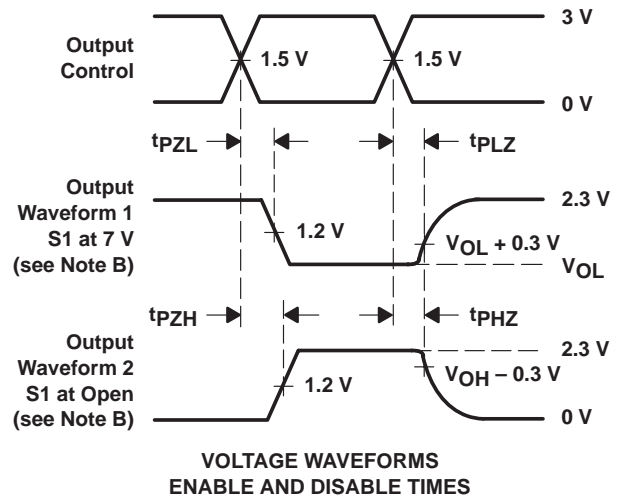
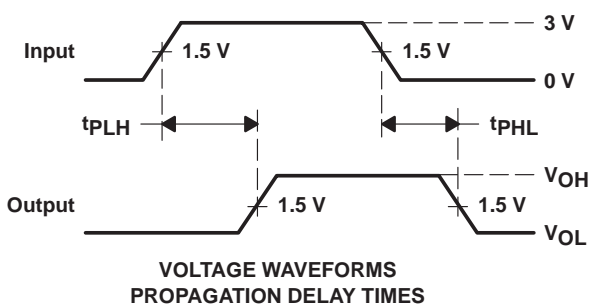
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PZL}/t_{PLZ}	7 V
t_{PZH}/t_{PHZ}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500- Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500- Ω pulldown resistor.
 C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} . $Z = R_{INT} = 500 \Omega$
 F. t_{PZL} and t_{PZH} are the same as t_{en} . $Z = R_{INT} = 500 \Omega$
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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