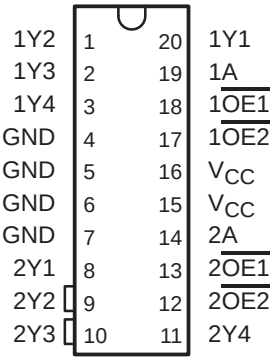
- **Low-Skew Propagation Delay Specifications for Clock-Driver Applications**
- **TTL-Compatible Inputs and CMOS-Compatible Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline (DW)**

DW PACKAGE
(TOP VIEW)



description

The CDC208 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

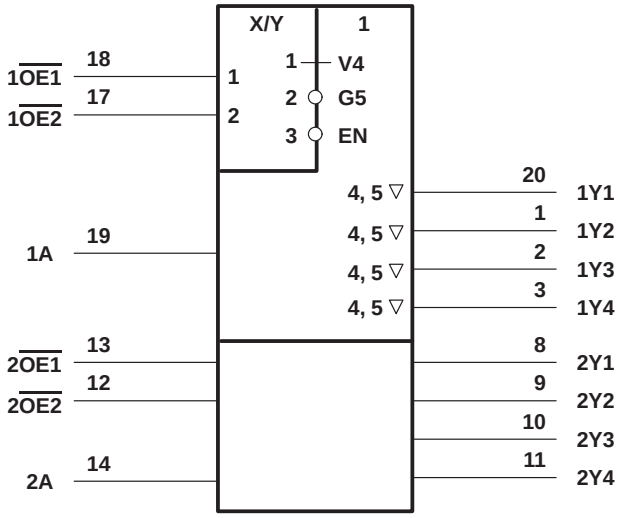
The CDC208 is characterized for operation from –40°C to 85°C.

FUNCTION TABLES

INPUTS			OUTPUTS			
$1\overline{OE1}$	$1\overline{OE2}$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

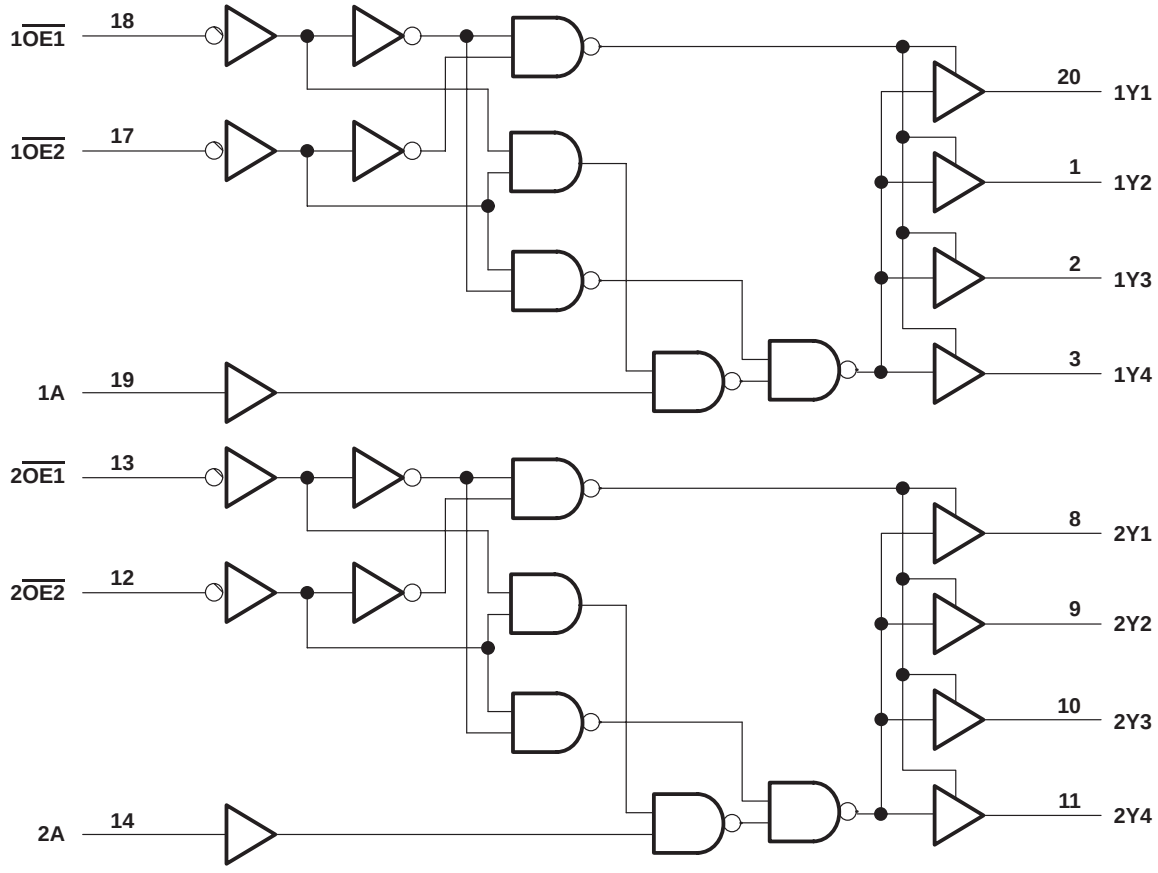
INPUTS			OUTPUTS			
$2\overline{OE1}$	$2\overline{OE2}$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.6 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
f_{clock}	Input clock frequency			60	MHz
T_A	Operating free-air temperature	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = –24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF
C_o	$V_O = V_{CC}$ or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	1A and 2A	Any Y	5.3	8.5	10.9	5.3	11.7	ns
t_{PHL}			3.6	7.7	11	3.6	11.5	
t_{PLH}	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	4.7	8.5	11.7	4.7	12.8	ns
t_{PHL}			4.4	8.4	11.3	4.4	12.4	
t_{PZH}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	4.4	8.1	11.3	4.4	12.4	ns
t_{PZL}	$1\overline{OE1}$ or $2\overline{OE1}$		5	9.6	13.3	5	14.9	
t_{PHZ}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	4.2	7.4	9.3	4.2	10.2	ns
t_{PLZ}	$1\overline{OE1}$ or $2\overline{OE1}$		5.4	7.5	9.2	5.4	9.9	

switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Note 3 and Figures 1 and 2)

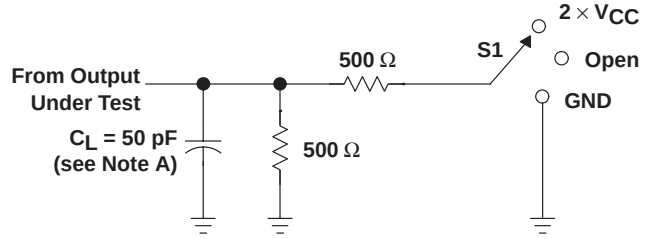
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	1A and 2A	Any Y	6.6	10.2	ns
t_{PHL}			6.6	9.8	
$t_{sk(o)}$	1A and 2A	Any Y		1	ns

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

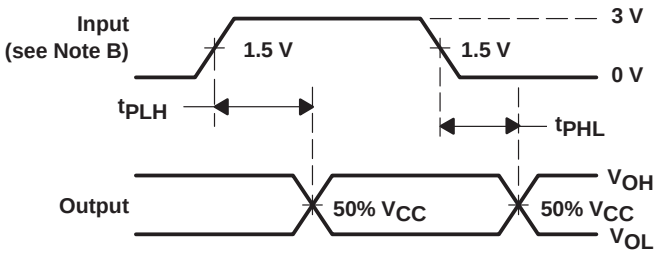
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	C_L = 50 pF, f = 1 MHz	96	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

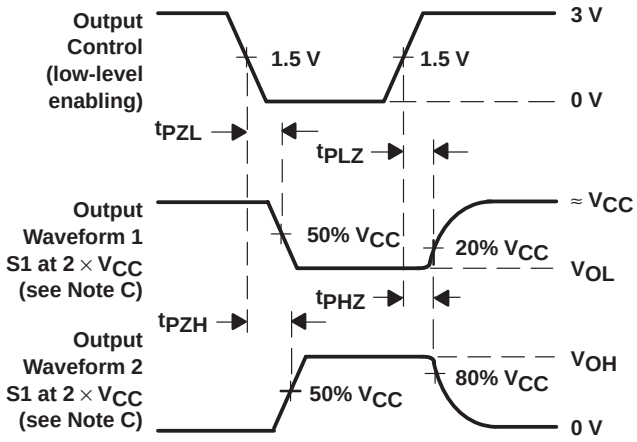


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

(see Note A) LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

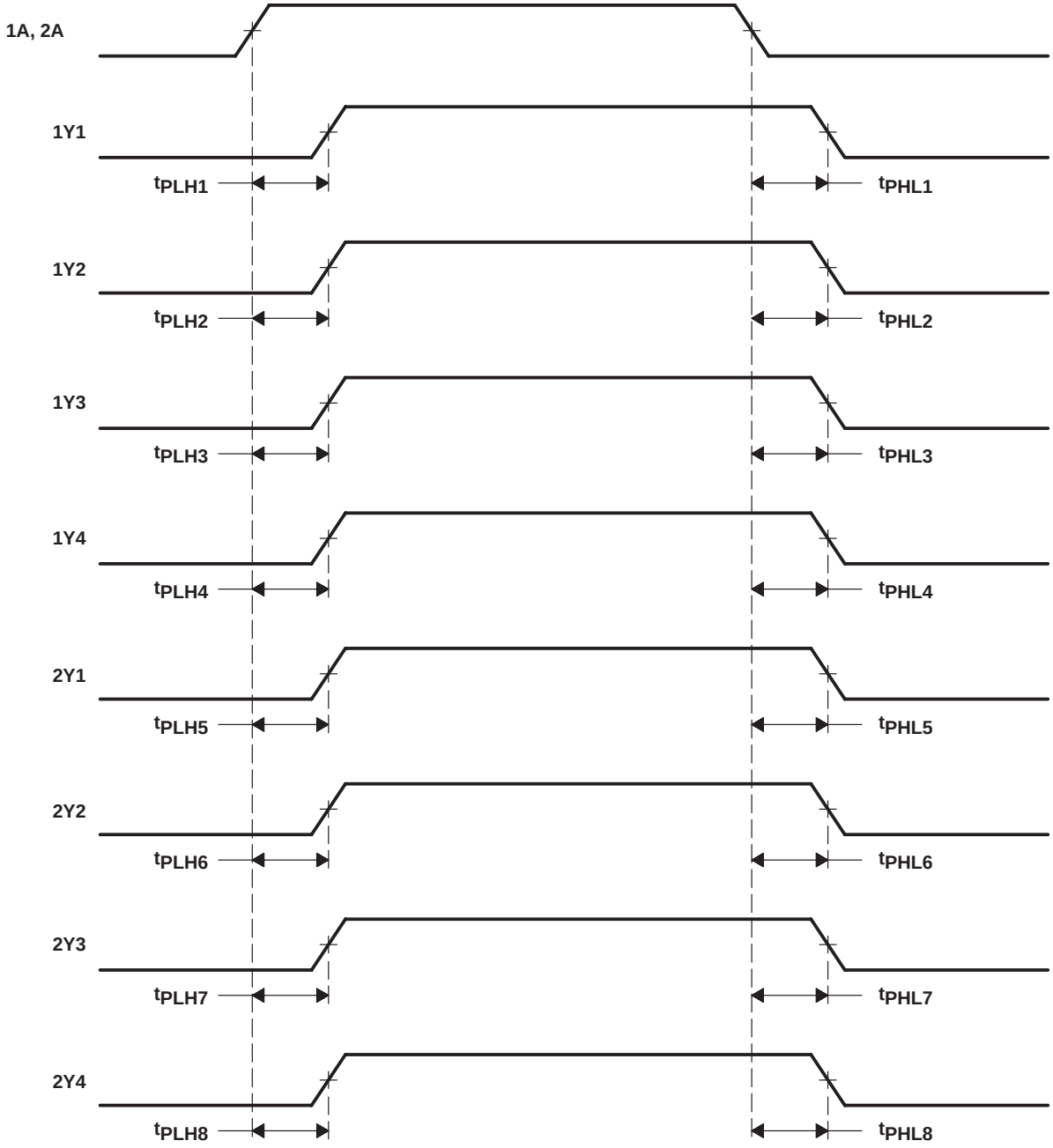


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: t_r = t_f = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



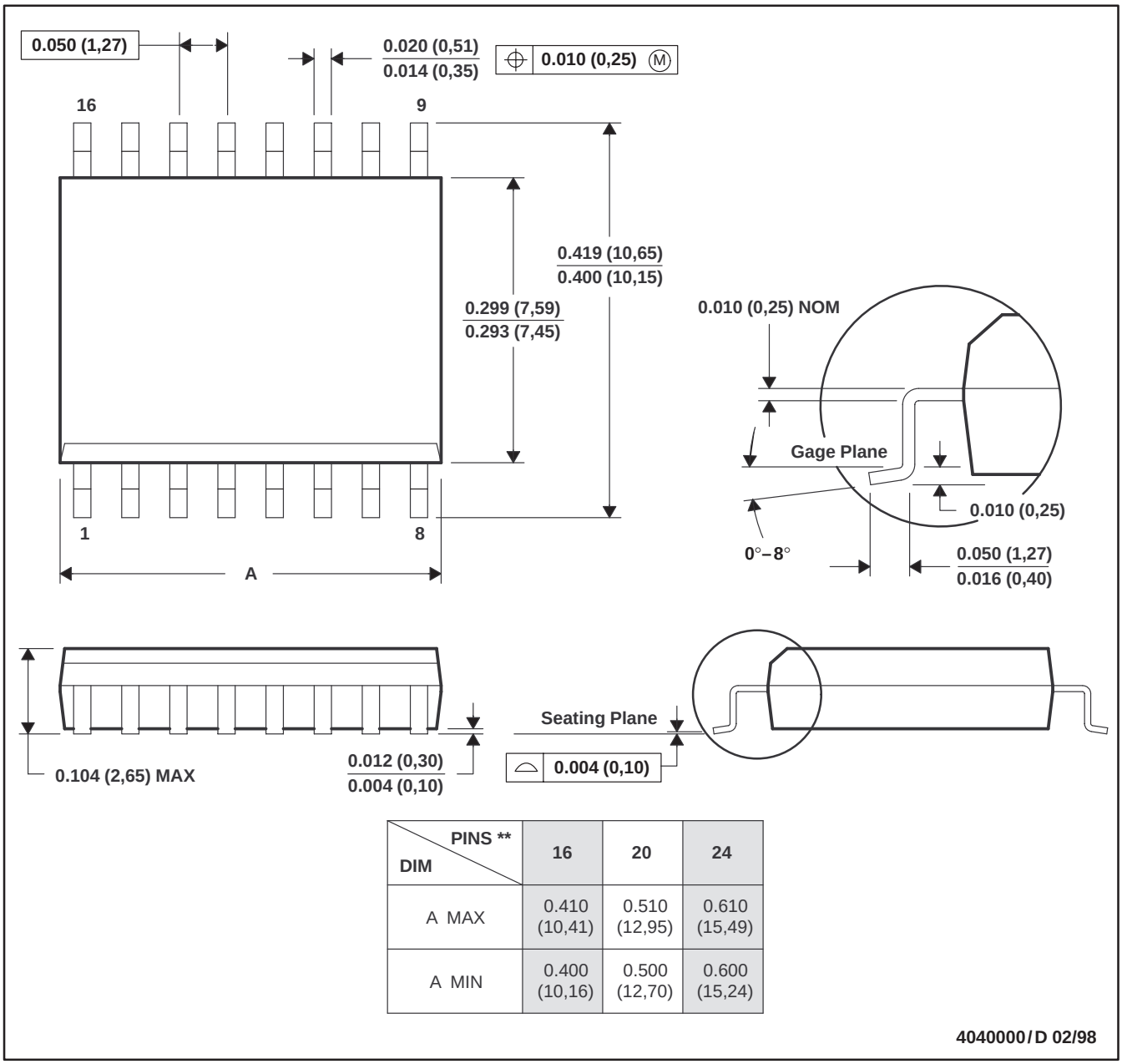
NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

MECHANICAL INFORMATION

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)

4040000/D 02/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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