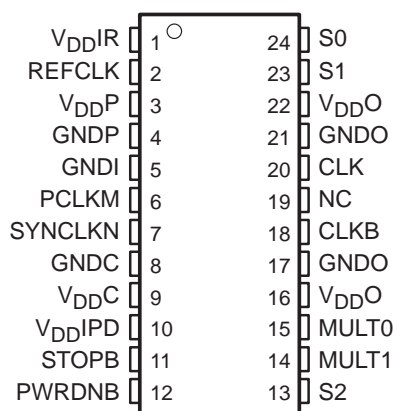


CDCR81 DIRECT RAMBUS™ CLOCK GENERATOR

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- **300-MHz Differential Clock Source for Direct RAMBUS Memory Systems for an 600-MHz Data Transfer Rate**
- **Synchronizes the Clock Domains of the Rambus Channel With an External System or Processor Clock**
- **Three Power Operating Modes to Minimize Power for Mobile and Other Power-Sensitive Applications**
- **Operates From a Single 3.3-V Supply and 120-mW at 300 MHz (Typ)**
- **Packaged in a Shrink Small-Outline Package (DBQ)**
- **Wide Phase-Lock Input Frequency Range 33 MHz to 100 MHz**
- **No External Components Required for PLL**
- **Supports Independent Channel Clocking**
- **Spread Spectrum Clocking Tracking Capability to Reduce EMI**
- **Designed For Use With TI's 133-MHz Clock Synthesizers CDC925, CDC924, CDC922 and CDC921**

DBQ PACKAGE
(TOP VIEW)



NC – No internal connection

description

The Direct Rambus clock generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock. It is designed to support Direct Rambus memory on desktop, workstation, server and mobile PC motherboards. DRCG also provides an off-the-shelf solution for a broad range of Direct Rambus memory applications.

The DRCG provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that $PCLK/M = SYNCLK/N$, where $SYNCLK = BUSCLK/4$. The DRCG detects the phase difference between $PCLK/M$ and $SYNCLK/N$ and adjusts the phase of BUSCLK such that the skew between $PCLK/M$ and $SYNCLK/N$ is minimized. This allows data to be transferred across the $SYNCLK/PCLK$ boundary without incurring additional latency.

User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 400 MHz with clock references ranging from 33 MHz to 100 MHz. The CDCR81 meets Rambus Clock Generator, Revision 1.0 specification up to 300 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass the PLL and output REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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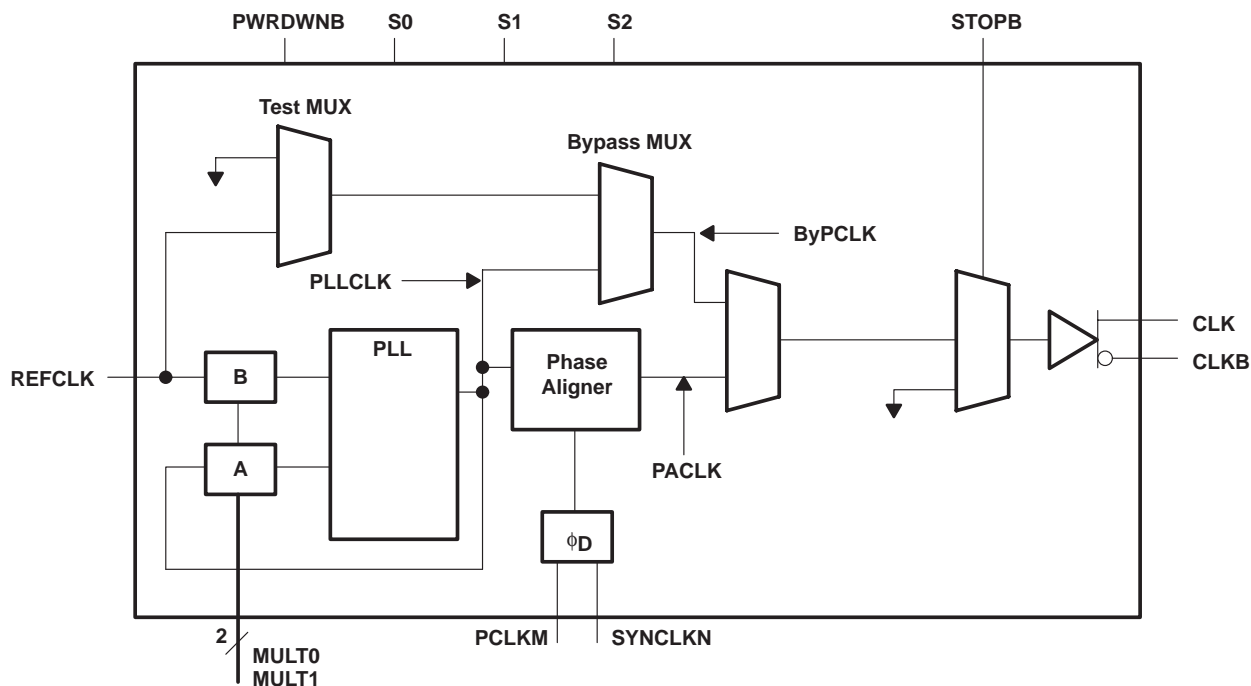
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description (continued)

The CDCR81 is characterized for operation over free-air temperatures of 0°C to 85°C.

functional block diagram



FUNCTION TABLE†

MODE	S0	S1	S2	CLK	CLKB
Normal	0	0	0	Phase aligned clock	Phase aligned clock B
Bypass	1	0	0	PLLCLK	PLLCLKB
Test	1	1	0	REFCLK	REFCLKB
Output test (OE)	0	1	X	Hi-Z	Hi-Z
Reserved	0	0	1	—	—
Reserved	1	0	1	—	—
Reserved	1	1	1	Hi-Z	Hi-Z

† X = don't care, Hi-Z = high impedance

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	20	O	Output clock
CLKB	18	O	Output clock (complement)
GNDC	8		GND for phase aligner
GNDI	5		GND for control inputs
GNDO	17, 21		GND for clock outputs
GNDP	4		GND for PLL
MULT0	15	I	PLL multiplier select
MULT1	14	I	PLL multiplier select
NC	19		Not used
PCLKM	6	I	Phase detector input
PWRDNB	12	I	Active low power down
REFCLK	2	I	Reference clock
S0	24	I	Mode control
S1	23	I	Mode control
S2	13	I	Mode control
STOPB	11	I	Active low output disable
SYNCLKN	7	I	Phase detector input
V _{DDC}	9		V _{DD} for phase aligner
V _{DDIPD}	10		Reference voltage for phase detector inputs and STOPB
V _{DDIR}	1		Reference voltage for REFCLK
V _{DDO}	16, 22		V _{DD} for clock outputs
V _{DDP}	3		V _{DD} for PLL



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PLL divider selection

Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that (267 MHz < BUSCLK < 400 MHz) and (33 MHz < REFCLK < 100 MHz).

Table 1. REFCLK and BUSCLK Frequencies

MULT0	MULT1	REFCLK (MHz)	MULTIPLY RATIO	BUSCLK (MHz)
0	0	67	4	267
0	1	50	6	300
0	1	67	6	400
1	1	33	8	267
1	1	50	8	400
1	0	100	8/3	267

clock output driver states

Table 2. Clock Output Driver States

STATE	PWRDNB	STOPB	CLK	CLKB
Powerdown	0	X	GND	GND
CLK stop	1	0	V _X , STOP	V _X , STOP
Normal	1	1	PACLK/PLLCLK/ REFCLK†	PACLKB/PLLCLKB/ REFCLKB

† Depending on the state of S0, S1, and S2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) -0.5 V to 4 V
 Output voltage range, V_O, at any output terminal -0.5 V to V_{DD} + 0.5 V
 Input voltage range, V_I, at any input terminal -0.5 V to V_{DD} + 0.5 V
 ESD rating TBD
 Continuous total power dissipation see Dissipation Rating Table
 Operating free-air temperature range, T_A 0°C to 85°C
 Storage temperature range, T_{stg} -65°C to 150°C
 Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C‡	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DBQ	1400 mW	11 mW/°C	905 mW	740 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3.135	3.3	3.465	V
High-level input voltage, V_{IH} (CMOS)	$0.7 \times V_{DD}$			V
Low-level input voltage, V_{IL} (CMOS)	$0.3 \times V_{DD}$			V
Initial phase error at phase detector inputs (required range for phase aligner)	$-0.5 \times t_c(\text{PD})$		$0.5 \times t_c(\text{PD})$	
REFCLK low-level input voltage, V_{IL}	$0.3 \times V_{DDIR}$			V
REFCLK high-level input voltage, V_{IH}	$0.7 \times V_{DDIR}$			V
Input signal low voltage, V_{IL} (STOPB)	$0.3 \times V_{DDIPD}$			V
Input signal high voltage, V_{IH} (STOPB)	$0.7 \times V_{DDIPD}$			V
Input reference voltage for (REFCLK) (V_{DDIR})	1.235		3.465	V
Input reference voltage for (PCLKM and SYSCLKN) (V_{DDIPD})	1.235		3.465	V
High-level output current, I_{OH}			-16	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		85	°C

timing requirements

	MIN	MAX	UNIT
Input cycle time, $t_{c(\text{in})}$	10	40	ns
Input cycle-to-cycle jitter		250	ps
Input duty cycle over 10,000 cycles	40%	60%	
Input frequency modulation, f_{mod}	30	33	kHz
Modulation index, non-linear maximum 0.5%		0.6%	
Phase detector input cycle time (PCLKM and SYNCLKN)	30	100	ns
Input slew rate, SR	1	4	V/ns
Input duty cycle (PCLKM and SYNCLKN)	25%	75%	



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT	
$V_{O(STOP)}$	Output voltage during CLK Stop (StopB=0)	See Figure 1	1.1		2		
$V_{O(X)}$	Output crossing-point voltage	See Figures 1 and 6	1.3		1.8	V	
V_O	Output voltage swing	See Figure 1	0.4		0.6	V	
V_{IK}	Input clamp voltage	$V_{DD} = 3.135\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V	
V_{OH}	High-level output voltage	See Figure 1			2	V	
		$V_{DD} = \text{min to max}$, $I_{OH} = -1\text{ mA}$	$V_{DD} - 0.1\text{ V}$				
		$V_{DD} = 3.135\text{ V}$, $I_{OH} = -16\text{ mA}$	2.4				
V_{OL}	Low-level output voltage	See Figure 1	1			V	
		$V_{DD} = \text{min to max}$, $I_{OL} = 1\text{ mA}$			0.1		
		$V_{DD} = 3.135\text{ V}$, $I_{OL} = 16\text{ mA}$			0.5		
I_{OH}	High-level output current	$V_{DD} = 3.135\text{ V}$, $V_O = 1\text{ V}$	-32	-52		mA	
		$V_{DD} = 3.3\text{ V}$, $V_O = 1.65\text{ V}$		-51			
		$V_{DD} = 3.465\text{ V}$, $V_O = 3.135\text{ V}$	-14.5	-21			
I_{OL}	Low-level output current	$V_{DD} = 3.135\text{ V}$, $V_O = 1.95\text{ V}$	43	61.5		mA	
		$V_{DD} = 3.3\text{ V}$, $V_O = 1.65\text{ V}$		65			
		$V_{DD} = 3.465\text{ V}$, $V_O = 0.4\text{ V}$		25.5	36		
I_{OZ}	High-impedance-state output current	$S_0 = 0$, $S_1 = 1$			± 10	μA	
$I_{OZ(STOP)}$	High-impedance-state output current during CLK stop	Stop=0, $V_O = \text{GND or } V_{DD}$			± 100	μA	
$I_{OZ(PD)}$	High-impedance-state output current in powerdown state	PWRDNB=0, $V_O = \text{GND or } V_{DD}$	-10		100	μA	
I_{IH}	High-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	$V_{DD} = 3.465\text{ V}$, $V_I = V_{DD}$		10	μA	
		PWRDNB, S0, S1, S2, MULT0, MULT1	$V_{DD} = 3.465\text{ V}$, $V_I = V_{DD}$		10		
I_{IL}	Low-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	$V_{DD} = 3.465\text{ V}$, $V_I = 0$		-10	μA	
		PWRDNB, S0, S1, S2, MULT0, MULT1	$V_{DD} = 3.465\text{ V}$, $V_I = 0$		-10		
Z_O	Output impedance	High state	R_I at $I_O -14.5\text{ mA to } -16.5\text{ mA}$	15	26	40	Ω
		Low state	R_I at $I_O 14.5\text{ mA to } 16.5\text{ mA}$	11	17	35	
	Reference current	V_{DDIR} , V_{DDIPD}	$V_{DD} = 3.465\text{ V}$,	PWRDNB = 0		50	μA
				PWRDNB = 1		0.5	mA
C_I	Input capacitance	$V_I = V_{DD}$ or GND		1.8		pF	
C_O	Output capacitance	$V_O = V_{DD}$ or GND		3.1		pF	
$I_{DD(PD)}$	Supply current in powerdown state	REFCLK = 0 MHz to 100 MHz, PWRDNB = 0, STOPB = 1			200	μA	
$I_{DD(CLKSTOP)}$	Supply current in CLK stop state	BUSCLK configured for 400 MHz			30	mA	
$I_{DD(NORMAL)}$	Supply current in normal state	BUSCLK = 400 MHz			70	mA	

† V_{DD} refers to any of the following: V_{DD} , V_{DDIPD} , V_{DDIR} , V_{DDO} , V_{DDC} , and V_{DDP}

‡ All typical values are at $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(out)}$	Clock output cycle time			2.5		3.75	ns
$t_{(jitter)}$	Total cycle jitter over 1, 2, 3, 4, 5, or 6 clock cycles	Stopped phase alignment	267 MHz – 400 MHz	See Figure 3		60	ps
		Infinite phase alignment	267 MHz	See Figure 3		80	
			300 MHz			70	ps
$t_{(phase)}$	Phase detector phase error for distributed loop		Static phase error	-50		50	ps
$t_{(phase, SSC)}$	PLL output phase error when tracking SSC		Dynamic phase error	-100		100	ps
$t_{(DC)}$	Output duty cycle over 10,000 cycles		See Figure 4	45%		55%	
$t_{(DC, err)}$	Output cycle-to-cycle duty cycle error	Stopped phase alignment	267 MHz – 400 MHz	See Figure 5		50	ps
			Infinite phase alignment	267 MHz	See Figure 5		
		300 MHz				80	ps
		400 MHz			90		
t_r, t_f	Output rise and fall times (measured at 20%-80% of output voltage)		See Figure 7	200		450	ps
Δt	Difference between rise and fall times on a single device (20%–80%) $ t_f - t_r $		See Figure 7			100	ps

† All typical values are at $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

state transition latency specifications

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB↑ to CLK/CLKB output settled (excluding $t_{(DISTLOCK)}$)	Power-down	Normal	See Figure 8			3	ms
	Delay time, PWRDNB↑ to internal PLL and clock are on and settled						3	
$t_{(VDDpowerup)}$	Delay time, powerup to CLK/CLKB output settled	V_{DD}	Normal	See Figure 8			3	ms
	Delay time, powerup to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLK/CLKB output resettled (excluding $t_{(DISTLOCK)}$)	Normal	Normal	See Figure 9			1	ms
$t_{(CLKON)}$	STOPB↑ to CLK/CLKB glitch-free clock edges	CLK Stop	Normal	See Figure 10			10	ns
$t_{(CLKSETL)}$	STOPB↑ to CLK/CLKB output settled to within 50 ps of the phase before STOPB was disabled	CLK Stop	Normal	See Figure 10			20	cycles
$t_{(CLKOFF)}$	STOPB↑ to CLK/CLKB output disabled	Normal	CLK Stop	See Figure 10			5	ns
$t_{(powerdown)}$	Delay time, PWRDNB↓ to the device in power-down mode	STOPB	Power-down				1	ms
$t_{(STOP)}$	Maximum time in CLKSTOP (STOPB = 0) before re-entering normal mode (STOPB = 1)	STOPB	Normal				100	μs



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state transition latency specifications (continued)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t(ON)	Normal	CLK stop		100			ms
t(DISTLOCK)	Un-locked	Locked				5	ms

PARAMETER MEASUREMENT INFORMATION

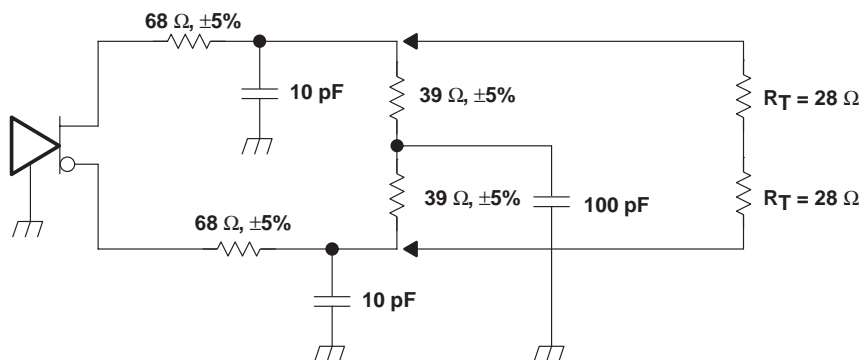
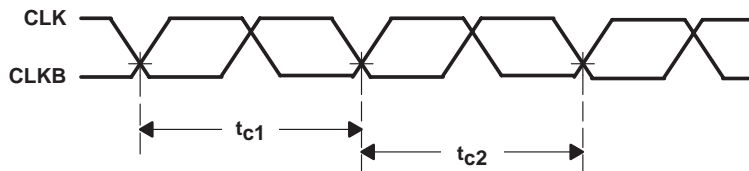
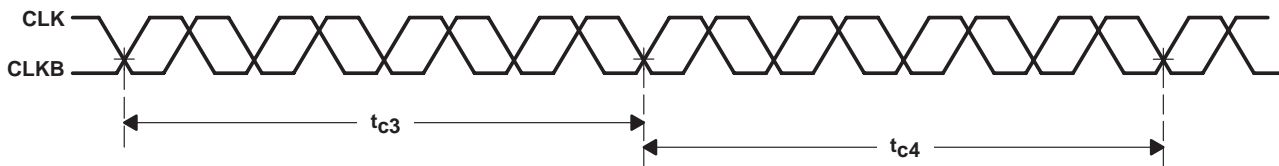


Figure 1. Test Load and Voltage Definitions ($V_{O(STOP)}$, $V_{O(X)}$, V_O , V_{OH} , V_{OL})



Cycle-to-cycle jitter = $|t_{c1} - t_{c2}|$ over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter



Cycle-to-cycle jitter = $|t_{c3} - t_{c4}|$ over 10000 consecutive cycles

Figure 3. Short Term Cycle-to-Cycle Jitter over 4 Cycles

PARAMETER MEASUREMENT INFORMATION

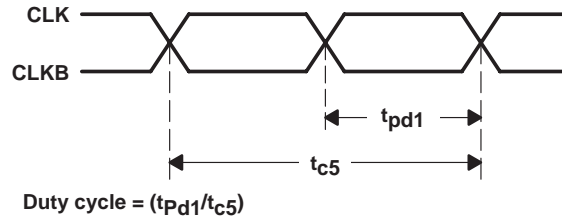


Figure 4. Output Duty Cycle

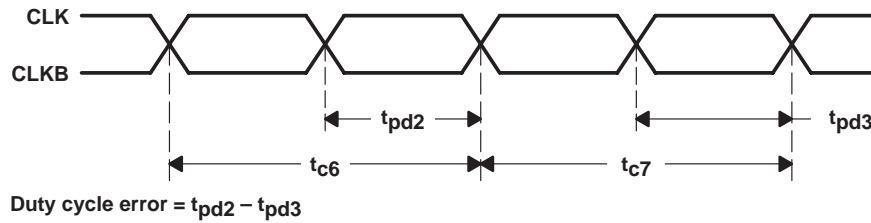


Figure 5. Duty Cycle Error (Cycle-to-Cycle)

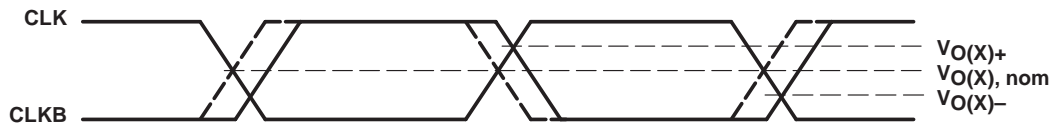


Figure 6. Crossing-Point Voltage



Figure 7. Voltage Waveforms

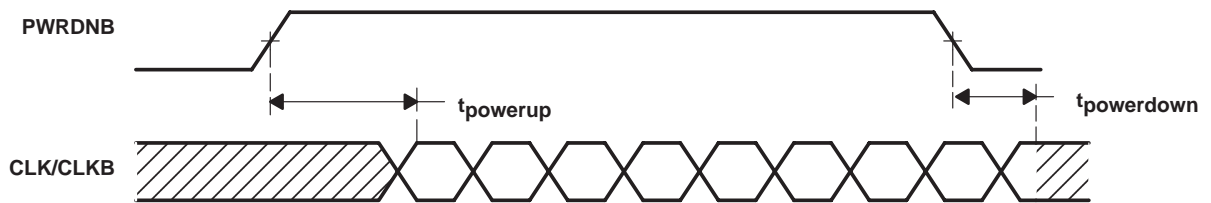


Figure 8. PWRDNB Transition Timings

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PARAMETER MEASUREMENT INFORMATION

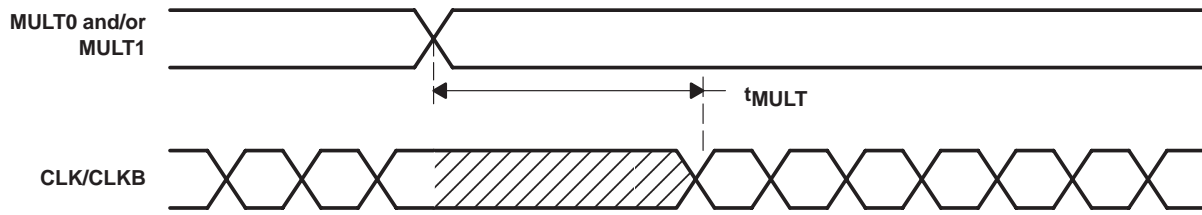
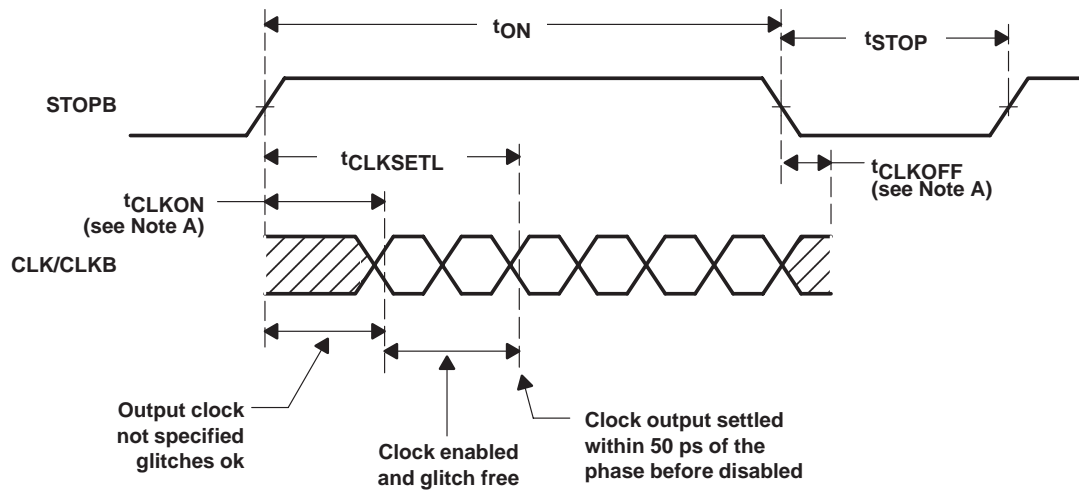


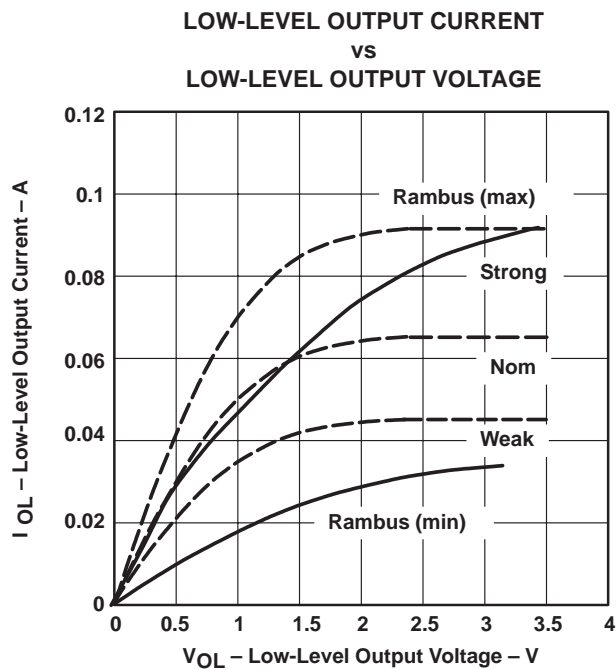
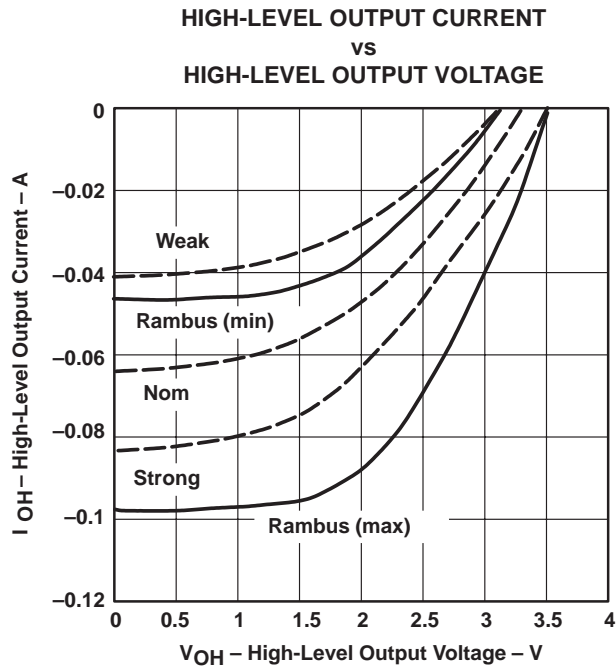
Figure 9. MULT Transition Timings



NOTE A: $V_{ref} = V_O \pm 200 \text{ mV}$

Figure 10. STOPB Transition Timings

PARAMETER MEASUREMENT INFORMATION



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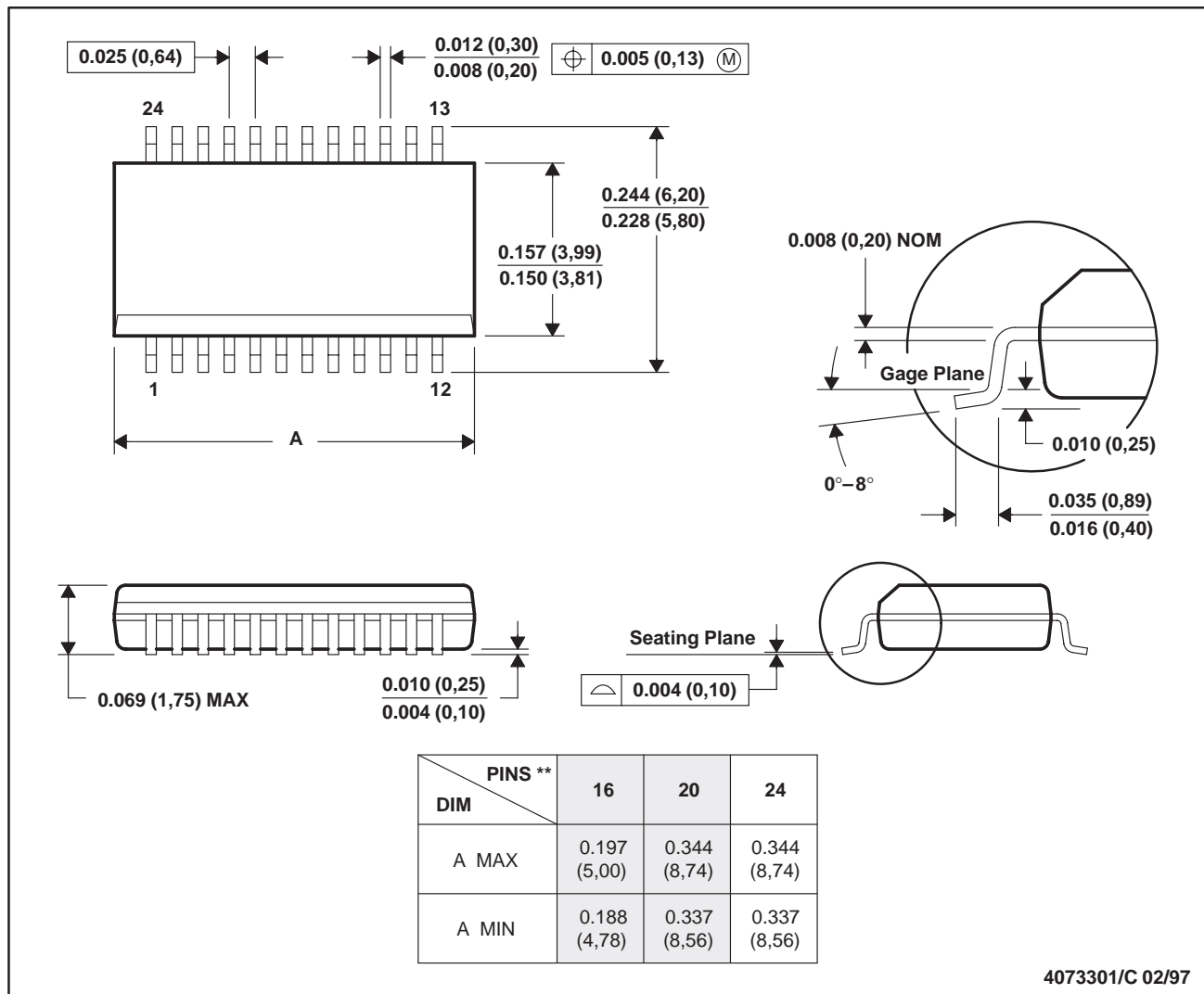
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MECHANICAL DATA

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

24-PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137

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