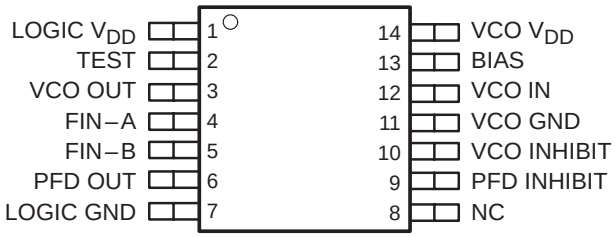
TLC2933
HIGH-PERFORMANCE PHASE-LOCKED LOOP

SLAS136A – APRIL 1996 – REVISED JUNE 1997

- **Voltage-Controlled Oscillator (VCO) Section:**
  - **Ring Oscillator Using Only One External Bias Resistor (R_{BIAS})**
  - **Lock Frequency:**
    43 MHz to 100 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1 Output)
    37 MHz to 55 MHz (V_{DD} = 3 V ±5%, T_A = –20°C to 75°C)
- **Phase-Frequency Detector (PFD) Section Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 terminal)**
- **CMOS Technology**
- **Typical Applications:**
  - **Frequency Synthesis**
  - **Modulation/Demodulation**
  - **Fractional Frequency Division**
- **CMOS Input Logic Level**

PW PACKAGE†
(TOP VIEW)

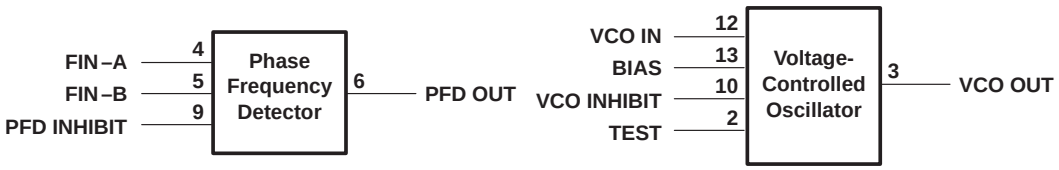


† Available in tape and reel only and ordered as the TLC2933PWLE.
NC – No internal connection

description

The TLC2933 is designed for phase-locked-loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The high-speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions that can be used as a power-down mode. With the high-speed and stable VCO characteristics, the TLC2933 is well suited for use in high-performance PLL systems.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
–20°C to 75°C	TLC2933PWLE

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BIAS	13	I	Bias supply. An external resistor (R_{BIAS}) between VCO V_{DD} and BIAS supplies bias for adjusting the oscillation frequency range.
FIN–A	4	I	Input reference frequency $f_{(REF\ IN)}$ is applied to FIN–A.
FIN–B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN–B is nominally provided from the external counter.
LOGIC GND	7		Ground for the internal logic.
LOGIC V_{DD}	1		Power supply for the internal logic. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.
NC	8		No internal connection.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD OUT is in the high-impedance state, see Table 2.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD OUT is in the high-impedance state.
TEST	2	I	Test terminal. TEST connects to ground for normal operation.
VCO GND	11		Ground for VCO.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low (see Table 1).
VCO OUT	3	O	VCO output. When VCO INHIBIT is high, VCO OUT is low.
VCO V_{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V_{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. While all resistor values within the specified range result in excellent low temperature coefficients, the bias resistor value for the minimum temperature coefficient is nominally 2.2 kΩ with 3-V V_{DD} and nominally 2.4 kΩ with 5-V V_{DD}. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

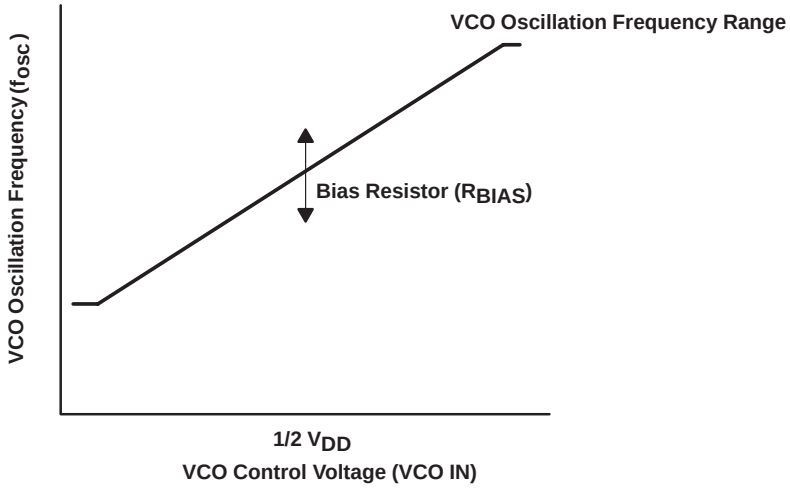


Figure 1. VCO Oscillation Frequency

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibits the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode as shown in Table 1.

Table 1. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUT	$I_{DD(VCO)}$
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN–A and FIN–B as shown in Figure 2. Nominally the reference is supplied to FIN–A, and the frequency from the external counter output is fed to FIN–B. For clock recovery PLL systems, other types of phase detectors should be used.

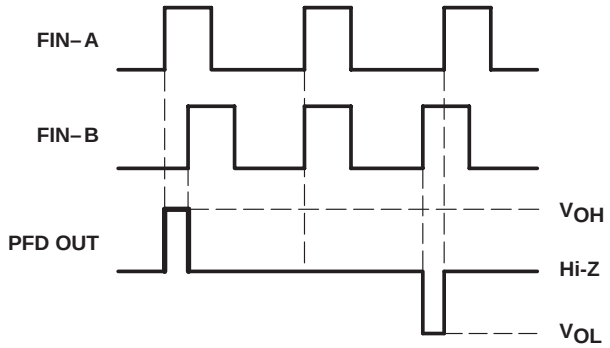


Figure 2. PFD Function Timing Chart

PFD inhibit control

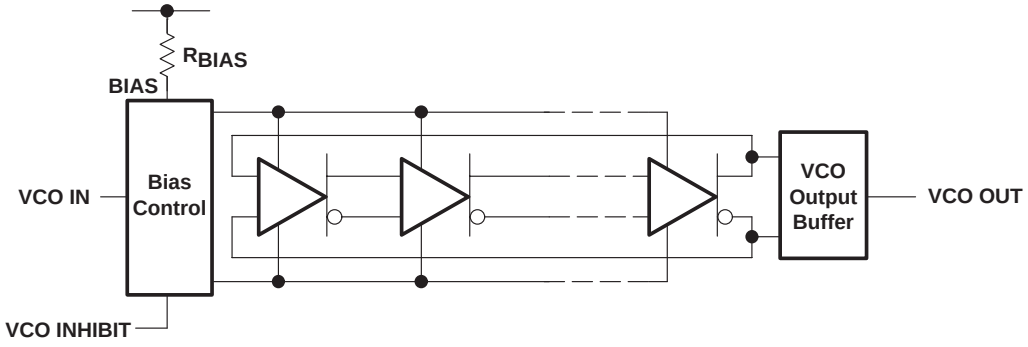
A high level on the PFD INHIBIT terminal places PFD OUT in the high-impedance state and the PFD stops phase detection as shown in Table 2. A high level on the PFD INHIBIT terminal can also be used as the power-down mode for the PFD.

Table 2. VCO Output Control Function

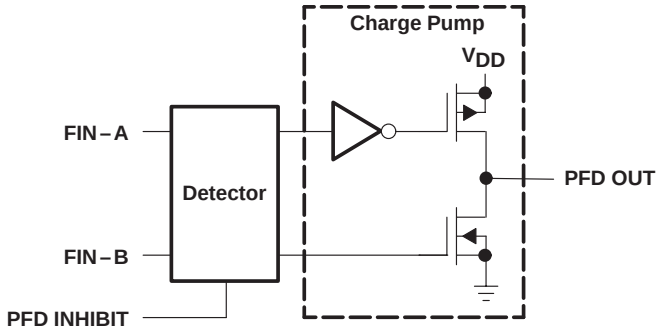
PFD INHIBIT	DETECTION	PFD OUT	$I_{DD(PFD)}$
Low	Active	Active	Normal
High	Stopped	Hi-Z	Power Down

schematics

VCO block schematic



PFD block schematic



absolute maximum ratings†

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_I (see Note 1)	–0.3 V to V_{DD} + 0.3 V
Input current (each input), I_I	±20 mA
Output current (each output), I_O	±20 mA
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2)	700 mW
Operating free-air temperature range, T_A	–20°C to 75°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage, V_I (inputs except VCO IN)		0		V_{DD}	V
Output current, I_O (each output)		0		±2	mA
VCO control voltage at VCO IN		1		V_{DD}	V
Lock frequency	V_{DD} = 3 V	37		55	MHz
	V_{DD} = 5 V	43		100	
Bias resistor, R_{BIAS}	V_{DD} = 3 V	1.8		2.7	kΩ
	V_{DD} = 5 V	2.2		3	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) be at the same voltage and separated from each other.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.3	V
V_{IT+}	Positive input threshold voltage at TEST, VCO INHIBIT		0.9	1.5	2.1	V
I_I	Input current at TEST, VCO INHIBIT	V_I = V_{DD} or ground			±1	µA
$Z_{i(VCO\ IN)}$	Input impedance at VCO IN	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 5		5.1	15	mA

NOTES: 4. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.
5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = 1/2 V_{DD}, R_{BIAS} = 2.4 kΩ, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, V_I = V_{DD} or ground			±1	µA
V_{IH}	High-level input voltage at FIN–A, FIN–B		2.1			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				0.9	V
V_{IT+}	Positive input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_i	Input capacitance at FIN–A, FIN–B			5		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.7	4	mA

NOTES: 6. The current into LOGIC V_{DD} when FIN–A and FIN–B = ground, PFD INHIBIT = V_{DD}, PFD OUT open, and VCO OUT is inhibited.
7. The current into LOGIC V_{DD} when FIN–A and FIN–B = 30 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 2.4 kΩ, VCO IN = 1/2 V_{DD}	38	48	55	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time, VCO OUT↑	C_L = 15 pF, See Figure 3		3.3	10	ns
t_f	Fall time, VCO OUT↓	C_L = 15 pF, See Figure 3		2	8	ns
	Duty cycle at VCO OUT	R_{BIAS} = 2.4 kΩ, VCO IN = 1/2 V_{DD}	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.4 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.03		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 2.4 kΩ, VCO IN = 1.5 V, V_{DD} = 2.85 V to 3.15 V		0.04		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 2.4 kΩ		100		ps

NOTES: 8. The time period to stabilize the VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed printed circuit board (PCB) with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		30			MHz
t_{PLZ}	Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z	See Figures 4 and 5 and Table 3		20	40	ns
t_{PHZ}	Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z			18	40	
t_{PZL}	Enable time, PFD INHIBIT↓ to PFD OUT low			4.1	18	ns
t_{PZH}	Enable time, PFD INHIBIT↓ to PFD OUT high			4.8	18	
t_r	Rise time, PFD OUT↑	C_L = 15 pF, See Figure 4		3.1	9	ns
t_f	Fall time, PFD OUT↓			1.5	9	ns

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
V_{IT+}	Positive input threshold voltage at TEST, VCO INHIBIT		1.5	2.5	3.5	V
I_I	Input current at TEST, VCO INHIBIT	V_I = V_{DD} or ground			±1	µA
$Z_{i(VCO\ IN)}$	Input impedance at VCO IN	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 5		14	35	mA

NOTES: 4. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD}, and PFD INHIBIT high.
5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = 1/2 V_{DD}, R_{BIAS} = 2.4 kΩ, VCO INHIBIT = ground, and PFD INHIBIT high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, V_I = V_{DD} or ground			±1	µA
V_{IH}	High-level input voltage at FIN–A, FIN–B		3.5			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				1.5	V
V_{IT+}	Positive input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_i	Input capacitance at FIN–A, FIN–B			7		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 10		2.6	8	mA

NOTES: 6. The current into LOGIC V_{DD} when FIN–A and FIN–B = ground, PFD INHIBIT = V_{DD}, PFD OUT open, and VCO OUT is inhibited.
10. The current into LOGIC V_{DD} when FIN–A and FIN–B = 50 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), PFD INHIBIT = ground, PFD OUT open, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 2.4 kΩ,, VCO IN = 1/2 V_{DD}	64	80	96	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time, VCO OUT↑	C_L = 15 pF, See Figure 3		2.1	5	ns
t_f	Fall time, VCO OUT↓	C_L = 15 pF, See Figure 3		1.5	4	ns
	Duty cycle at VCO OUT	R_{BIAS} = 2.4 kΩ, VCO IN = 1/2 V_{DD}	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.4 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.03		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 2.4 kΩ, VCO IN = 2.5 V, V_{DD} = 4.75 V to 5.25 V		0.02		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 2.4 kΩ		100		ps

NOTES: 8: The time period to stabilize the VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed printed circuit board (PCB) with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		50			MHz
t_{PLZ}	Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z	See Figures 4 and 5 and Table 3		20	40	ns
t_{PHZ}	Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z			17	40	
t_{PZL}	Enable time, PFD INHIBIT↓ to PFD OUT low			3.7	10	ns
t_{PZH}	Enable time, PFD INHIBIT↓ to PFD OUT high			3.4	10	
t_r	Rise time, PFD OUT↑	C_L = 15 pF, See Figure 4		1.7	5	ns
t_f	Fall time, PFD OUT↓			1.3	5	ns

PARAMETER MEASUREMENT INFORMATION

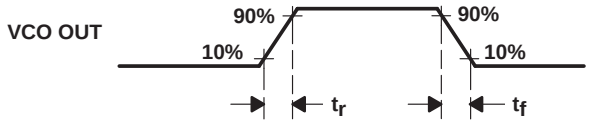
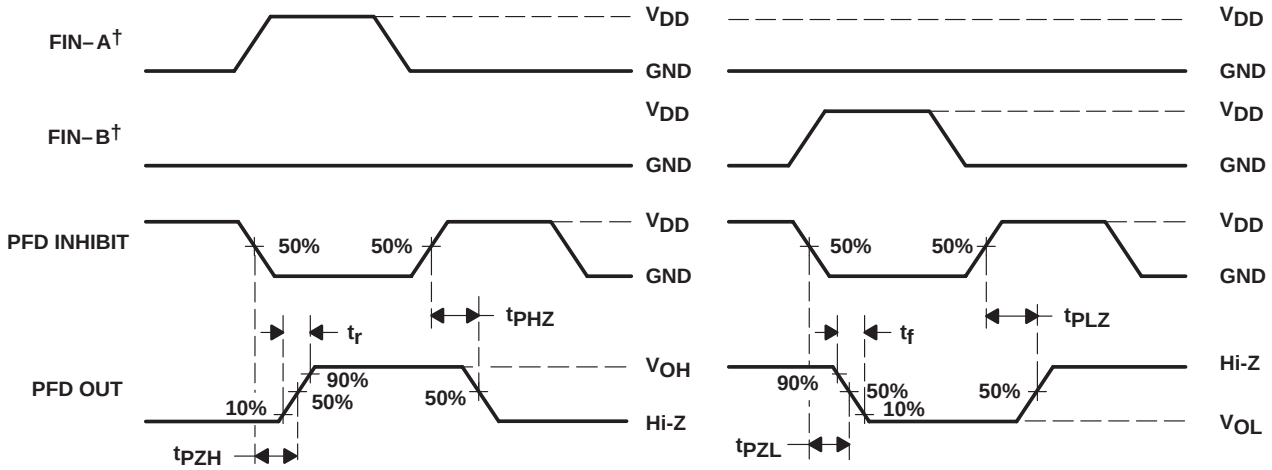


Figure 3. VCO Output Voltage Waveform



(a) PFD OUT Hi-Z Timing To and From a High Level (see Figure 5 and Table 3)

(b) PFD OUT Hi-Z Timing To and From a Low Level (see Figure 5 and Table 3)

† FIN–A and FIN–B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

Table 3. PFD Output Test Conditions

PARAMETER	R_L	C_L	S_1	S_2
t_{PZH}	1 kΩ	15 pF	Open	Closed
t_{PHZ}				
t_r				
t_{PZL}			Closed	Open
t_{PLZ}				
t_f				

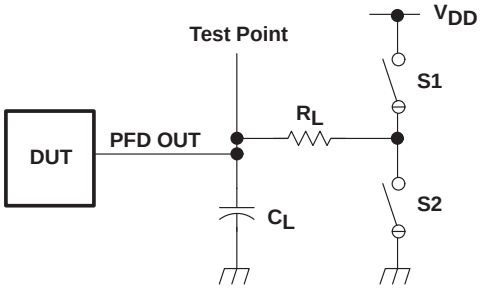


Figure 5. PFD Output Test Conditions

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

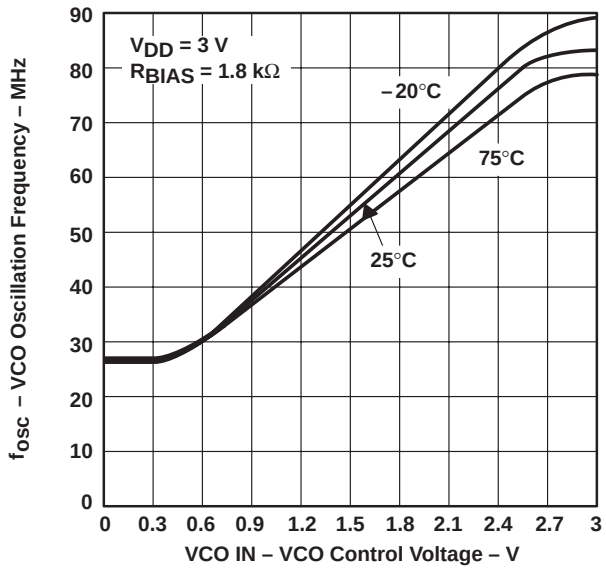


Figure 6

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

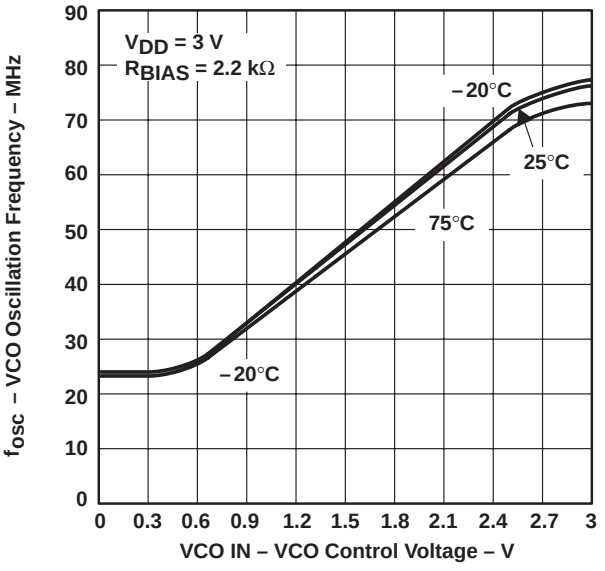


Figure 7

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

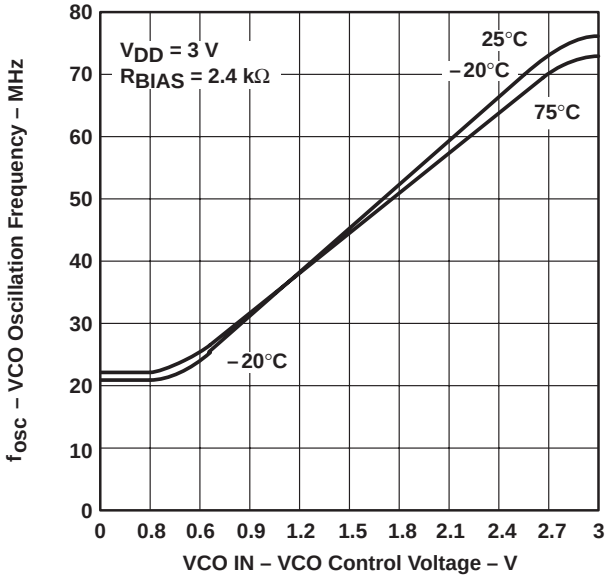


Figure 8

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

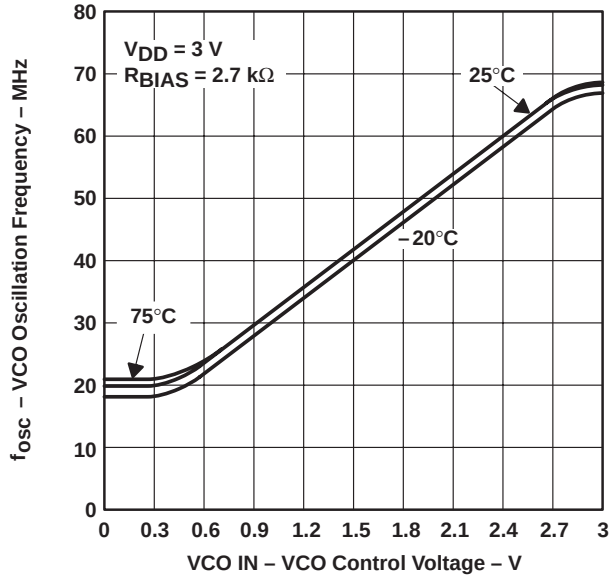


Figure 9

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

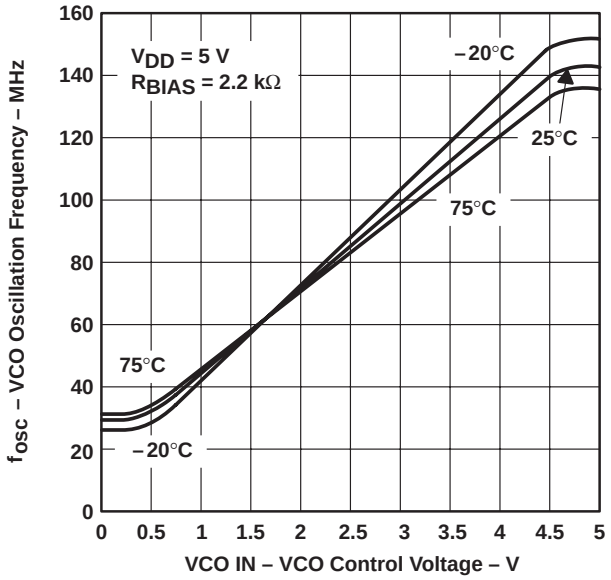


Figure 10

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

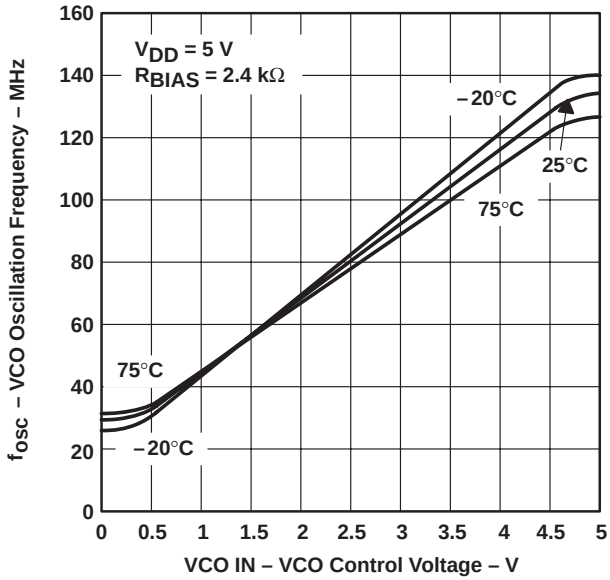


Figure 11

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

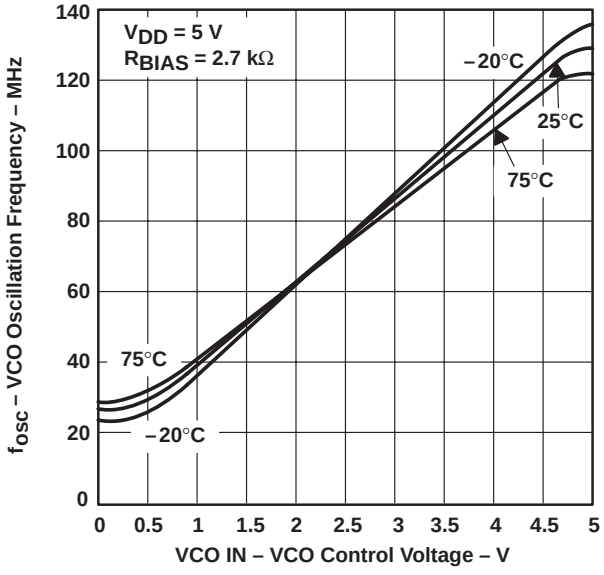


Figure 12

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

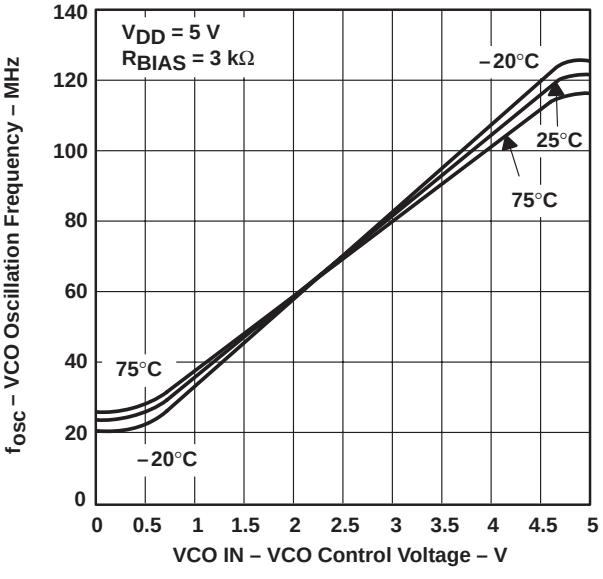


Figure 13

TYPICAL CHARACTERISTICS

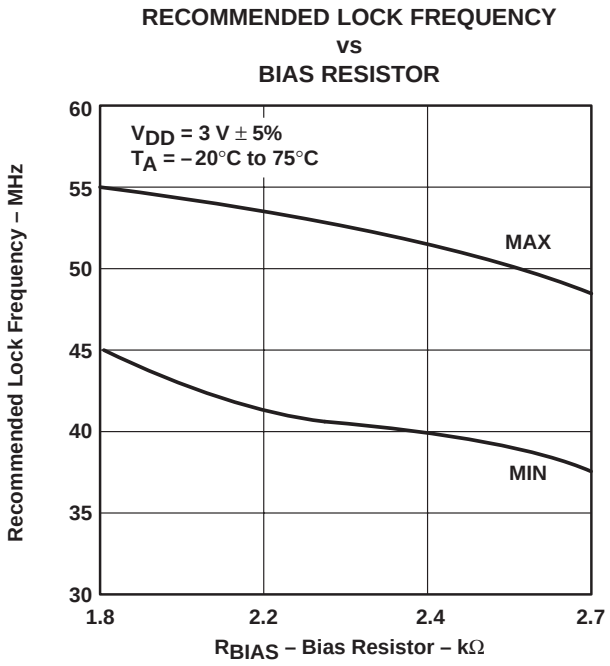


Figure 14

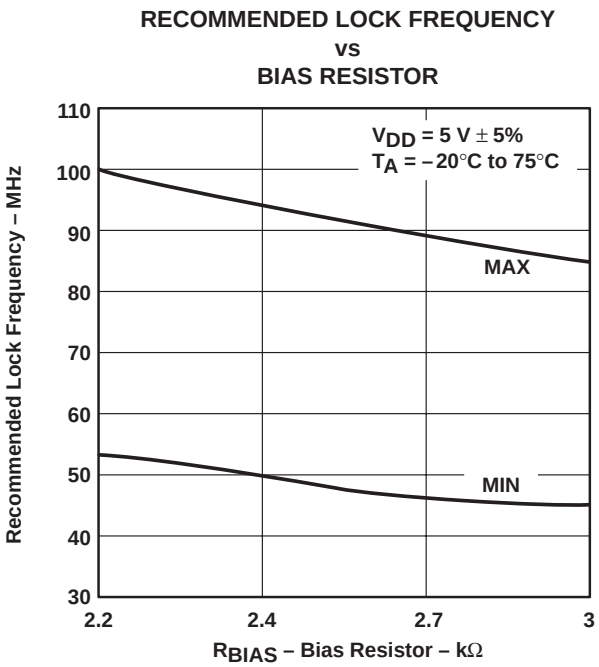


Figure 15

APPLICATION INFORMATION

gain of VCO and PFD

Figure 16 is a block diagram of the PLL. The divider N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 16. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 16(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 16(c).

The parameters for the block diagram with the units are as follows:

K_V : VCO gain (rad/s/V)
K_p : PFD gain (V/rad)
K_f : LPF gain (V/V)
K_N : countdown divider gain (1/N)

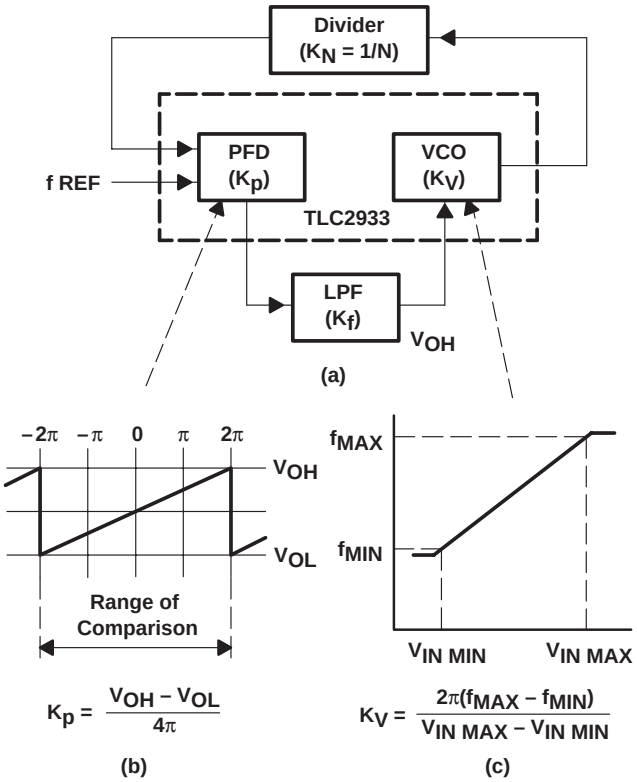


Figure 16. Example of a PLL Block Diagram

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

R_{BIAS}

The external bias resistor sets the VCO center frequency with 1/2 V_{DD} applied to the VCO IN terminal. For the most accurate results, a metal-film resistor is the better choice but a carbon-composition resistor can also be used with excellent results. A 0.22 μF capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 17 is as follows:

$$\Delta\omega_H \simeq 0.8 \left(K_p\right) \left(K_V\right) \left(K_f\ (\infty)\right) \quad (1)$$

Where

$K_f\ (\infty)$ = the filter transfer function value at $\omega = \infty$

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low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 17. When the active filter of Figure 17(c) is used, the reference should be applied to FIN-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

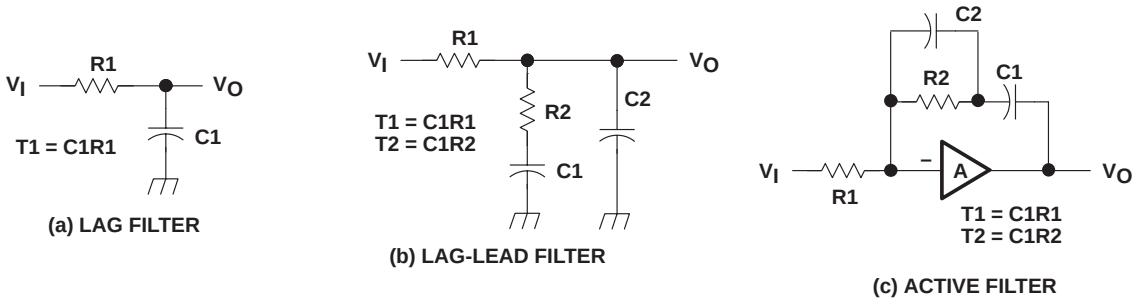

Figure 17. LPF Examples for PLL

the passive filter

The transfer function for the low-pass filter shown in Figure 17(b) is;

$$\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T2}{1 + s \cdot (T1 + T2)} \qquad (2)$$

where

$$T1 = R1 \cdot C1 \text{ and } T2 = R2 \cdot C1$$

Using this filter makes the closed-loop PLL system a type 1 second-order system. The response curves of this system to a unit step are shown in Figure 18.

the active filter

When using the active filter shown in Figure 17(c), the phase detector inputs must be reversed since the filter adds an additional inversion. Therefore, the input reference frequency should be applied to the FIN-B terminal and the output of the VCO divider should be applied to the input reference terminal, FIN-A.

The transfer function for the active filter shown in Figure 17(c) is:

$$F(s) = \frac{1 + s \cdot R2 \cdot C1}{s \cdot R1 \cdot C1} \qquad (3)$$

Using this filter makes the closed-loop PLL system a type 2 second-order system. The response curves of this system to a unit step are shown in Figure 19.

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Using the lag-lead filter in Figure 17(b) and divider N value, the transfer function for phase and frequency are shown in equations 4 and 5. Note that the transfer function for phase differs from the transfer function for frequency by only the divider N value. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, the transfer function of Figure 17(a) for phase is

$$\frac{\Phi 2(s)}{\Phi 1(s)} = \frac{K_p \cdot K_V}{N \cdot (T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \quad (4)$$

and the transfer function for frequency is

$$\frac{F_{OUT(s)}}{F_{REF(s)}} = \frac{K_p \cdot K_V}{(T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \cdot \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \quad (5)$$

The standard 2-pole denominator is $D = s^2 + 2\,\zeta\,\omega_n\,s + \omega_n^2$ and comparing the coefficients of the denominator of equation (4) and (5) with the standard 2-pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \quad (6)$$

Solving for T1 + T2

$$T1 + T2 = \frac{K_p \cdot K_V}{N \cdot \omega_n^2}$$

and by using this value for T1 + T2 in equation (6) the damping factor is

$$\zeta = \frac{\omega_n}{2} \cdot \left(T2 + \frac{N}{K_p \cdot K_V} \right) \quad (7)$$

solving for T2

$$T2 = \frac{2\,\zeta}{\omega} - \frac{N}{K_p \cdot K_V} \quad (8)$$

then by substituting for T2 in equation (6)

$$T1 = \frac{K_V \cdot K_p}{N \cdot \omega_n^2} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \quad (9)$$

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From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2\,\zeta}{\omega_n} - \frac{N}{K_p \cdot K_V}\right]\frac{1}{C1} \tag{10}$$

$$R1 = \left[\frac{K_p \cdot K_v}{\omega_n{}^2 \cdot N} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V}\right]\frac{1}{C1} \tag{11}$$

The capacitor, C1, is usually chosen between 1 μF and 0.1 μF to allow for reasonable resistor values and physical capacitor size.

APPLICATION INFORMATION

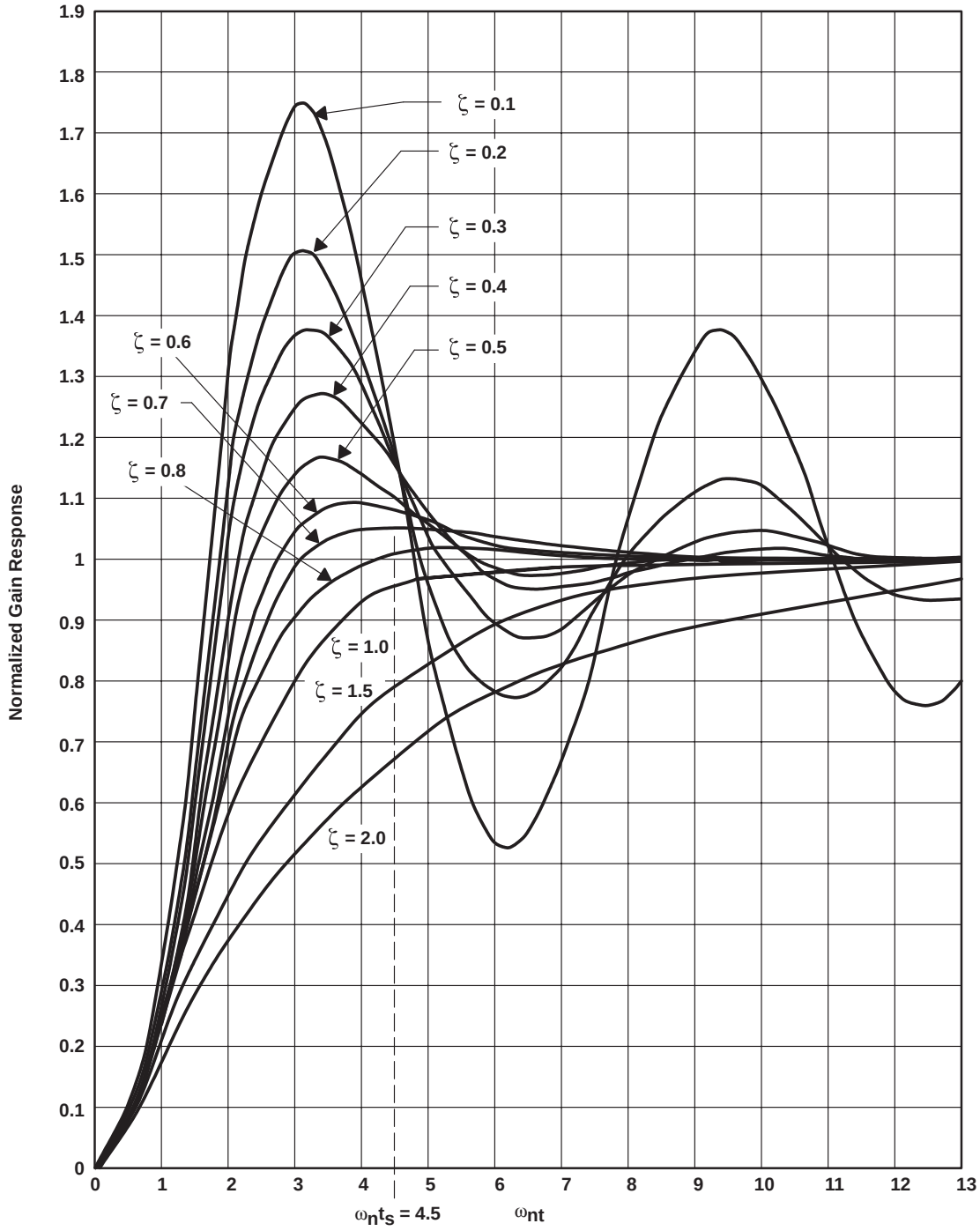

Figure 18. Type 1 Second-Order Step Response

APPLICATION INFORMATION

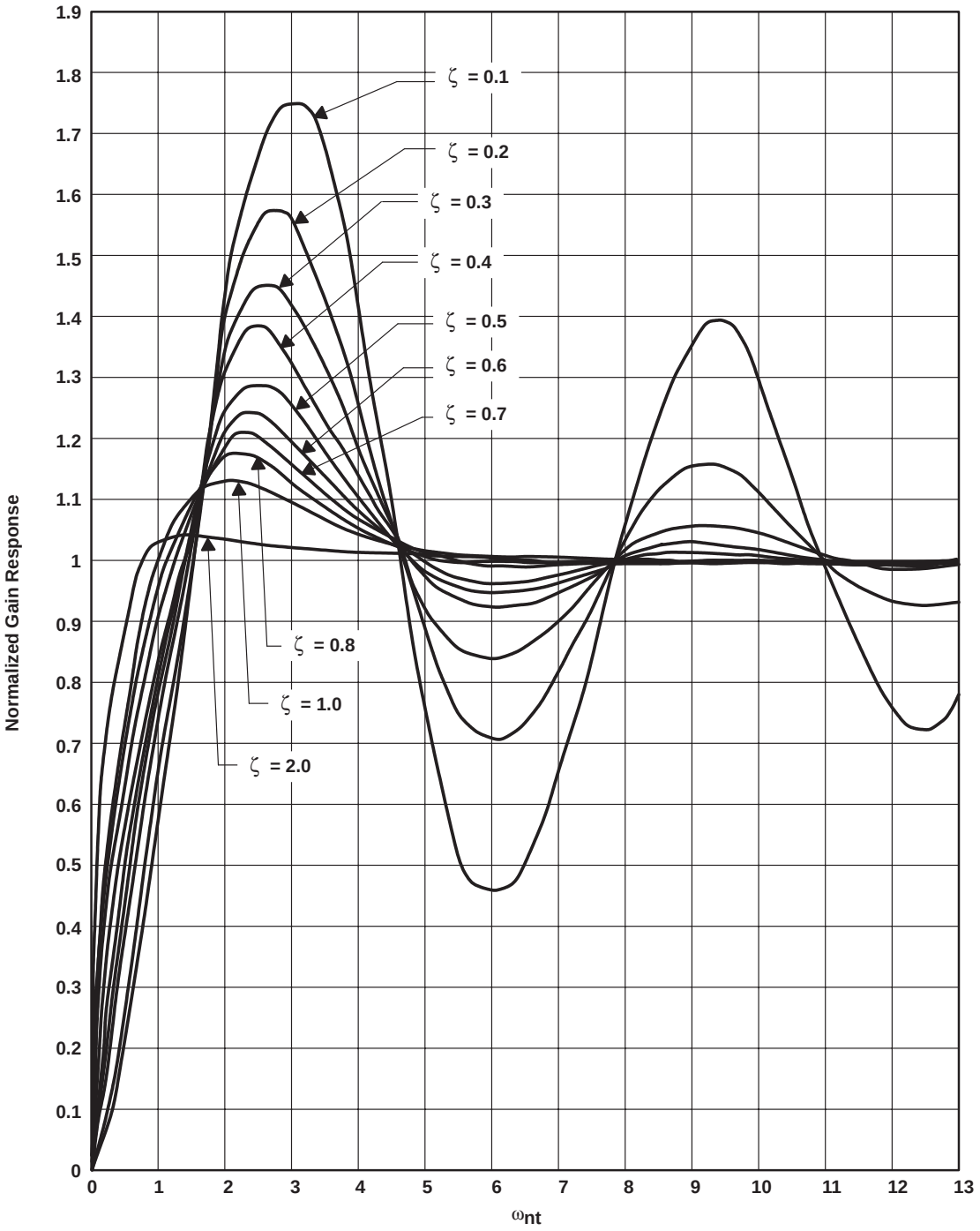

Figure 19. Type 2 Second-Order Step Response

APPLICATION INFORMATION

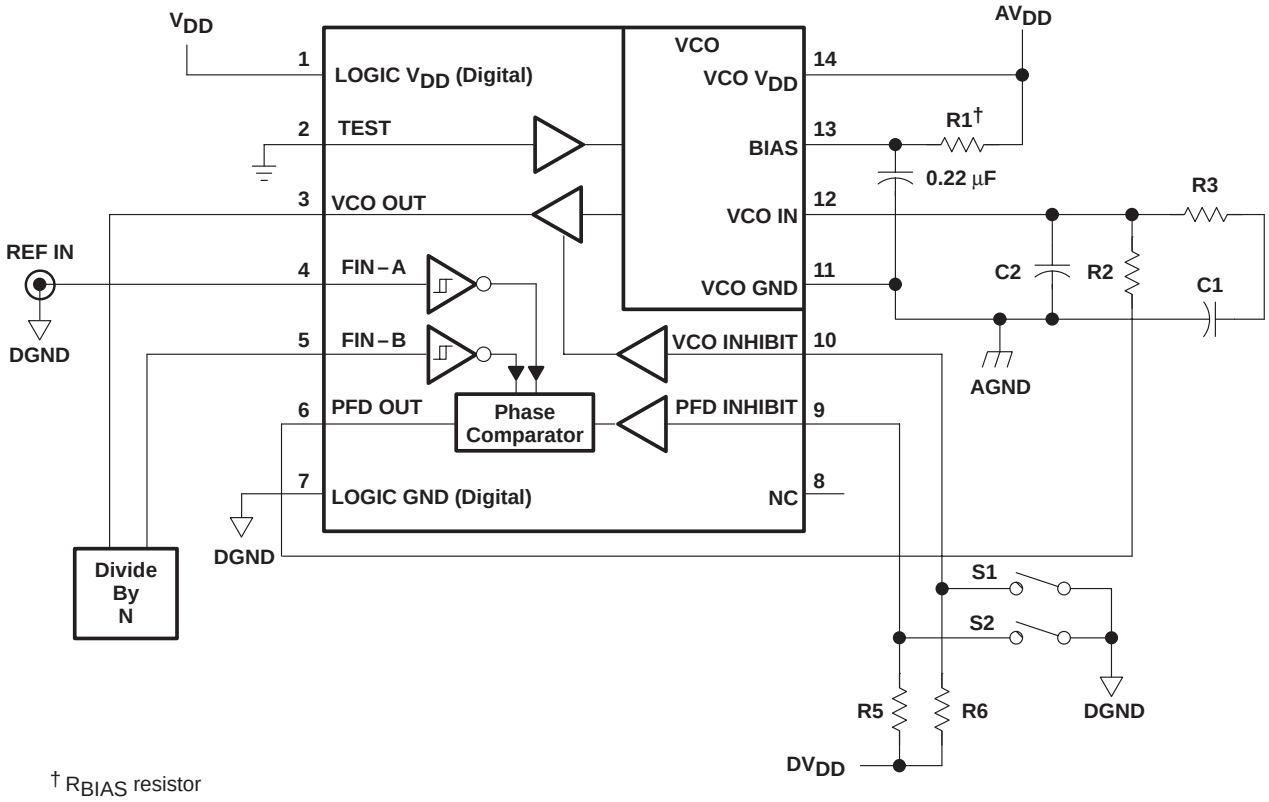

Figure 20. Evaluation and Operation Schematic

PCB layout considerations

The TLC2933 contains a high frequency oscillator; therefore, very careful breadboarding and PCB layout is required for evaluation.

The following design recommendations benefit the TLC2933 user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- Radio frequency (RF) breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to ground and LOGIC V_{DD} to ground should be decoupled with a 0.1-µF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to ground to prevent stray pickup.

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