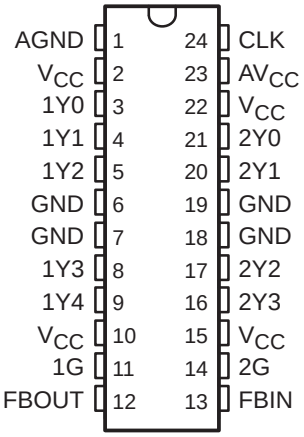
- **Designed to Meet and Exceed PC133 SDRAM Registered DIMM Specification Rev. 1.1**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency 50 MHz to 175 MHz**
- **Static Phase Error Distribution at 66MHz to 166 MHz is ±125 ps**
- **Jitter (cyc – cyc) at 66 MHz to 166 MHz is |70| ps**
- **Advanced Deep Sub-Micron Process Results in More Than 40% Lower Power Consumption Versus Current Generation PC133 Devices**
- **Available in Plastic 24-Pin TSSOP**
- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback (FBIN) Terminal Is Used to Synchronize the Outputs to the Clock Input**
- **25-Ω On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Operates at 3.3 V**

PW PACKAGE
(TOP VIEW)



description

The CDCVF2509 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDCVF2509 operates at 3.3 V V_{CC}. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK. Each bank of outputs is enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDCVF2509 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDCVF2509 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, and following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

The CDCVF2509 is characterized for operation from 0°C to 85°C.

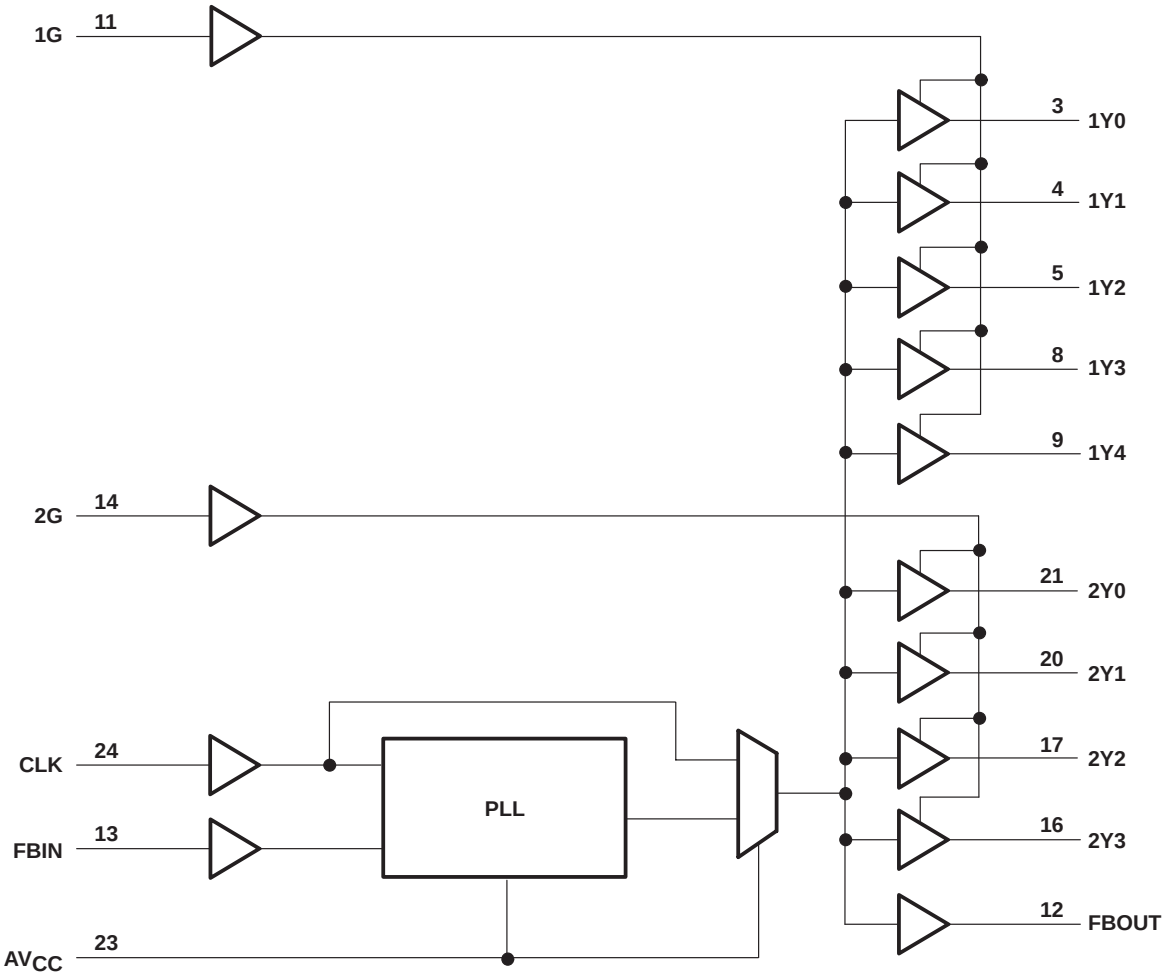
description (continued)

For application information refer to application reports *High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516* (literature number SLMA003) and *Using CDC2509A/2510A PLL with Spread Spectrum Clocking (SSC)* (literature number SCAA039).

FUNCTION TABLE

INPUTS			OUTPUTS		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 85°C	CDCVF2509PWR

Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDCVF2509 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25-Ω series-damping resistor.
1Y (0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25-Ω series-damping resistor.
2Y (0:3)	21, 20, 17, 16	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated 25-Ω series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{CC} (see Note 1) . . . . . $AV_{CC} < V_{CC} + 0.7$ V
Supply voltage range, V_{CC} . . . . . –0.5 V to 4.3 V
Input voltage range, V_I (see Note 2) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or low state,
V_O (see Notes 2 and 3) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 4) . . . . . 0.7 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. AV_{CC} **must not** exceed V_{CC}+ 0.7 V
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 4.6 V maximum.
4. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

DISSIPATION RATING TABLE

PACKAGE	BOARD TYPE†	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATNG	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PW	JEDEC low-K	114.5°C/W	920 mW	8.7 mW/°C	520 mW	390 mW
	JEDEC high-K	62.1°C/W	1690 mW	16.1 mW/°C	960 mW	720 mW

† JECEC high-K board has better thermal performance due to multiple internal copper planes.
‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).

recommended operating conditions (see Note 5)

		MIN	MAX	UNIT
V_{CC}, AV_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	85	°C

NOTE 5: Unused inputs must be held high or low to prevent them from floating.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{clk}	Clock frequency	50	175	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time†		1	ms

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, AV_{CC}	MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA	3 V			–1.2	V
V_{OH}	High-level output voltage	I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2			V
		I_{OH} = –12 mA	3 V	2.1			
		I_{OH} = –6 mA	3 V	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 100 μA	MIN to MAX			0.2	V
		I_{OL} = 12 mA	3 V			0.8	
		I_{OL} = 6 mA	3 V			0.55	
I_{OH}	High-level output current	V_O = 1 V	3 V	–28			mA
		V_O = 1.65 V	3.3 V		–36		
		V_O = 3.135 V	3.6 V			–8	
I_{OL}	Low-level output current	V_O = 1.95 V	3 V	30			mA
		V_O = 1.65 V	3.3 V		40		
		V_O = 0.4 V	3.6 V			10	
I_I	Input current	$V_I = V_{CC}$ or GND	3.6 V			±5	μA
I_{CC}§	Supply current (static, output not switching)	$V_I = V_{CC}$ or GND, I_O = 0, Outputs: low or high	0 V, 3.6 V			40	μA
ΔI_{CC}	Change in supply current	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	μA
C_i	Input capacitance	$V_I = V_{CC}$ or GND	3.3 V		2.5		pF
C_o	Output capacitance	$V_O = V_{CC}$ or GND	3.3 V		2.8		pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ For dynamic I_{CC} vs Frequency, refer to Figures 8 and 9.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF (see Note 6 and Figures 1 and 2)‡

PARAMETER		FROM (INPUT)/CONDITION	TO (OUTPUT)	V_{CC}, AV_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP	MAX	
	Phase error time – static (normalized) (see Figures 3 – 6)	CLK↑ = 66 MHz to166 MHz	FBIN↑	–125		125	ps
$t_{sk(o)}$	Output skew time§	Any Y	Any Y			100	ps
	Phase error time – jitter (see Note 7)	CLK = 66 MHz to 166 MHz	Any Y or FBOUT	–50		50	ps
	Jitter(cycle-cycle) (see Figure 7)		Any Y or FBOUT		|70|		
		CLK = 100 MHz to 166 MHz	Any Y or FBOUT		|65|		
	Duty cycle	$f_{(CLK)}$ > 60 MHz	Any Y or FBOUT	45%		55%	
t_r	Rise time	V_O = 0.4 V to 2 V	Any Y or FBOUT	0.5		2.5	ns/V
t_f	Fall time	V_O = 0.4 V to 2 V	Any Y or FBOUT	0.5		2.5	ns/V
$t_{PLH(bypass mode)}$	Low-to-high propagation delay time, bypass mode	CLK	Any Y or FBOUT	0.4		2.3	ns
$t_{PHL(bypass mode)}$	High-to-low propagation delay time, bypass mode	CLK	Any Y or FBOUT	0.4		2.3	ns

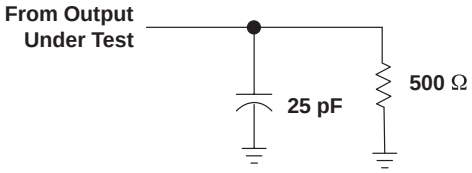
‡ These parameters are not production tested.

§ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

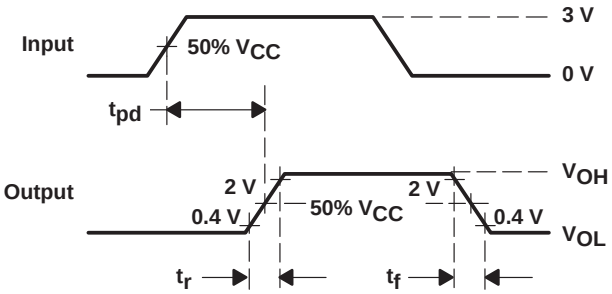
NOTES: 6. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

7. Calculated per PC DRAM SPEC ($t_{phase\ error}$, static – $jitter_{(cycle\text{-}to\text{-}cycle)}$).

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 133 MHz, Z_O = 50 Ω, t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

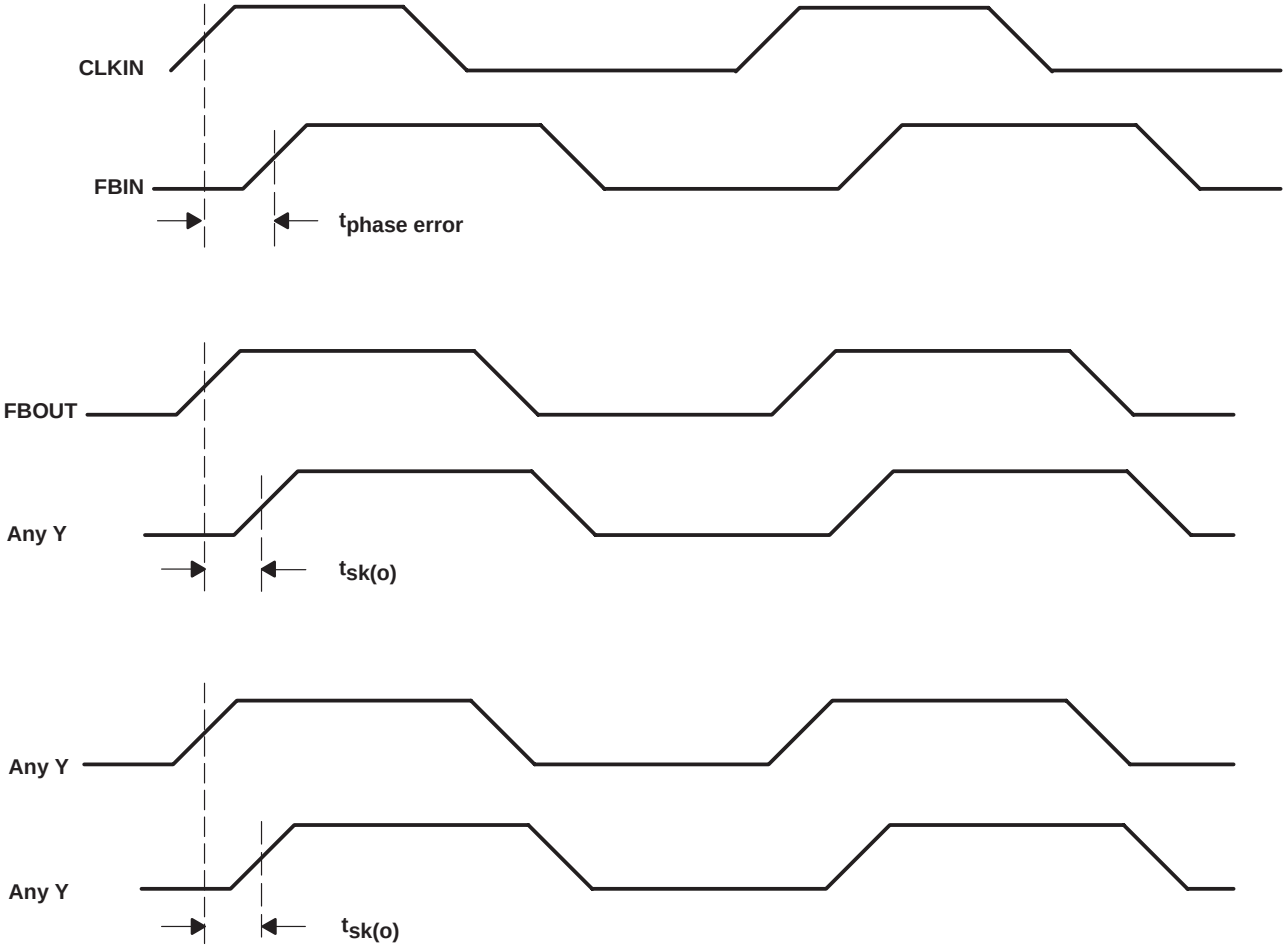


Figure 2. Phase Error and Skew Calculations

TYPICAL CHARACTERISTICS

STATIC PHASE ERROR vs LOAD CAPACITANCE

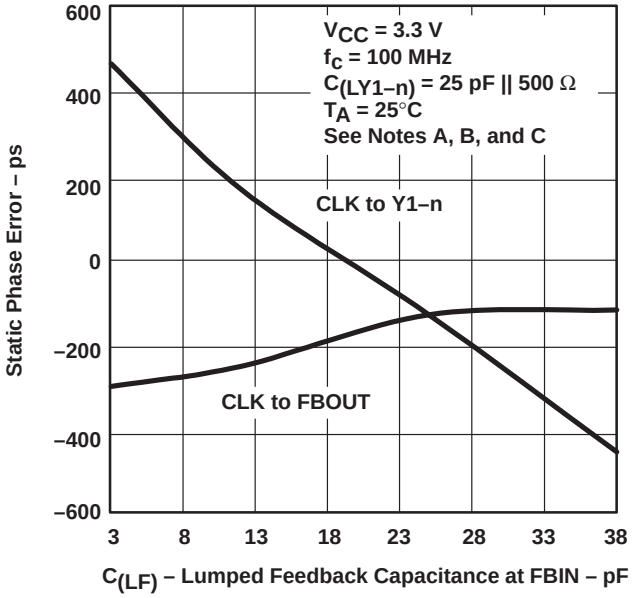


Figure 3

STATIC PHASE ERROR vs LOAD CAPACITANCE

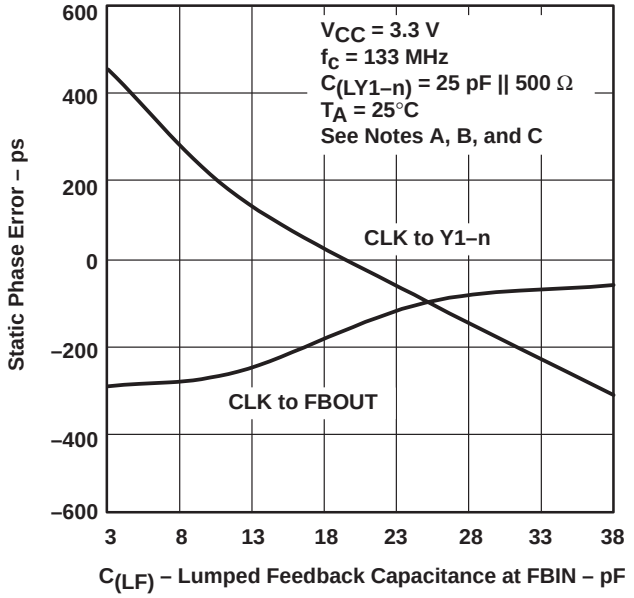


Figure 4

STATIC PHASE ERROR vs SUPPLY VOLTAGE AT FBOUT

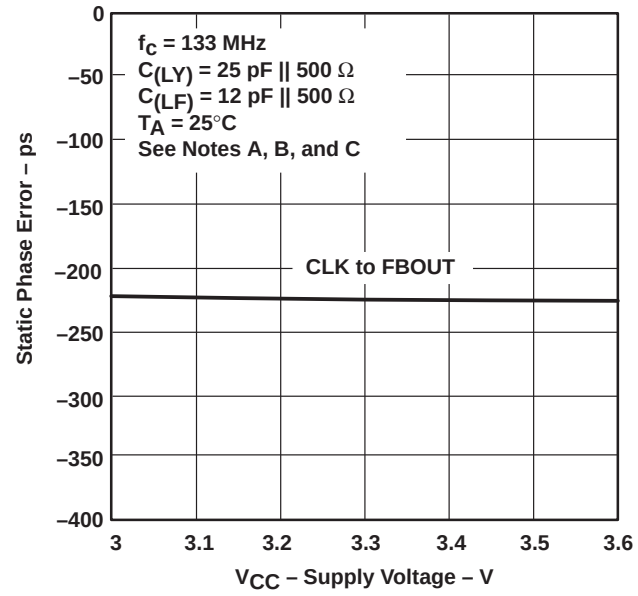


Figure 5

STATIC PHASE ERROR vs CLOCK FREQUENCY

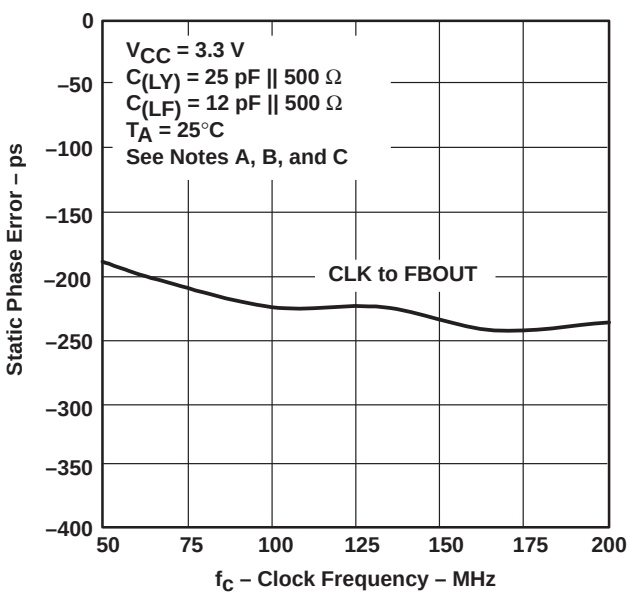


Figure 6

NOTES: A. Trace length FBOUT to FBIN = 5 mm, Z_O = 50 Ω
B. $C_{(LY)}$ = Lumped capacitive load $Y_{1–n}$
C. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN

TYPICAL CHARACTERISTICS

JITTER vs CLOCK FREQUENCY AT FBOUT

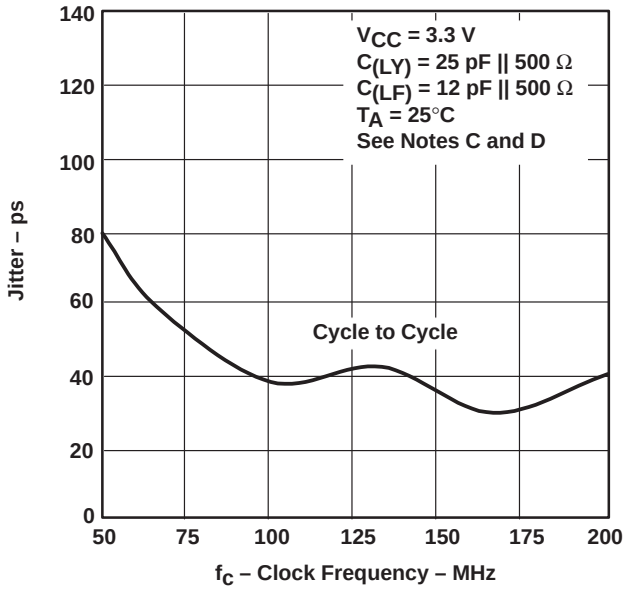


Figure 7

ANALOG SUPPLY CURRENT vs CLOCK FREQUENCY

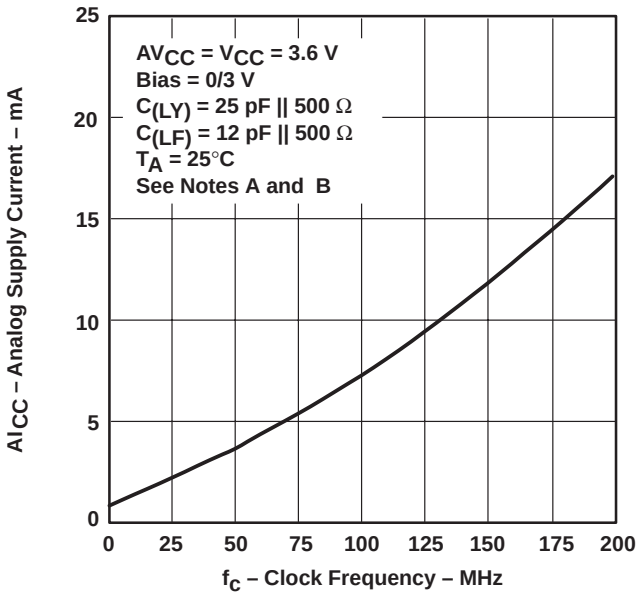


Figure 8

SUPPLY CURRENT vs CLOCK FREQUENCY

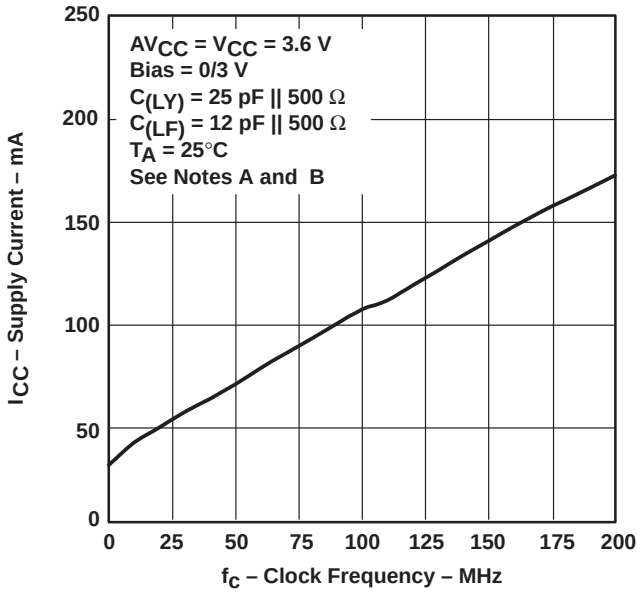


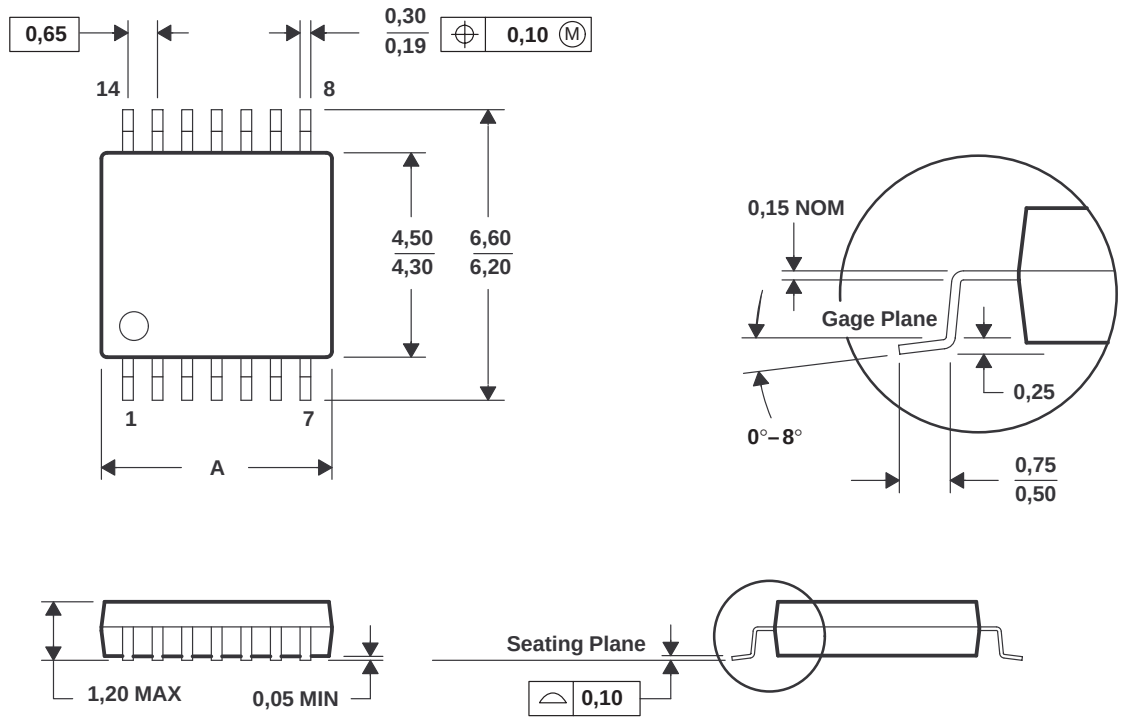
Figure 9

NOTES: A. Trace length FBOUT to FBIN = 5 mm, Z_O = 50 Ω
B. Total current = I_{CC} + AI_{CC}
C. $C_{(LY)}$ = Lumped capacitive load $Y_{1–n}$
D. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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