BENCHMARQ

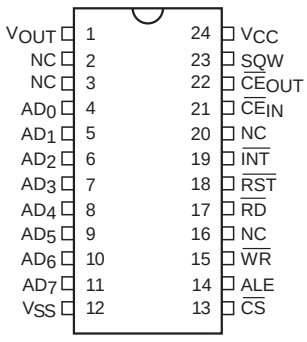
bq4287

Real-Time Clock Module With NVRAM Control

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1287/DS1287A and MC146818A
- 114 bytes of general nonvolatile storage
- Automatic backup supply and write-protection to make external SRAM nonvolatile
- Integral lithium cell and crystal
- 160 ns cycle time allows fast bus operation
- Intel bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

Pin Connections



24-Pin DIP Module

PN428701.eps

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
$\overline{CS}$	Chip select input
ALE	Address strobe input
$\overline{RD}$	Data strobe input
$\overline{WR}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
NC	No connect
V_{OUT}	Supply output
V_{CC}	+5V supply
V_{SS}	Ground

General Description

The CMOS bq4287 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

The bq4287 write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

The bq4287 uses its integral battery-backup controller and battery to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4287 automatically write-protects the external SRAM and provides a V_{CC} output sourced from its internal battery.

The bq4287 is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of V_{CC}, this isolation is broken, and the backup cell provides data retention to the clock, internal RAM, V_{OUT}, and $\overline{CE}_{OUT}$ on subsequent power-downs.

The bq4287 is functionally equivalent to the bq4285, except that the battery (16, 20) and crystal pins (2, 3) are not accessible. These pins are connected internally to a coin cell and quartz crystal. The coin cell provides 130mAh of capacity. For a complete description of features, operating conditions, electrical characteristics, bus timing, and pin descriptions, see the bq4285 data sheet.

Caution:

Take care to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

Nov. 1993 C

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity	-	130	-	mAh	Refer to graphs in Typical Battery Characteristics section
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{SO}	Supply switch-over voltage	-	3.0	-	V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{BC}	Backup cell voltage	-	3.0	-	V	Internal backup cell voltage; refer to graphs in Typical Battery Characteristics section
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V	-	-	V	I_{OUT} = 100µA, $V_{CC} < V_{BC}$
$I_{\overline{CE}}$	Chip enable input current	-	-	100	µA	Internal 50K pull-up

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

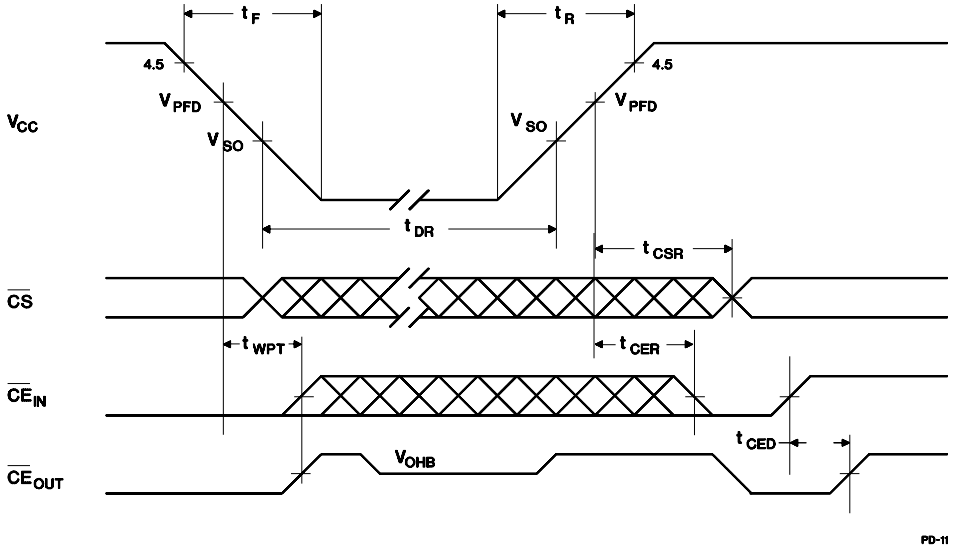
Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and time-keeping time	10	-	-	years	T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slows down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	7	10	ns	

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

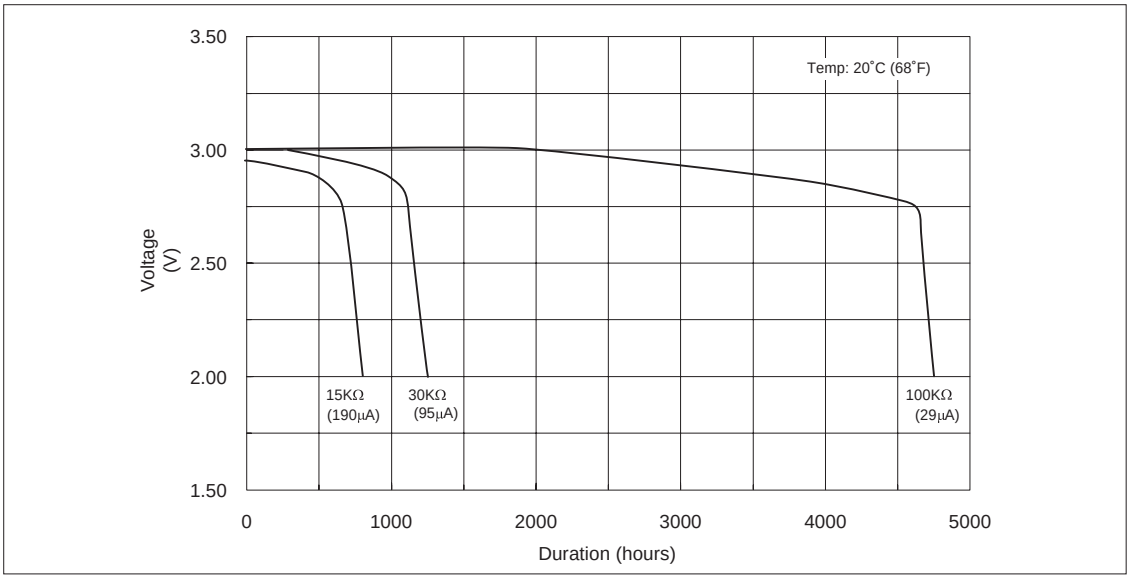
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing

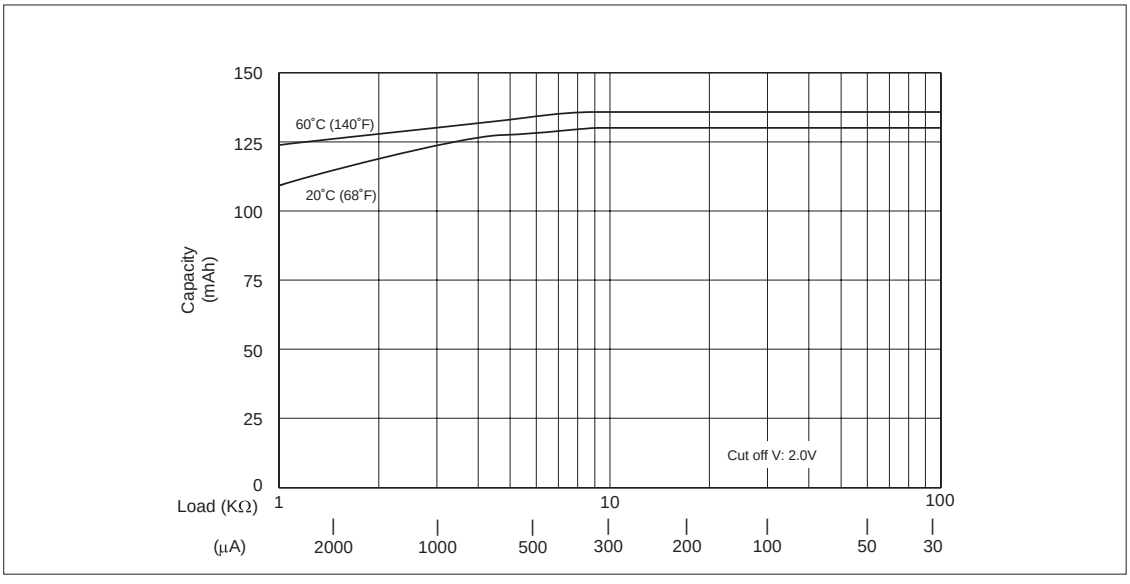


Typical Battery Characteristics (source = Panasonic)

CR1632 Load Characteristics

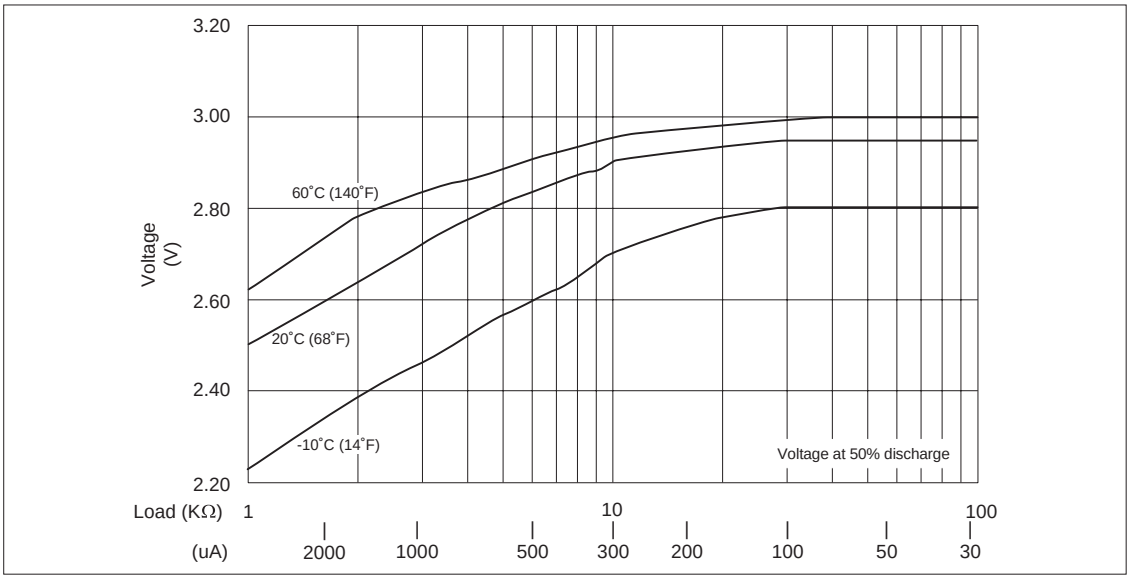


CR1632 Capacity vs. Load Resistance

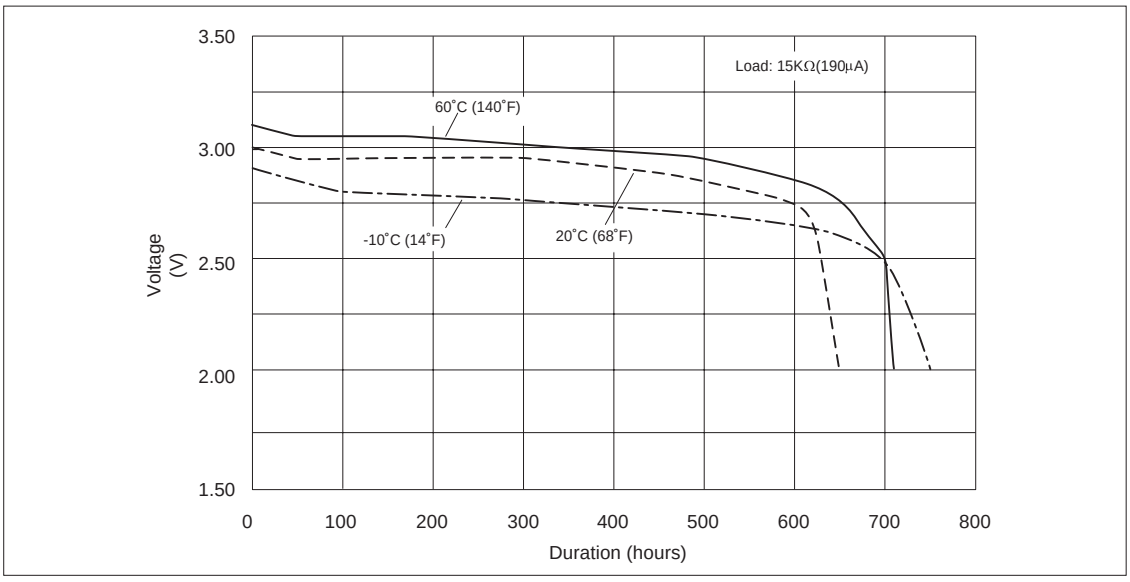


Nov. 1993 C

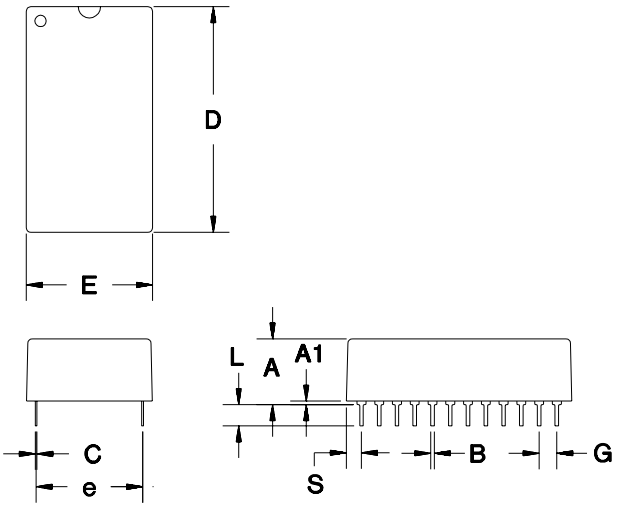
CR1632 Operating Voltage vs. Load Resistance



CR1632 Temperature Characteristics



24-Pin MT (T-type module)



24-Pin MT (T-type module)

Dimension	Minimum	Maximum
A	0.360	0.375
A1	0.015	-
B	0.015	0.022
C	0.008	0.013
D	1.320	1.335
E	0.685	0.700
e	0.590	0.620
G	0.090	0.110
L	0.120	0.130
S	0.100	0.120

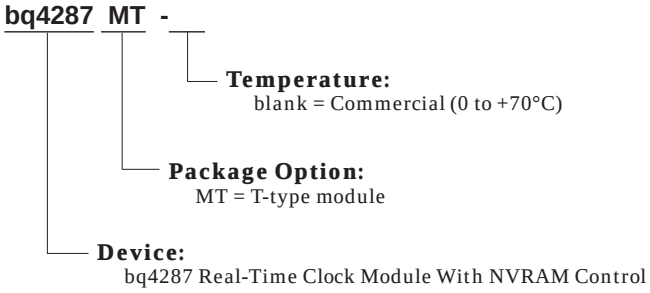
All dimensions are in inches.

Data Sheet Revision History

Change	Page No.	Description	Nature of Change
1	2	Power-fail detect voltage VPFD	Was 4.1 min, 4.25 max; is 4.0 min, 4.35 max
1	2	Chip enable input current	Additional specification
2	9	Was: "As shipped from Benchmarq, the backup cell is electrically isolated from the memory." Is: "As shipped from Benchmarq, the backup cell is electrically isolated from the active circuitry."	Clarification
2	14	Deleted specifications for t_{RWH} and t_{RWS}	Clarification; these parameters are not supported by the bq4287

Notes: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.

Ordering Information



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.