

# SN74CBTD16210 20-BIT FET BUS SWITCH WITH LEVEL SHIFTING

SCDS049C – MARCH 1998 – REVISED MAY 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

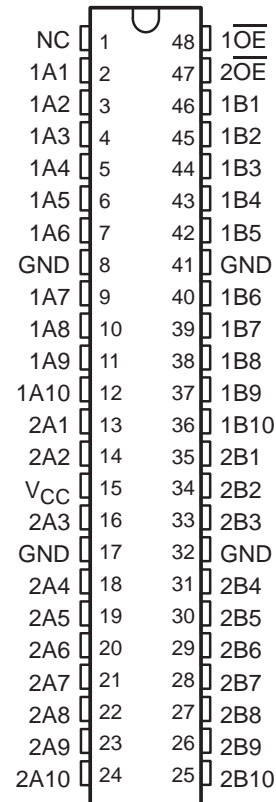
## description

The SN74CBTD16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to  $V_{CC}$  is integrated in the circuit to allow for level shifting between 5-V inputs and 3.3-V outputs.

The device is organized as a dual 10-bit bus switch with separate output-enable ( $\overline{OE}$ ) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When  $\overline{OE}$  is low, the associated 10-bit bus switch is on and A port is connected to B port. When  $\overline{OE}$  is high, the switch is open, and a high-impedance state exists between the ports.

The SN74CBTD16210 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

**FUNCTION TABLE**  
(each 10-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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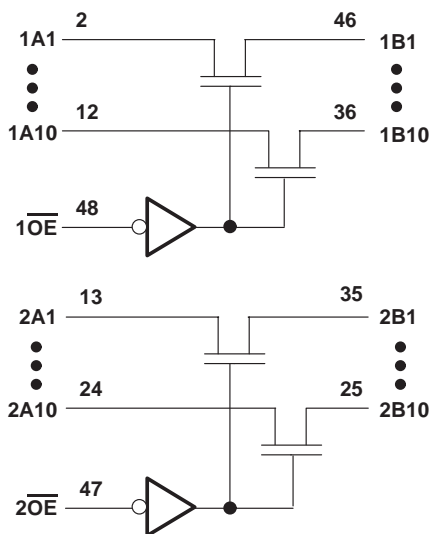
# SN74CBTD16210

## 20-BIT FET BUS SWITCH

### WITH LEVEL SHIFTING

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Continuous channel current	.....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DGG package	89°C/W
	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level control input voltage	2		V
$V_{IL}$	Low-level control input voltage		0.8	V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT			
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				-1.2	V			
$V_{OH}$		See Figure 2								
$I_I$		$V_{CC} = 0\text{ V}$ , $V_I = 5.5\text{ V}$				10	$\mu\text{A}$			
		$V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V or GND}$				$\pm 1$				
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$				1.5	mA			
$\Delta I_{CC}^\ddagger$	Control inputs	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND				2.5	mA			
$C_i$	Control inputs	$V_I = 3\text{ V or 0}$				4.5	pF			
$C_{io(OFF)}$		$V_O = 3\text{ V or 0}$ , $\overline{OE} = V_{CC}$				5.5	pF			
$r_{on}^\S$		$V_{CC} = 4.5\text{ V}$		$V_I = 0$		$I_I = 64\text{ mA}$		5	7	$\Omega$
						$I_I = 30\text{ mA}$		5	7	
				$V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$		35	50			

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^\parallel$	A or B	B or A		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	1.5	9.8	ns
$t_{dis}$	$\overline{OE}$	A or B	1.5	8.9	ns

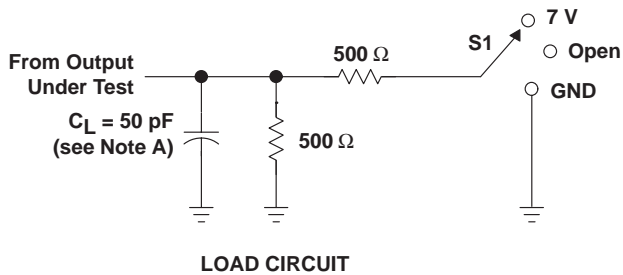
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



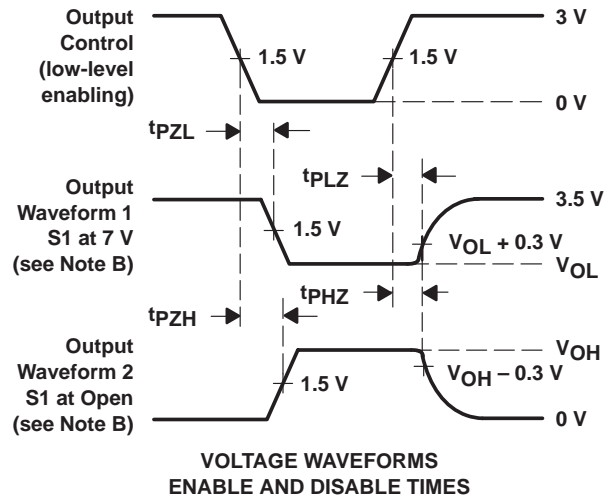
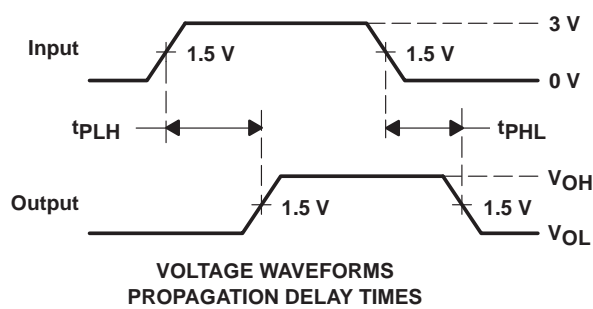
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**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

TYPICAL CHARACTERISTICS

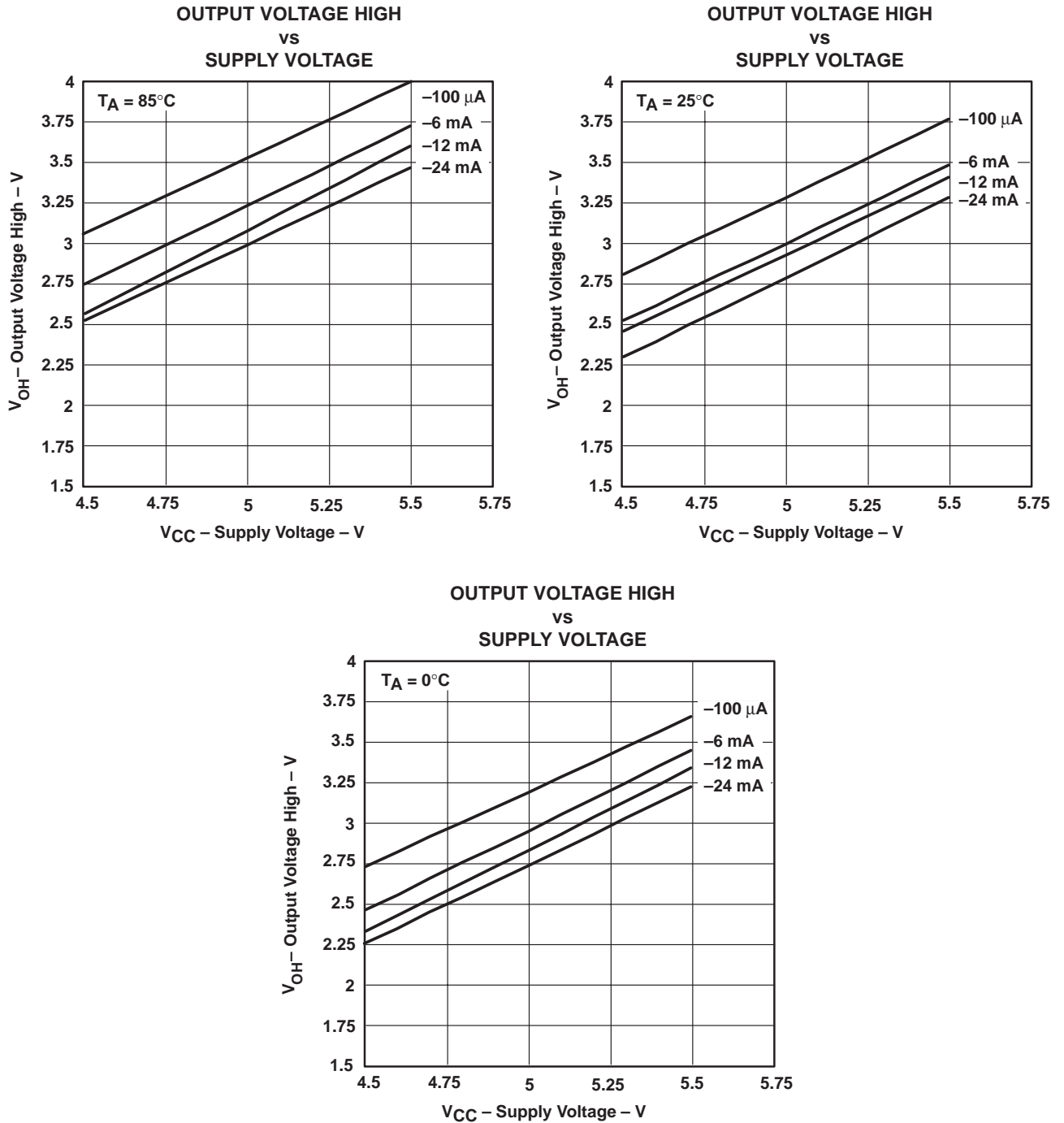


Figure 2.  $V_{OH}$  Values

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