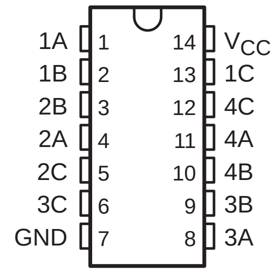
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, and Standard Plastic (N) and Ceramic (J) DIPs**

SN54LV4066A . . . J OR W PACKAGE
SN74LV4066A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



description

This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V V_{CC} operation.

These switches are designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

The SN54LV4066A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV4066A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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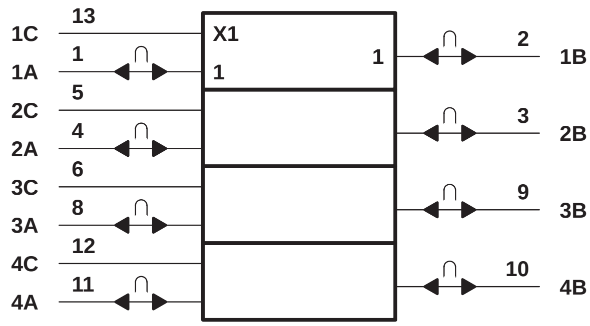
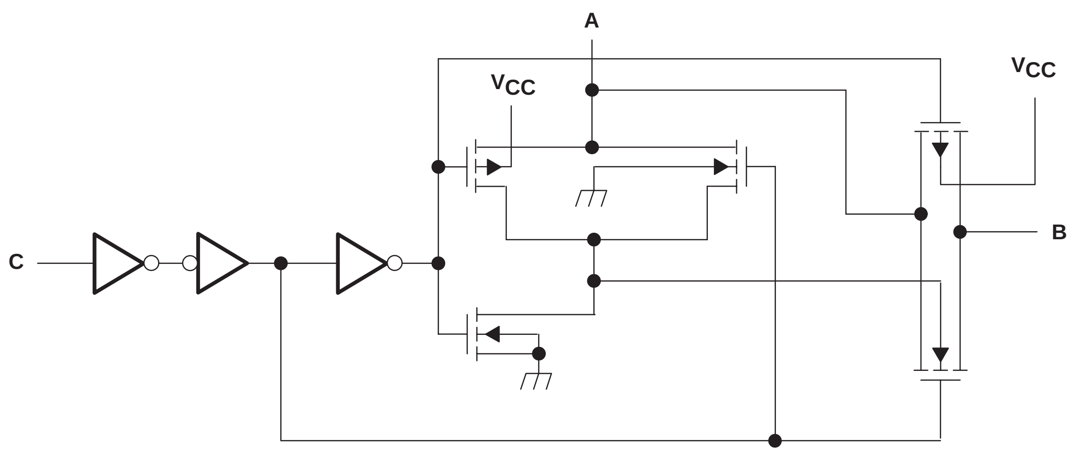
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



One of Four Switches

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Switch I/O voltage range, V_{IO} (see Note 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V
Control-input clamp current, I_{IK} (V_I < 0) . . . . –20 mA
I/O diode current, I_{IOK} (V_{IO} < 0 or V_{IO} > V_{CC}) . . . . ±50 mA
On-state switch current, I_T (V_{IO} = 0 to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . 127°C/W
DB package . . . . 158°C/W
DGV package . . . . 182°C/W
N package . . . . 78°C/W
NS package . . . . 127°C/W
PW package . . . . 170°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 4)

			SN54LV4066A		SN74LV4066A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	0	V_{CC}	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
R_{on}	On-state switch resistance	I_T = –1 mA, $V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 1)	2.3 V		38	180		225		225	Ω
			3 V		29	150		190		190	
			4.5 V		21	75		100		100	
$R_{on(p)}$	Peak on-state resistance	I_T = –1 mA, $V_I = V_{CC}$ to GND, $V_C = V_{IH}$	2.3 V		143	500		600		600	Ω
			3 V		57	180		225		225	
			4.5 V		31	100		125		125	
ΔR_{on}	Difference in on-state resistance between switches	I_T = –1 mA, $V_I = V_{CC}$ to GND, $V_C = V_{IH}$	2.3 V		6	30		40		40	Ω
			3 V		3	20		30		30	
			4.5 V		2	15		20		20	
I_I	Control input current	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{soff}	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 2)	5.5V			±0.1		±1		±1	µA
I_{son}	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 3)	5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5 V					20		20	µA
C_{ic}	Control input capacitance				1.5						pF
C_{io}	Switch input/output capacitance				5.5						pF
C_f	Feedthrough capacitance				0.5						pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		1.2	10		16		16	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		3.3	15		20		20	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		6	15		23		23	ns
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		2.6	12		18		18	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		4.2	25		32		32	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		9.6	25		32		32	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		0.8	6		10		10	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		2.3	11		15		15	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		4.5	11		15		15	ns
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		1.5	9		12		12	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		3	18		22		22	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		7.2	18		22		22	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		0.3	4		7		7	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		1.6	7		10		10	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		3.2	7		10		10	ns
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		0.6	6		8		8	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		2.1	12		16		16	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		5.1	12		16		16	ns

PRODUCT PREVIEW

analog switch characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C			UNIT
						MIN	TYP	MAX	
Frequency response (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) $20\log_{10}(V_O/V_I)$ = –3 dB (see Figure 6)		2.3 V		30		MHz
					3 V		35		
					4.5 V		50		
Crosstalk (between any switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)		2.3 V		–45		dB
					3 V		–45		
					4.5 V		–45		
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		15		mV
					3 V		20		
					4.5 V		50		
Feedthrough attenuation (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see Figure 9)		2.3 V		–40		dB
					3 V		–40		
					4.5 V		–40		
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 V_{p-p}	2.3 V		0.1		
				V_I = 2.5 V_{p-p}	3 V		0.1		
				V_I = 4 V_{p-p}	4.5 V		0.1		

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance		4.5	pF

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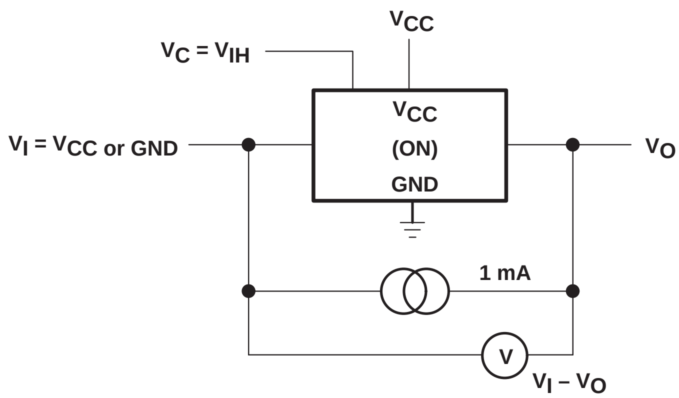
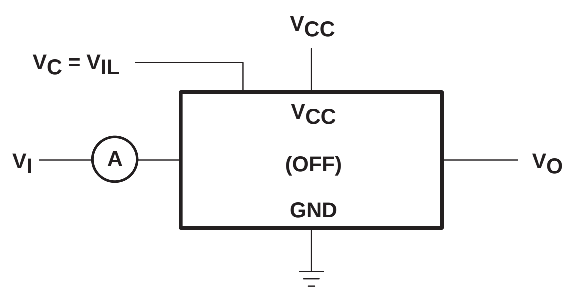
PARAMETER MEASUREMENT INFORMATION



$$R_{ON} = \frac{V_I - V_O}{10^{-3}}\ \Omega$$

Figure 1. On-State Resistance Test Circuit



Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

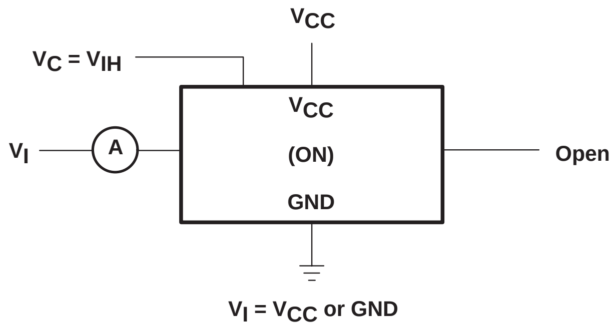


Figure 3. On-State Leakage-Current Test Circuit

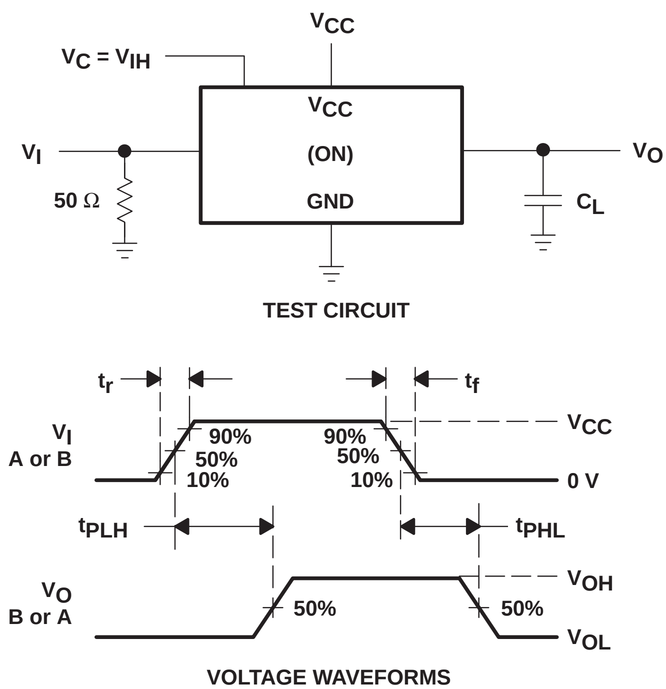
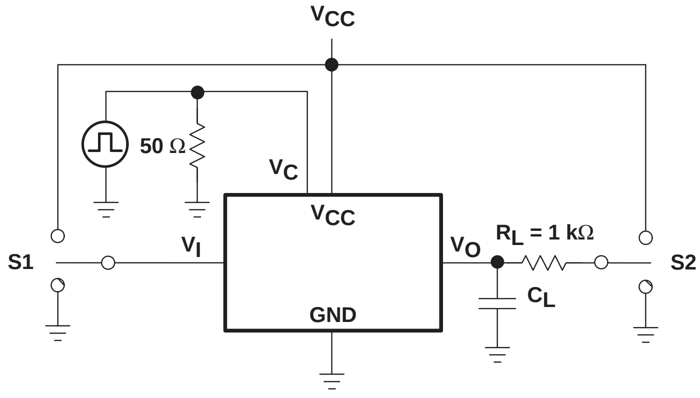


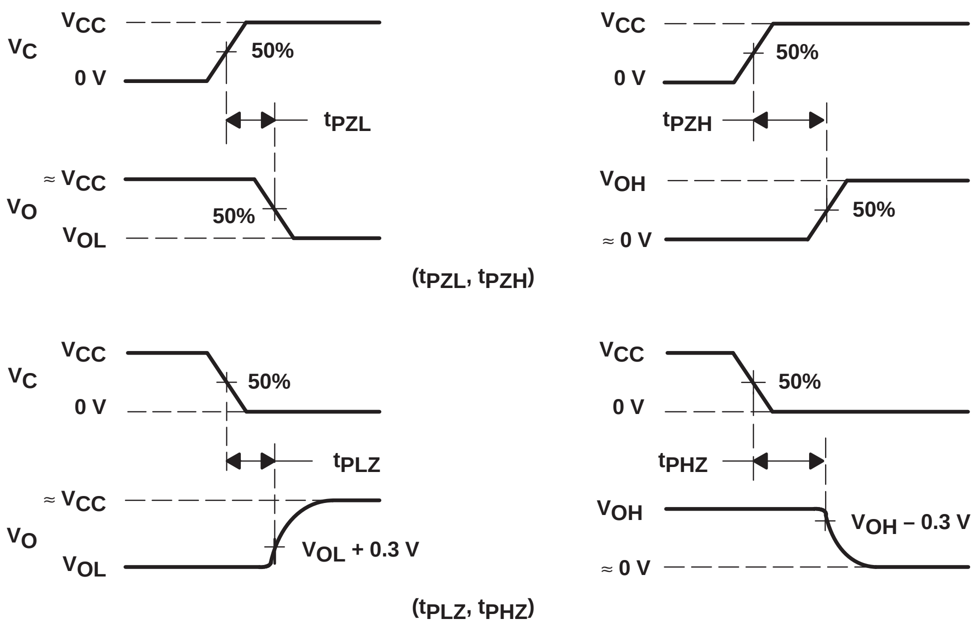
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION

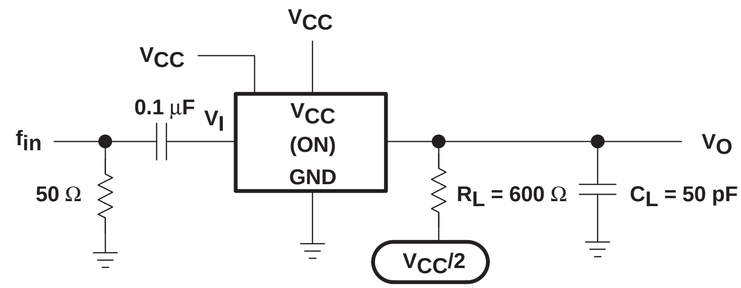


Figure 6. Frequency Response (Switch On)

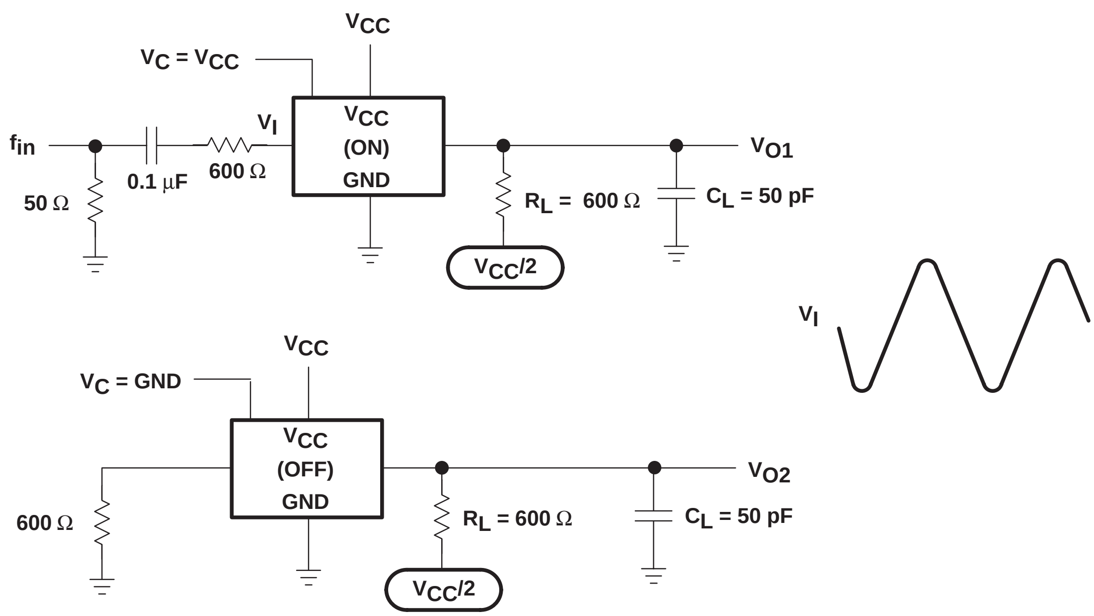


Figure 7. Crosstalk Between Any Two Switches

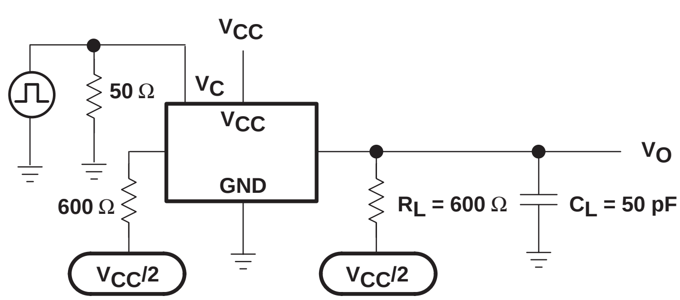


Figure 8. Crosstalk (Control Input – Switch Output)

PARAMETER MEASUREMENT INFORMATION

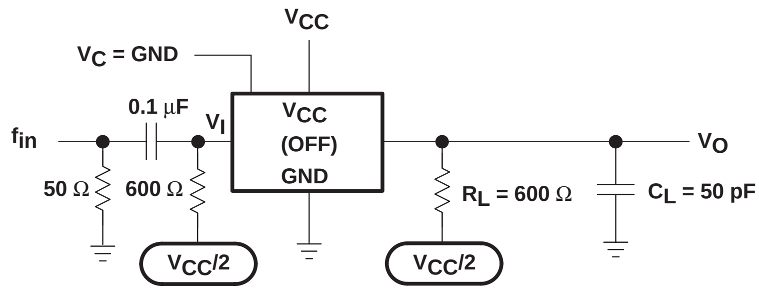


Figure 9. Feedthrough Attenuation (Switch Off)

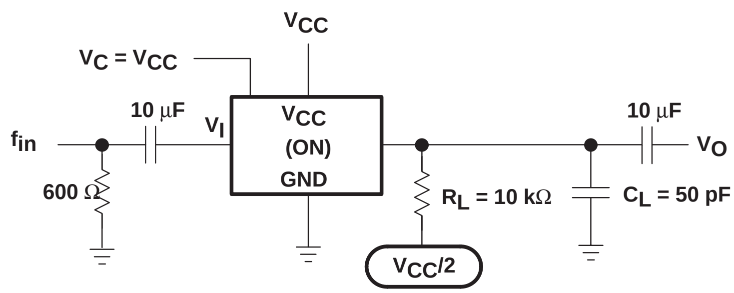


Figure 10. Sine-Wave Distortion

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