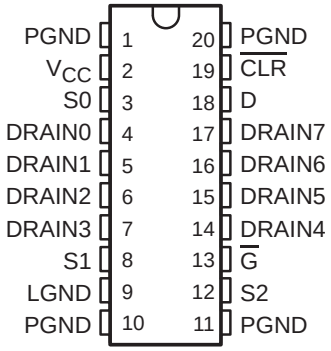
SLIS009A – APIRL 1992 – REVISED SEPTEMBER 1995

- **Low $r_{DS(on)}$ . . . 1.3 Ω Typical**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage at 45 V**
- **Four Distinct Function Modes**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



description

This power logic 8-bit addressable latch controls open-drain DMOS transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of storing single-line data in eight addressable latches with 3-to-8 decoding or demultiplexing mode active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 9, logic ground (LGND), and pins 1, 10, 11, and 20, power ground (PGND) must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6259 is characterized for operation over the operating case temperature range of –40°C to 125°C.

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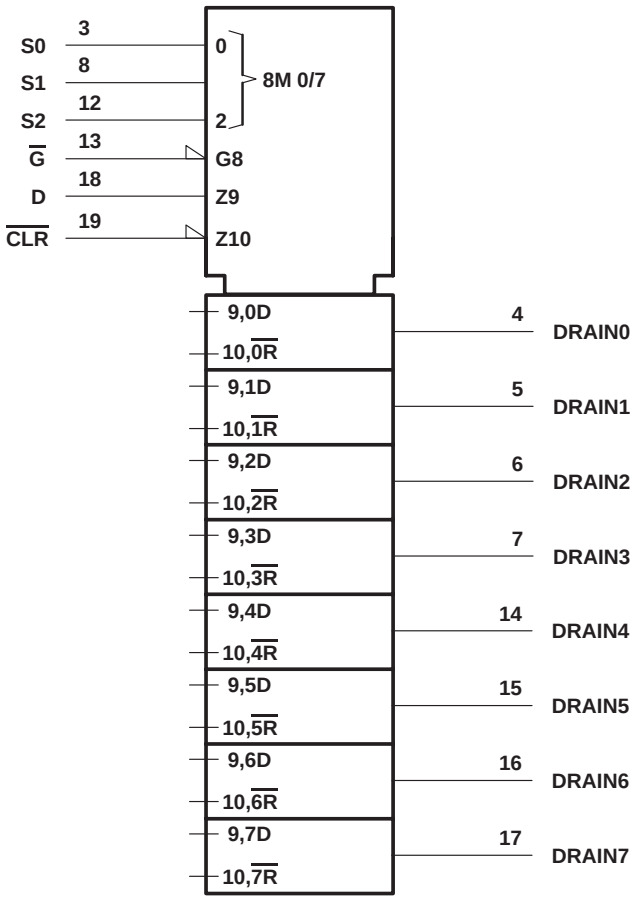
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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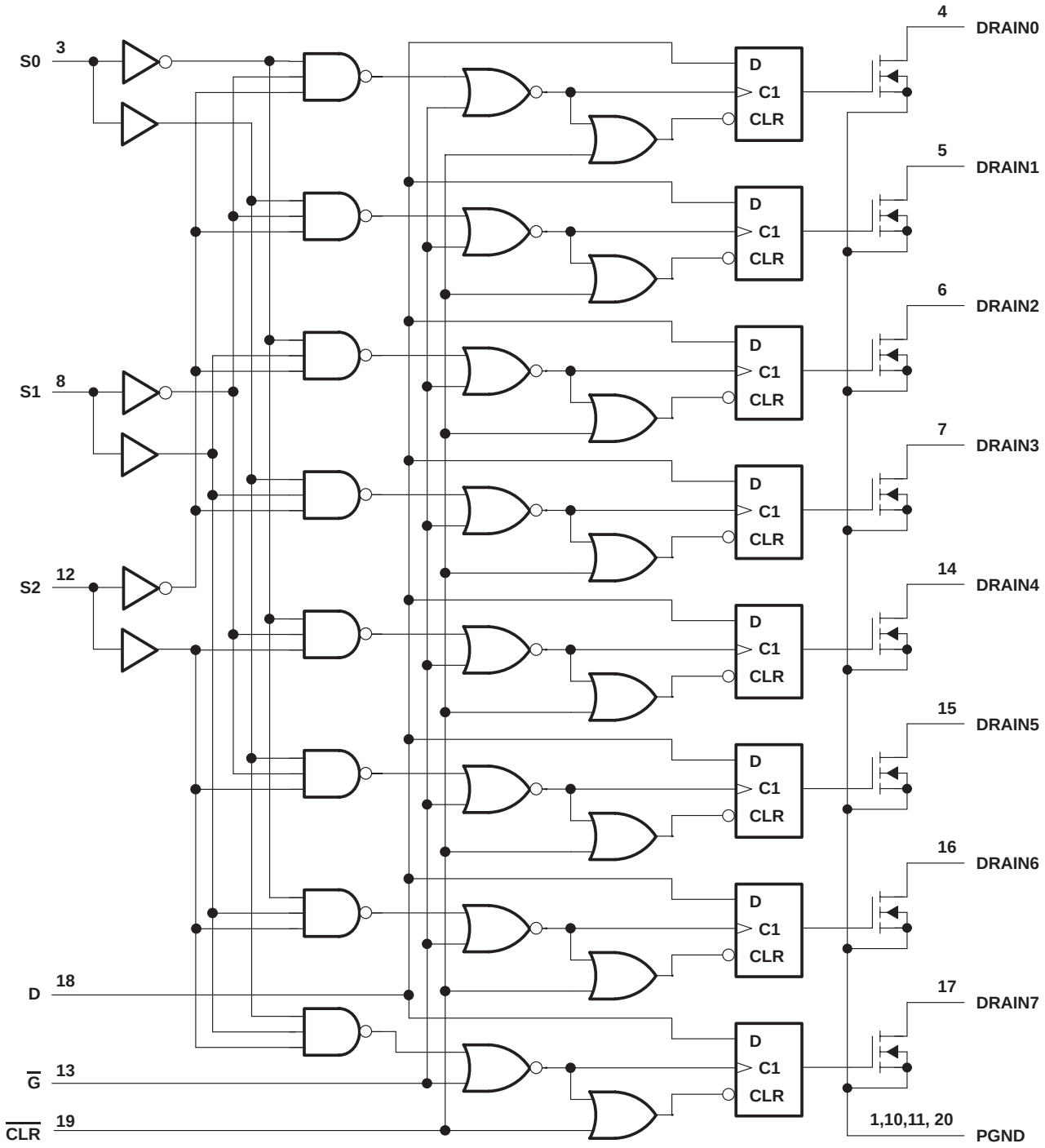
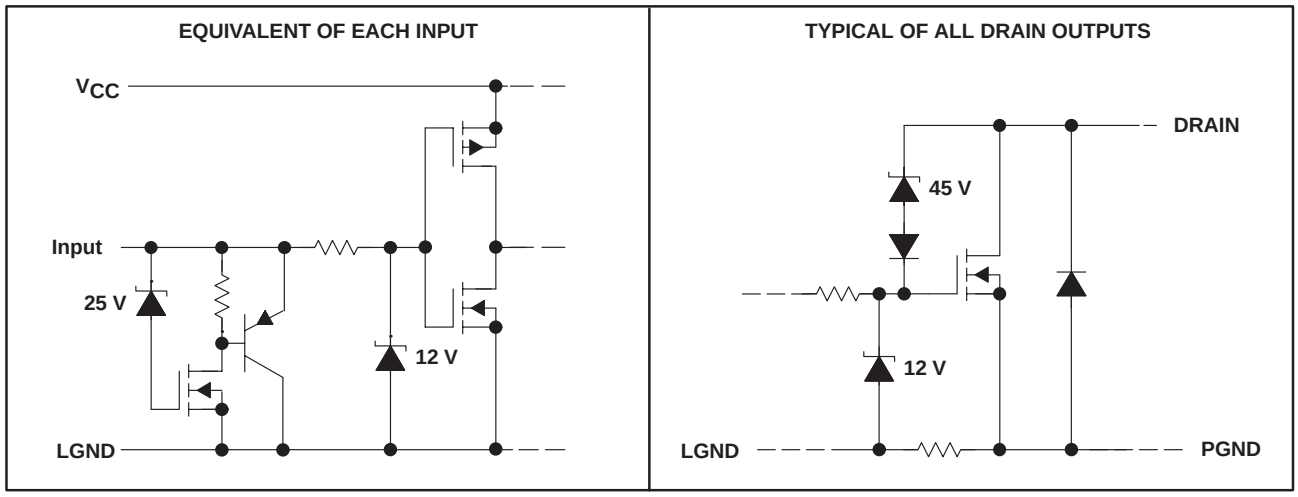
logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Note 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%
4. DRAIN supply voltage = 15 V, starting junction temperature, (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

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recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–1.8	1.5	A
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high after $\overline{G}\uparrow$, t_h (see Figure 2)	5		ns
Pulse duration, t_w (see Figure 2)	15		ns
Operating case temperature, T_C	–40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				–1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C, See Notes 5, 6, and 7			250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 8 and 9		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from D	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 10		625		ns
t_{PHL}	Propagation delay time, high-to-low-level output from D			140		ns
t_r	Rise time, drain output			650		ns
t_f	Fall time, drain output			400		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit T_J – T_C to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

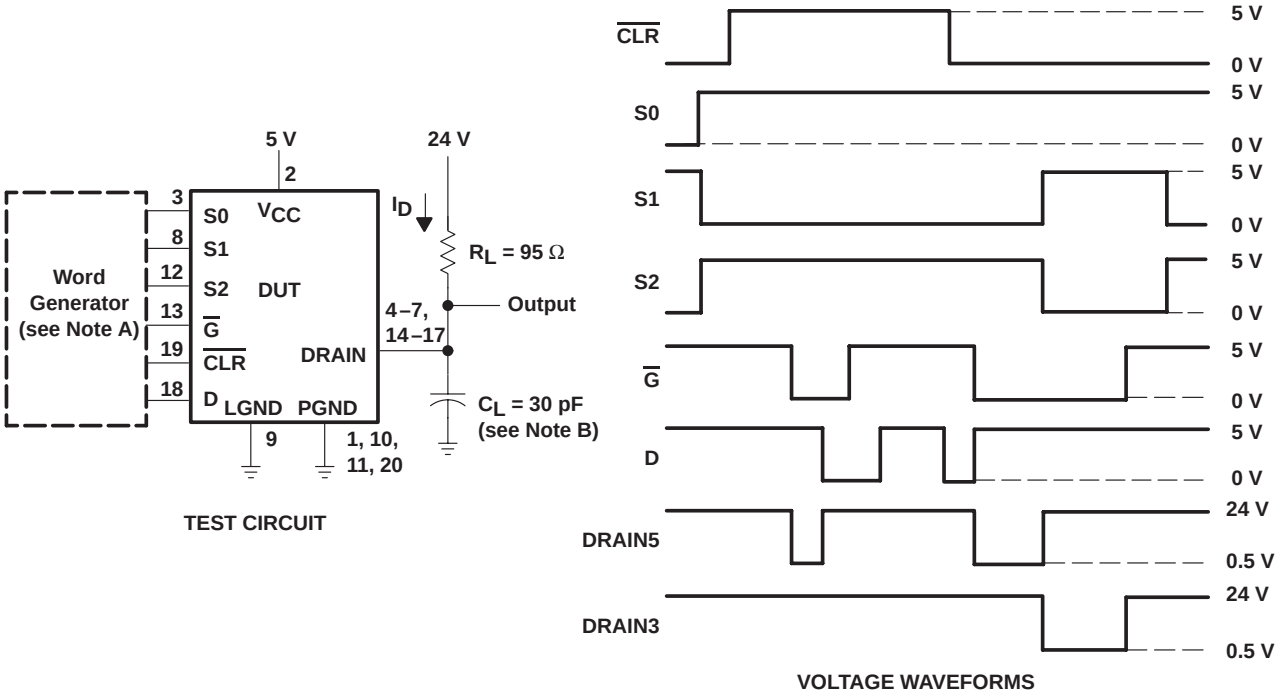

Figure 1. Typical Operation Mode

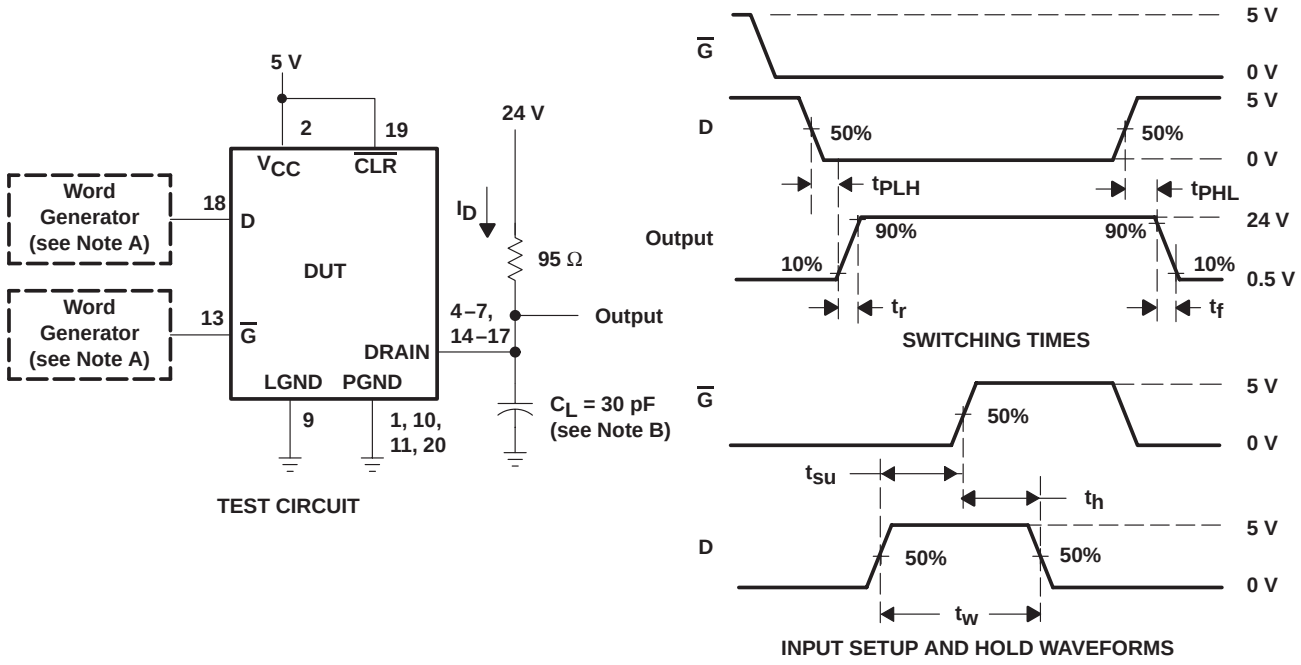

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

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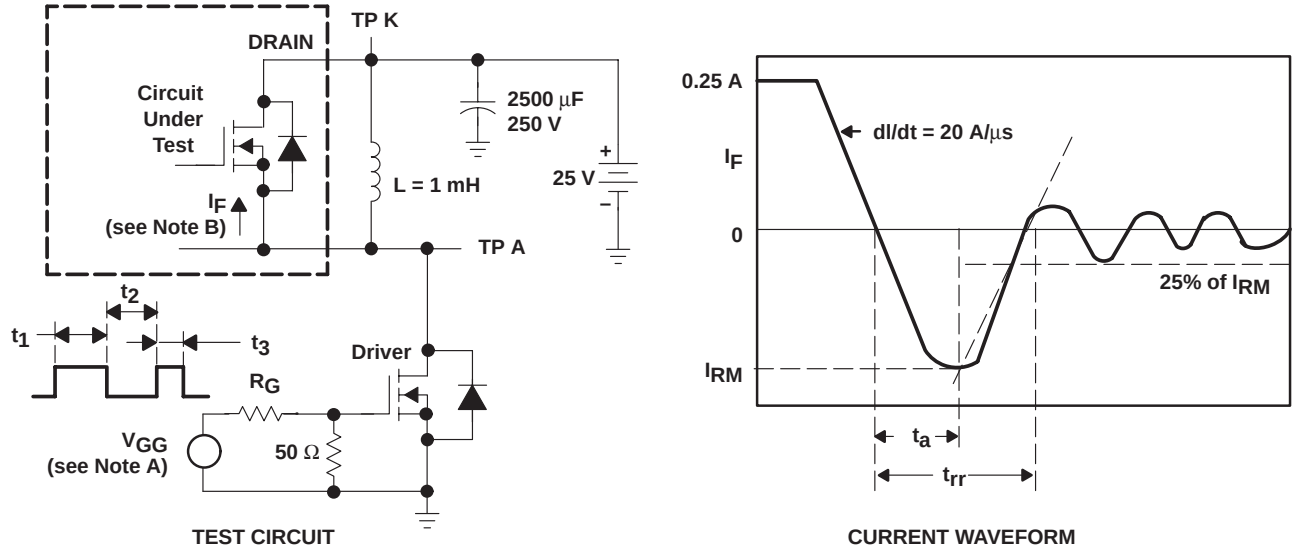
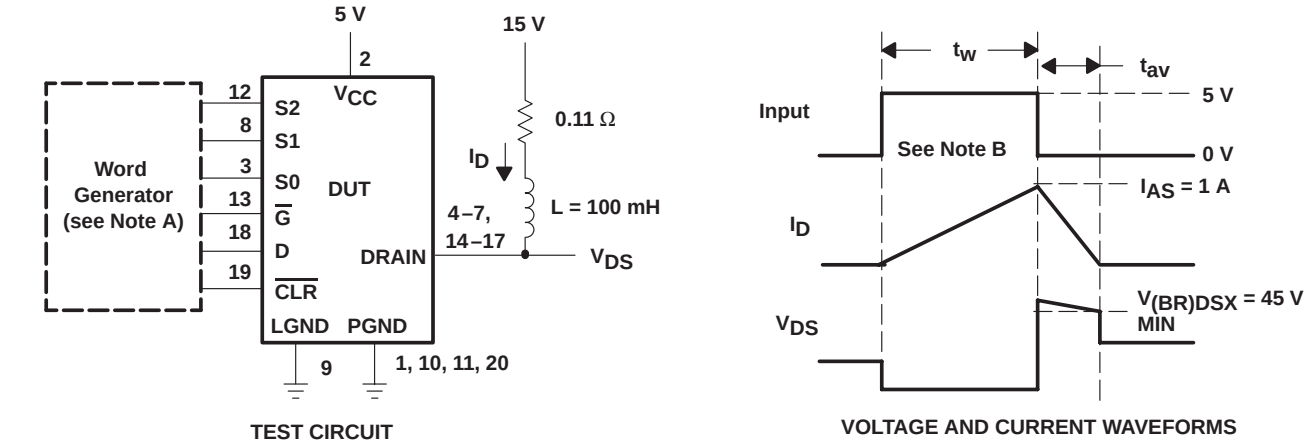
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

**PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

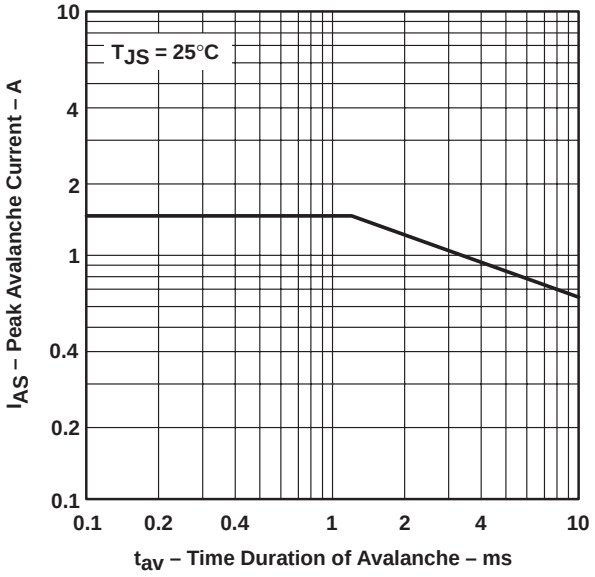


Figure 5

**MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY**

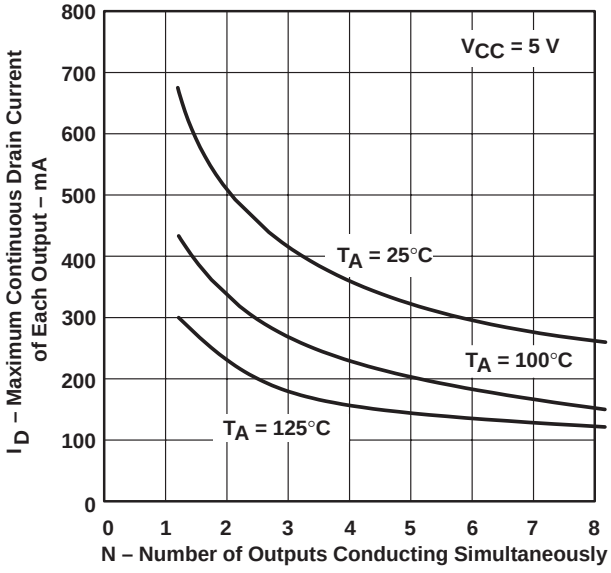


Figure 6

**MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY**

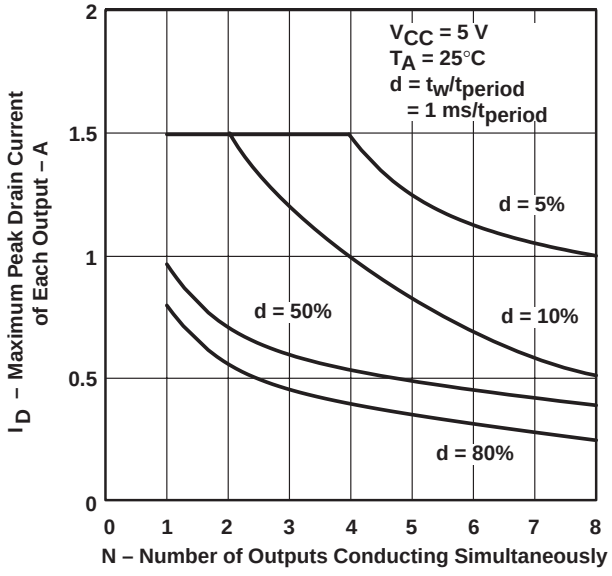


Figure 7

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TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

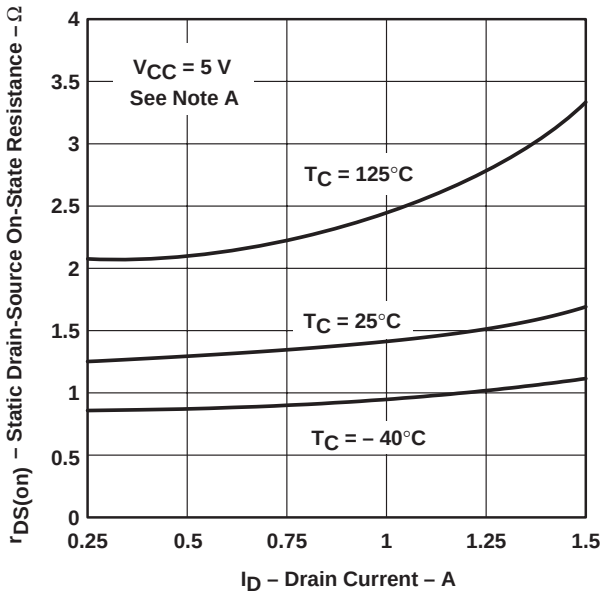

Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

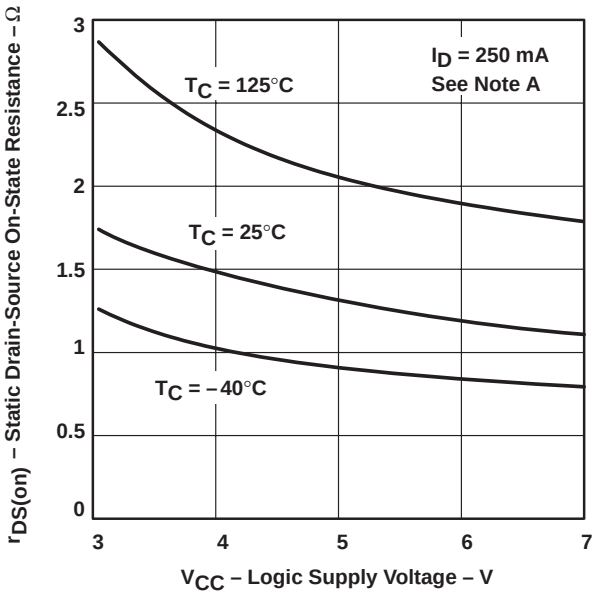

Figure 9

SWITCHING TIME vs FREE-AIR TEMPERATURE

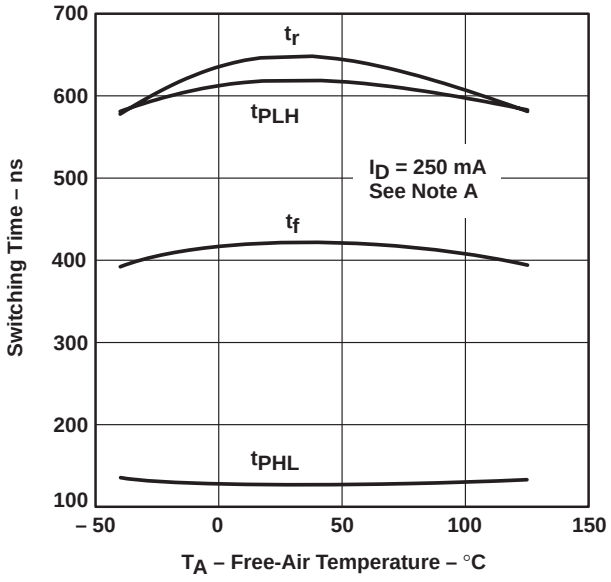

Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

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