

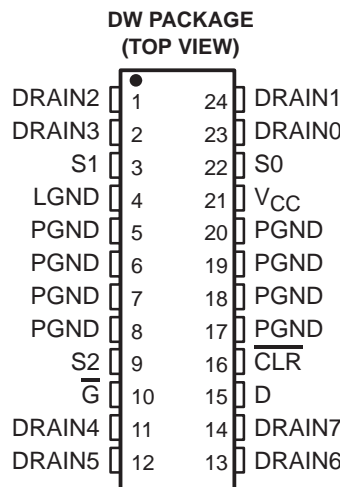
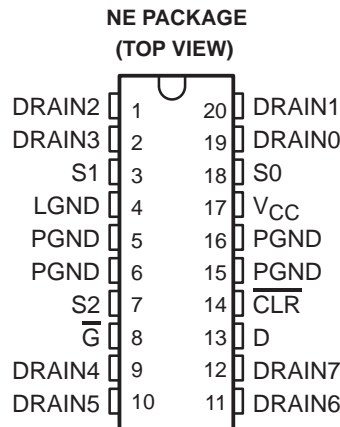
- Low $r_{DS(on)}$. . . 1 Ω Typ
- Output Short-Circuit Protection
- Avalanche Energy . . . 75 mJ
- Eight 350-mA DMOS Outputs
- 50-V Switching Capability
- Four Distinct Function Modes
- Low Power Consumption

description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multi-functional device capable of operating as eight addressable latches or an 8-line demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

Four distinct modes of operation are selectable by controlling the clear (\overline{CLR}) and enable (\overline{G}) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable \overline{G} should be held high (inactive) while the address lines are changing. In the 8-line demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.



FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
\overline{CLR}	\overline{G}	D			
H	L	H	L	Q_{i0}	Addressable Latch
H	L	L	H	Q_{i0}	Addressable Latch
H	H	X	Q_{i0}	Q_{i0}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	8-Line Demultiplexer
L	H	X	H	H	Clear

LATCH SELECTION TABLE

SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

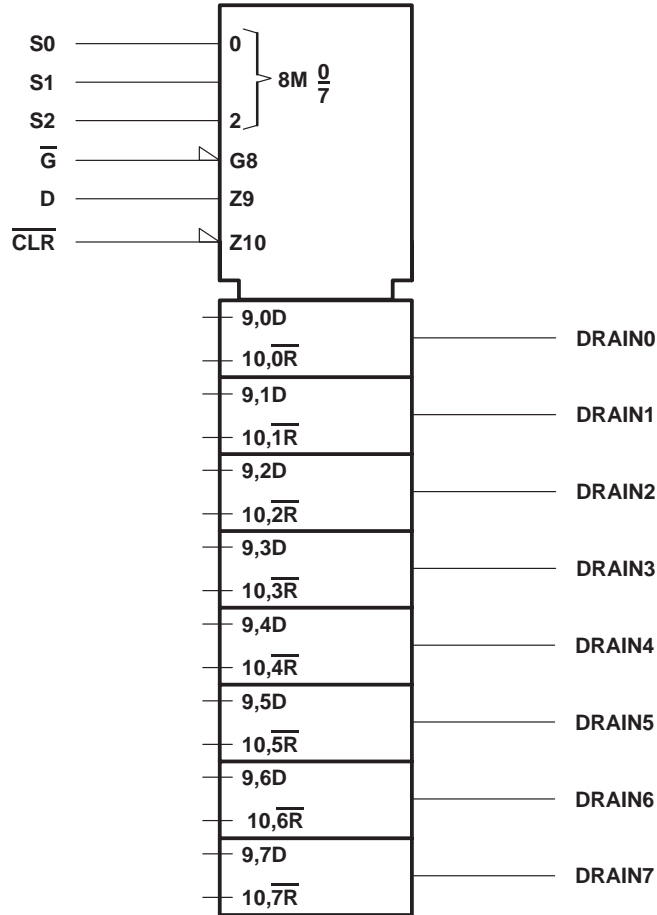
TPIC6A259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS004B – APRIL 1993 – REVISED SEPTEMBER 1995

description (continued)

The TPIC6A259 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body, surface-mount (DW) package. The TPIC6A259 is characterized for operation over the operating case temperature range of -40°C to 125°C .

logic symbol†

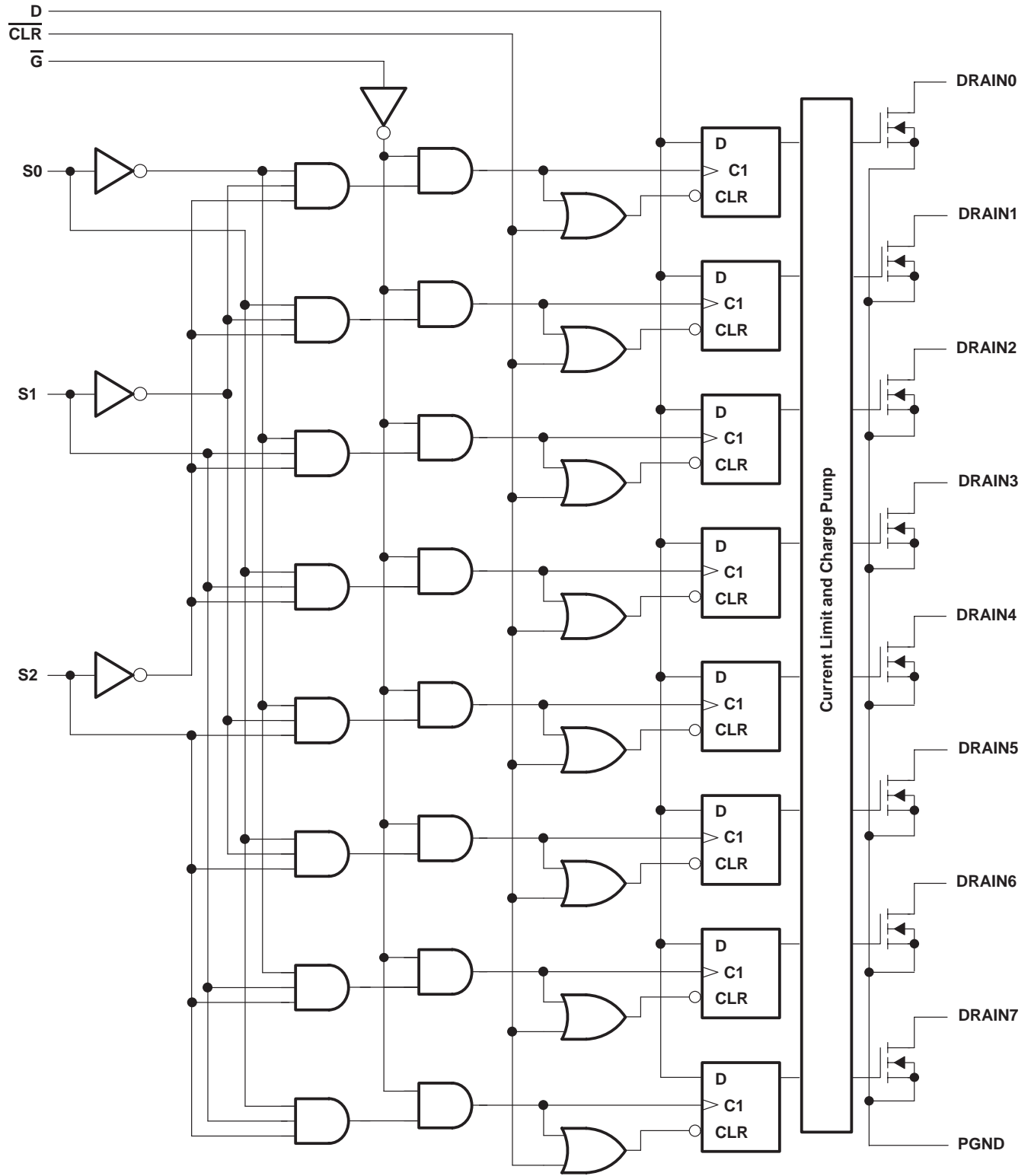


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TPIC6A259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS004B – APRIL 1993 – REVISED SEPTEMBER 1995

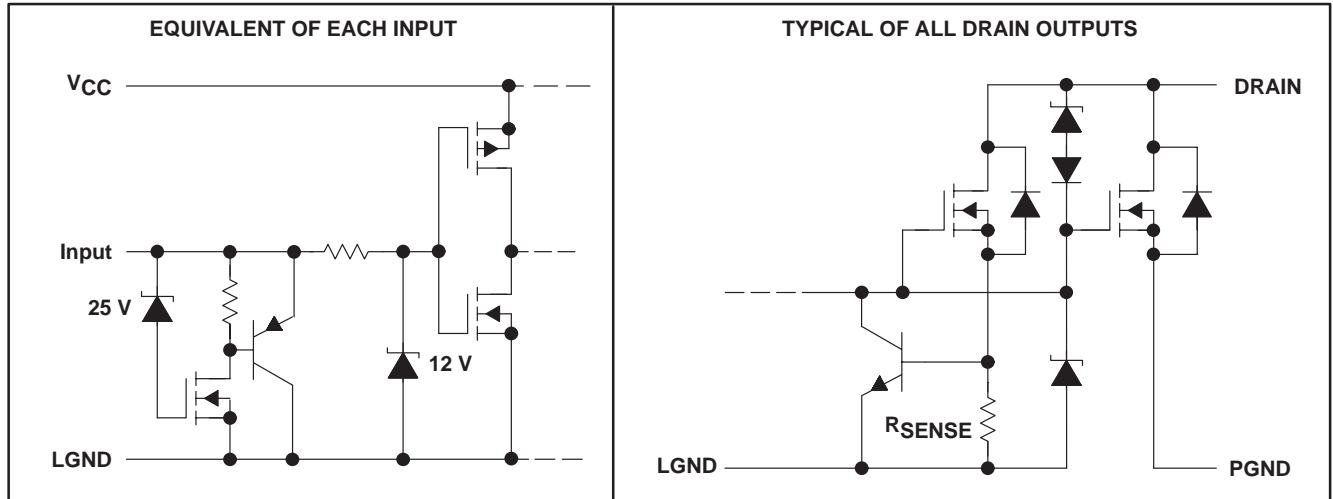
logic diagram (positive logic)



TPIC6A259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS004B – APRIL 1993 – REVISED SEPTEMBER 1995

schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	-0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	1 A
Pulsed source-to-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_D , $T_C = 25^\circ\text{C}$ (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_D , $T_C = 25^\circ\text{C}$	350 mA
Peak drain current single output, $T_C = 25^\circ\text{C}$ (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values are with respect to LGND and PGND.
 - Each power DMOS source is internally connected to PGND.
 - Pulse duration $\leq 100 \mu\text{s}$, and duty cycle $\leq 2\%$.
 - DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, $L = 210 \text{ mH}$, and $I_{AS} = 600 \text{ mA}$ (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW

TPIC6A259
POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS004B – APRIL 1993 – REVISED SEPTEMBER 1995

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	$0.85 V_{CC}$	V_{CC}	V
Low-level input voltage, V_{IL}	0	$0.15 V_{CC}$	V
Pulsed drain output current, $T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-1.8	0.6	A
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high before $\overline{G}\uparrow$, t_h (see Figure 2)	5		ns
Pulse duration, t_w (see Figure 2)	15		ns
Operating case temperature, T_C	-40	125	$^\circ\text{C}$

electrical characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 1\text{ mA}$	50			V
V_{SD} Source-to-drain diode forward voltage	$I_F = 350\text{ mA}$, See Note 3		0.8	1.1	V
I_{IH} High-level input current	$V_I = V_{CC}$			1	μA
I_{IL} Low-level input current	$V_I = 0$			-1	μA
I_{CC} Logic supply current	$I_O = 0$, $V_I = V_{CC}$ or 0		0.5	5	mA
I_{OK} Output current at which chopping starts	$T_C = 25^\circ\text{C}$, See Note 5 and Figures 3 and 4	0.6	0.8	1.1	A
$I_{(nom)}$ Nominal current	$V_{DS(on)} = 0.5\text{ V}$, $I_{(nom)} = I_D$, $T_C = 85^\circ\text{C}$, $V_{CC} = 5\text{ V}$, See Notes 5, 6, and 7		350		mA
I_D Off-state drain current	$V_{DS} = 40\text{ V}$, $T_C = 25^\circ\text{C}$		0.1	1	μA
	$V_{DS} = 40\text{ V}$, $T_C = 125^\circ\text{C}$		0.2	5	
$r_{DS(on)}$ Static drain-to-source on-state resistance	$I_D = 350\text{ mA}$, $T_C = 25^\circ\text{C}$	See Notes 5 and 6 and Figures 9 and 10	1	1.5	Ω
	$I_D = 350\text{ mA}$, $T_C = 125^\circ\text{C}$		1.7	2.5	

switching characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PHL} Propagation delay time, high- to low-level output from D	$C_L = 30\text{ pF}$, $I_D = 350\text{ mA}$, See Figures 1, 2, and 11		30		ns	
t_{PLH} Propagation delay time, low- to high-level output from D			125		ns	
t_r Rise time, drain output				60		ns
t_f Fall time, drain output				30		ns
t_a Reverse-recovery-current rise time	$I_F = 350\text{ mA}$, $di/dt = 20\text{ A}/\mu\text{s}$, See Notes 5 and 6 and Figure 5		100		ns	
t_{rr} Reverse-recovery time			300		ns	

- NOTES: 3. Pulse duration $\leq 100\ \mu\text{s}$ and duty cycle $\leq 2\%$.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^\circ\text{C}$.

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$ Thermal resistance, junction-to-case	DW		10	$^\circ\text{C}/\text{W}$
	NE	All eight outputs with equal power	10	
$R_{\theta JA}$ Thermal resistance, junction-to-ambient	DW		50	$^\circ\text{C}/\text{W}$
	NE	All eight outputs with equal power	50	



TPIC6A259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS004B – APRIL 1993 – REVISED SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION

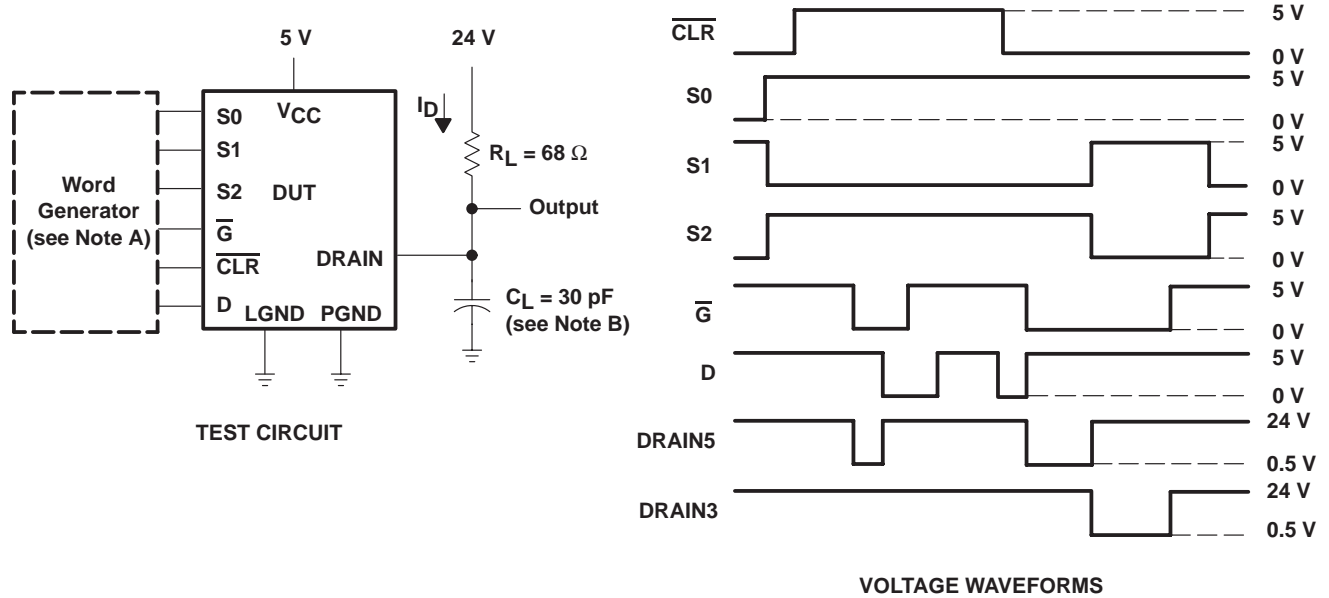


Figure 1. Typical Operation Mode

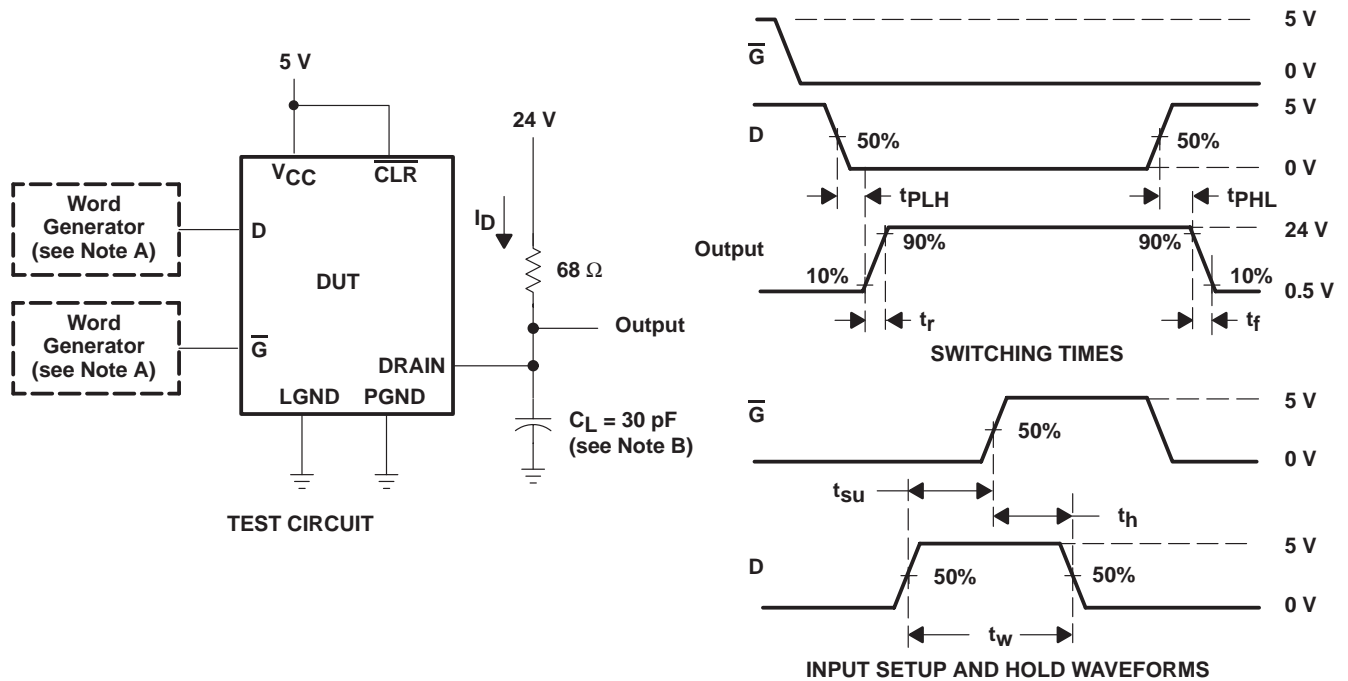
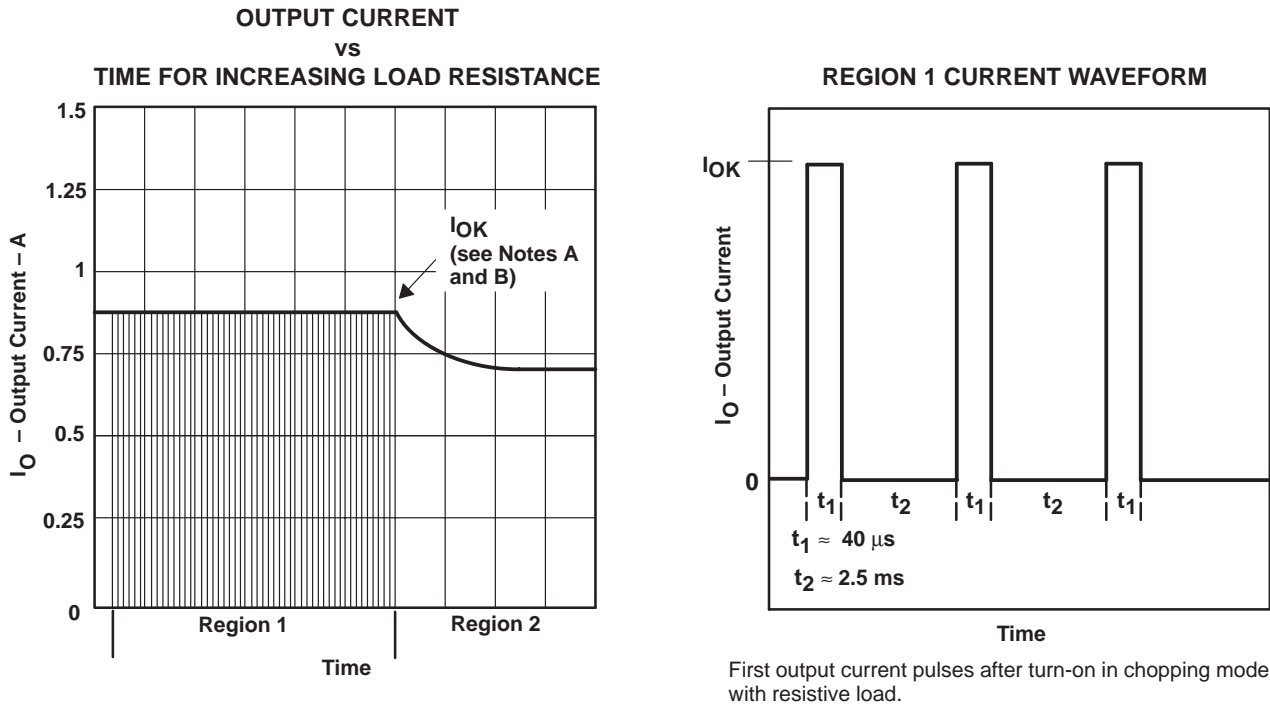


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

- NOTES: A. The word generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 300 \text{ ns}$, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK} . In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
- B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

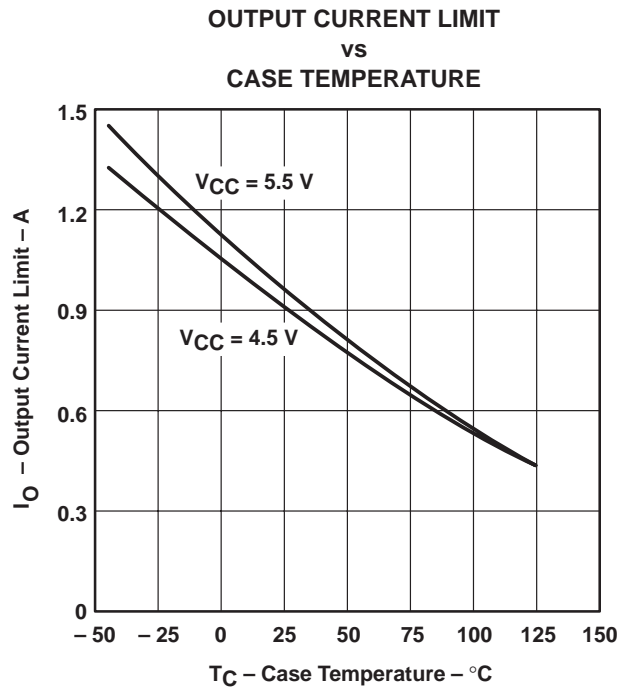
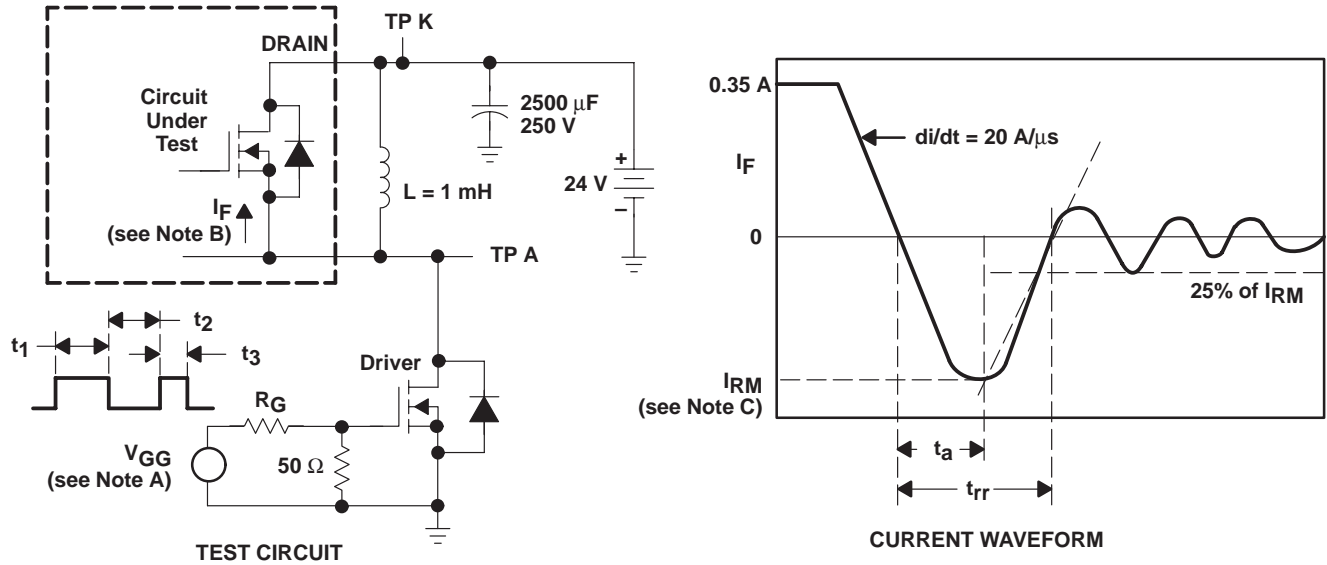


Figure 4

TPIC6A259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

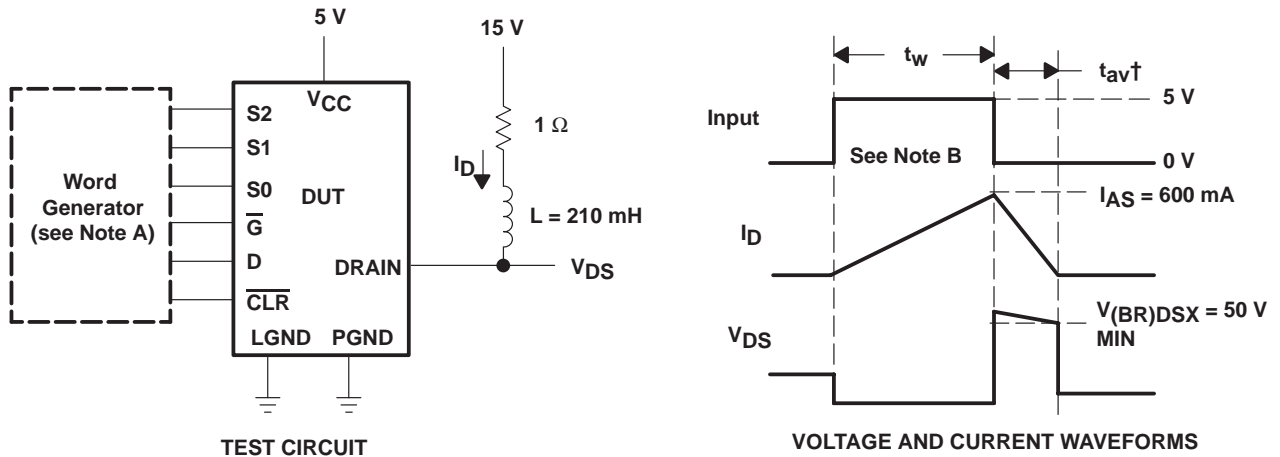
SLIS004B – APRIL 1993 – REVISED SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The V_{GG} amplitude and R_G are adjusted for $di/dt = 20 \text{ A}/\mu\text{s}$. A V_{GG} double-pulse train is used to set $I_F = 0.35 \text{ A}$, where $t_1 = 10 \mu\text{s}$, $t_2 = 7 \mu\text{s}$, and $t_3 = 3 \mu\text{s}$.
 B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
 C. I_{RM} = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche time.

- NOTES: A. The word generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_0 = 50 \Omega$.
 B. Input pulse duration, t_w , is increased until peak current $I_{AS} = 600 \text{ mA}$.
 Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2 = 75 \text{ mJ}$.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

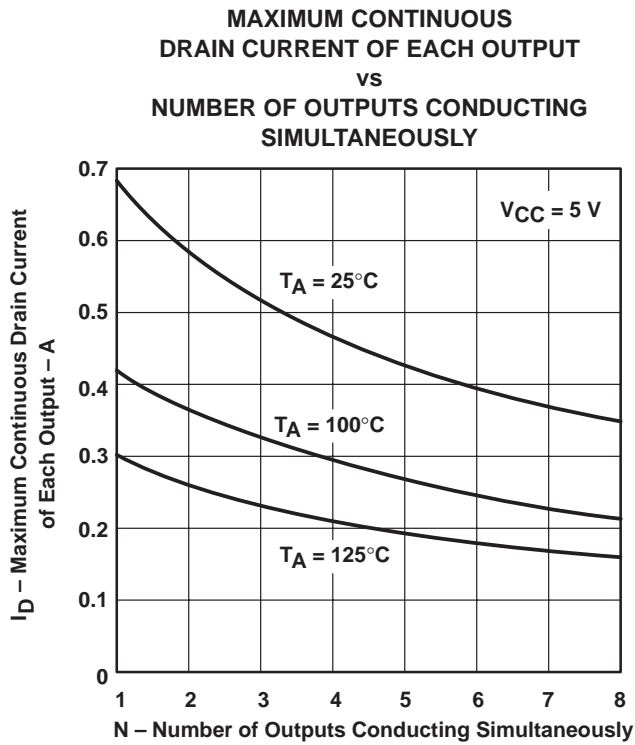


Figure 7

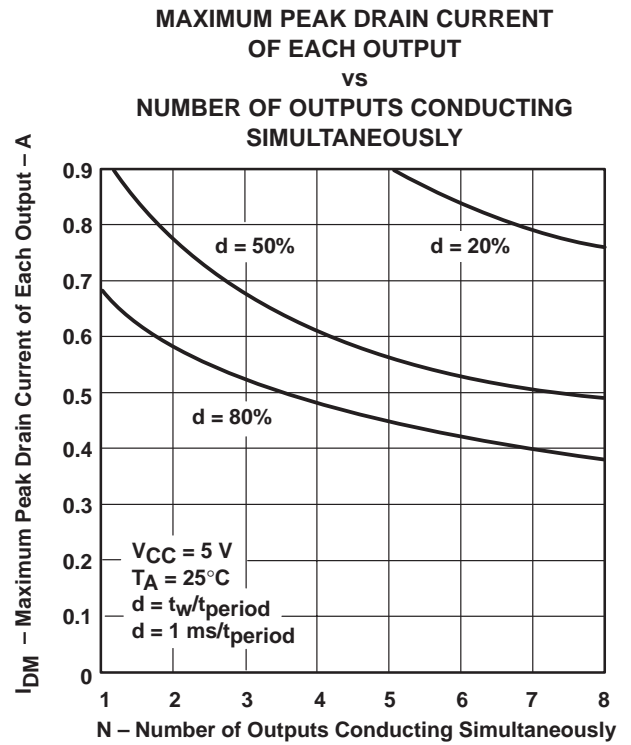


Figure 8

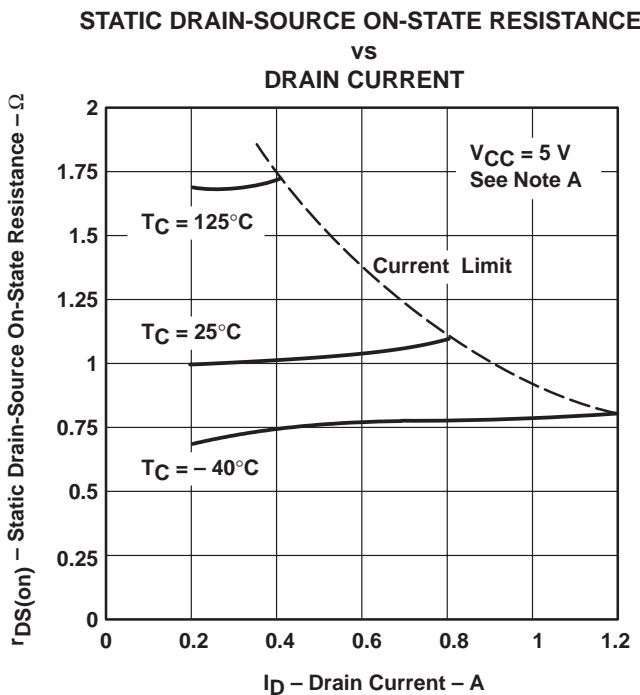


Figure 9

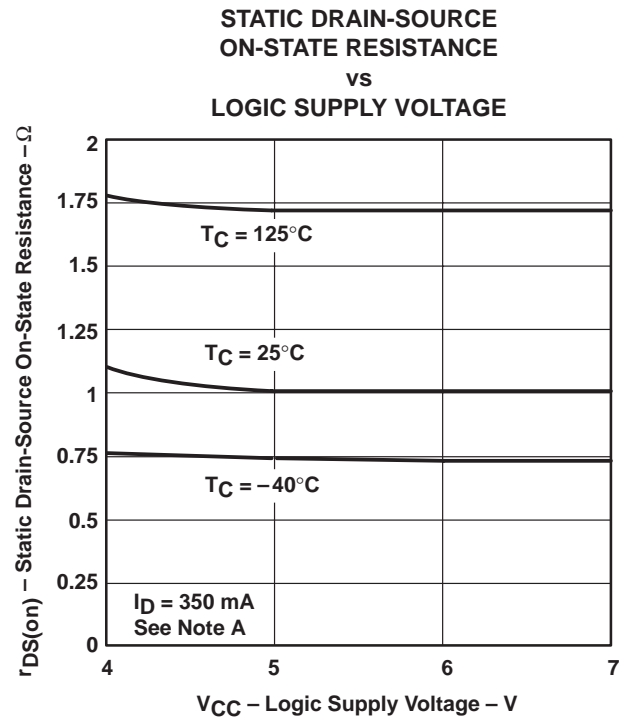


Figure 10

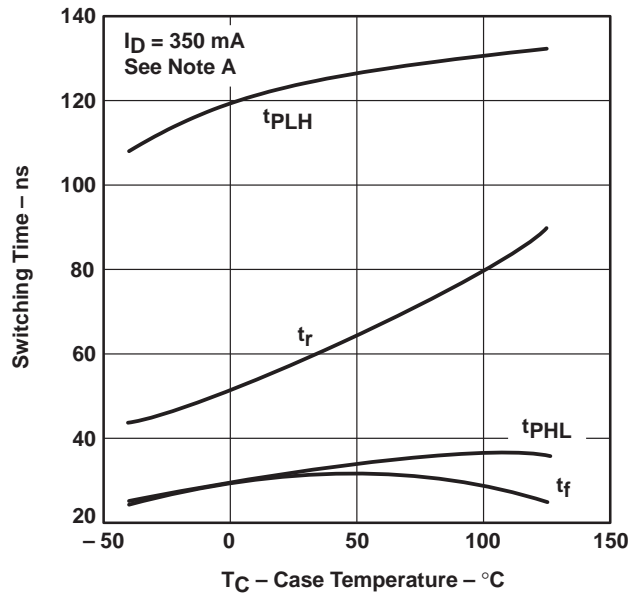
NOTE A: Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.

TPIC6A259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS004B – APRIL 1993 – REVISED SEPTEMBER 1995

TYPICAL CHARACTERISTICS

SWITCHING TIME VS CASE TEMPERATURE

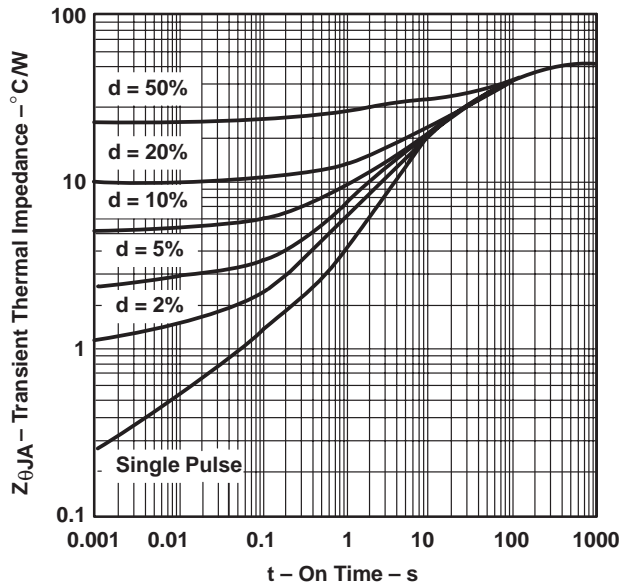


NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

THERMAL INFORMATION

NE PACKAGE TRANSIENT THERMAL IMPEDANCE VS ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta}(t_w + t_c) + Z_{\theta}(t_w) - Z_{\theta}(t_c)$$

Where:

$Z_{\theta}(t_w)$ = the single-pulse thermal impedance for $t = t_w$ seconds

$Z_{\theta}(t_c)$ = the single-pulse thermal impedance for $t = t_c$ seconds

$Z_{\theta}(t_w + t_c)$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds

$$d = t_w/t_c$$

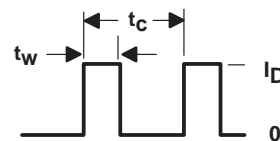


Figure 12

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