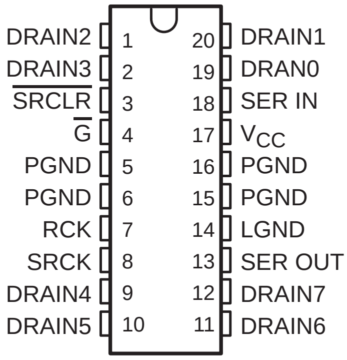
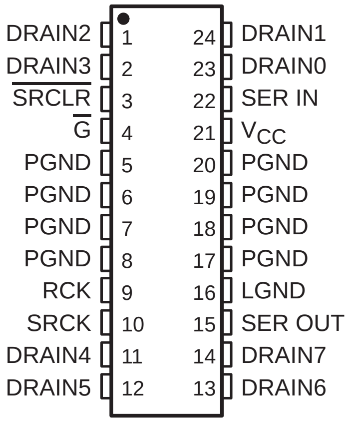
TPIC6A596 POWER LOGIC 8-BIT SHIFT REGISTER

- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Output Short-Circuit Protection**
- **Avalanche Energy . . . 75 mJ**
- **Eight 350-mA DMOS Outputs**
- **50-V Switching Capability**
- **Enhanced Cascading for Multiple Stages**
- **All Registers Cleared With Single Input**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



description

The TPIC6A596 is a monolithic, high-voltage, high-current power logic 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

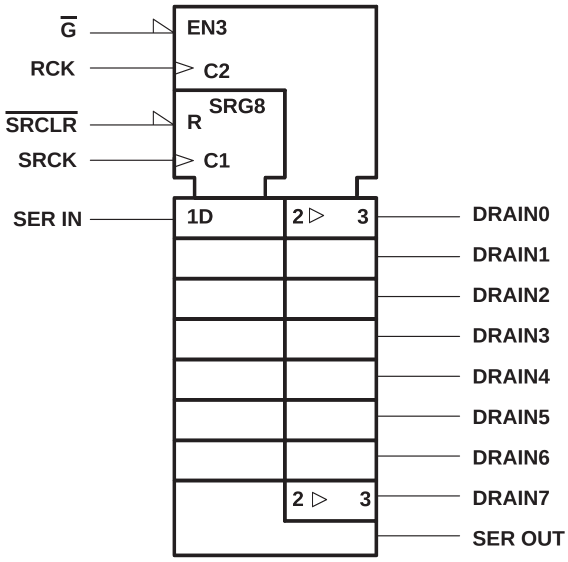
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit, D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{SRCLR}}$) is high. When $\overline{\text{SRCLR}}$ is low, all registers in the device are cleared. When output enable $\overline{\text{G}}$ is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{\text{G}}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and a 350-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

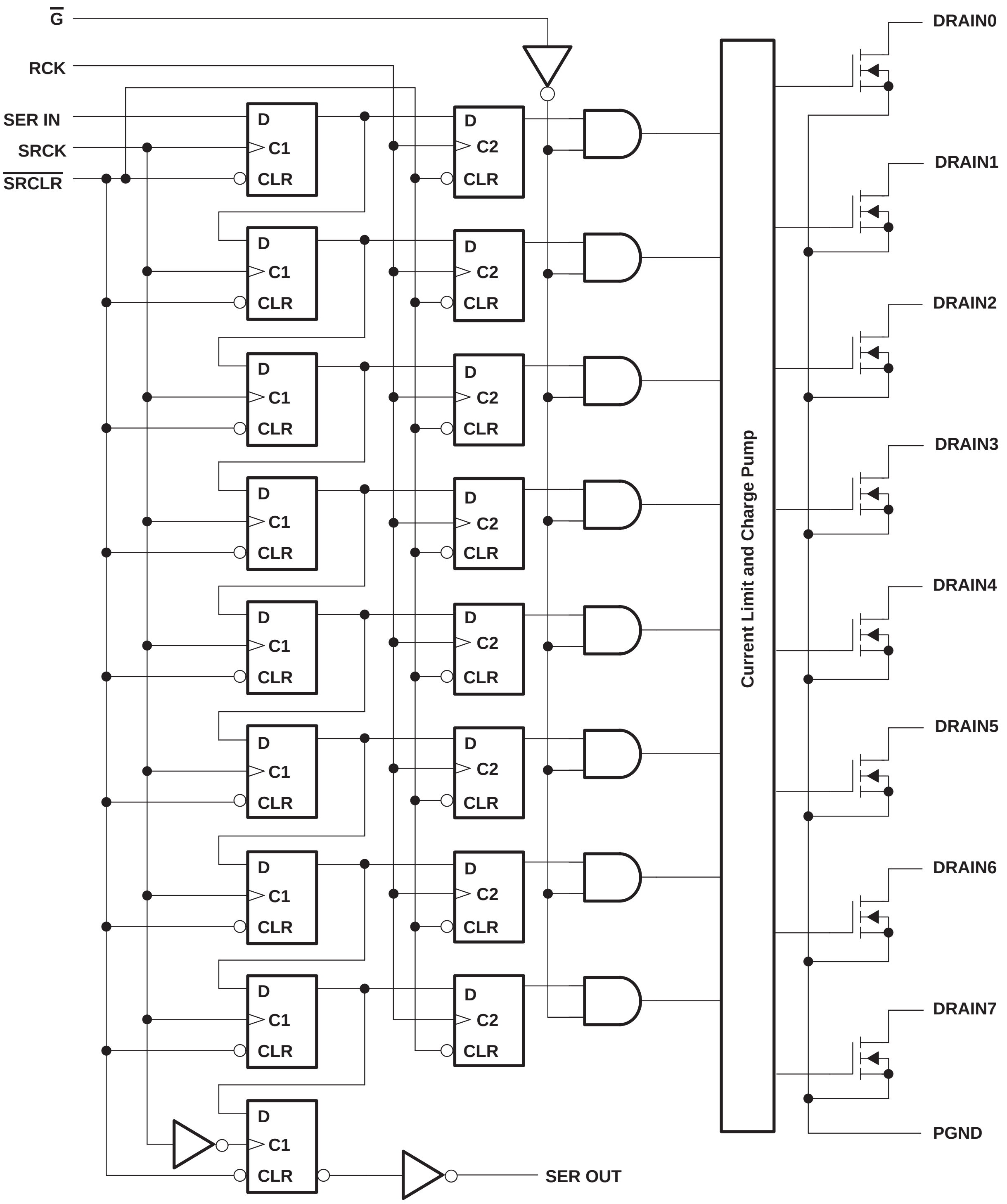
The TPIC6A596 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC6A596 is characterized for operation over the operating case temperature range of –40°C to 125°C.

logic symbol†

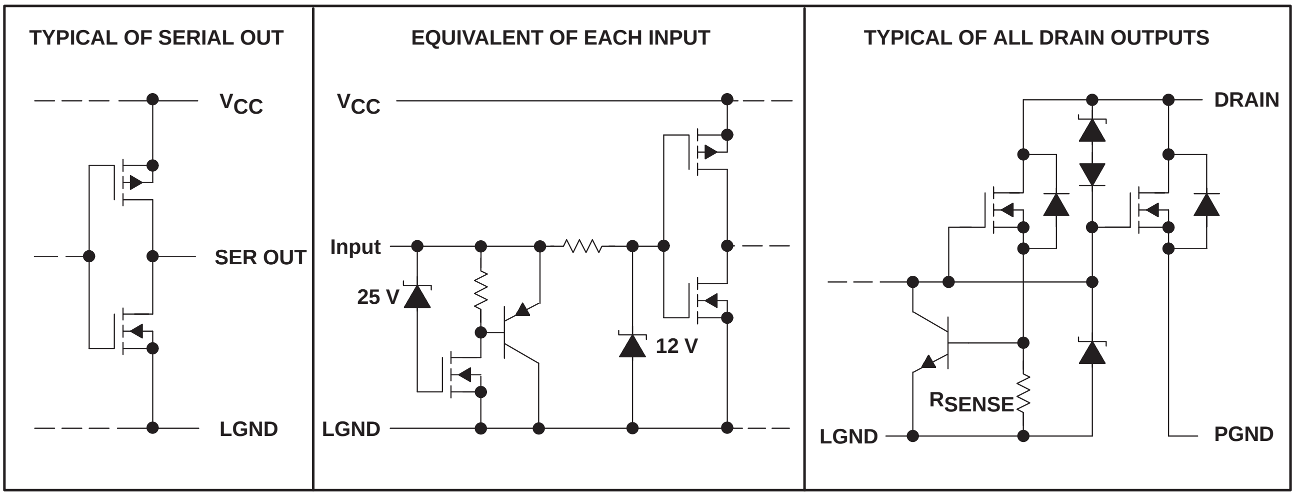


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1) .... 7 V
Logic input voltage range, V_I .... –0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2) .... 50 V
Continuous source-drain diode anode current .... 1 A
Pulsed source-drain diode anode current (see Note 3) .... 2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3) .... 1.1 A
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C .... 350 mA
Peak drain current, single output, T_A = 25°C (see Note 3) .... 1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6) .... 75 mJ
Avalanche current, I_{AS} (see Note 4) .... 600 mA
Continuous total dissipation .... See Dissipation Rating Table
Operating case temperature range, T_C .... –40°C to 125°C
Operating virtual junction temperature range, T_J .... –40°C to 150°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2 %.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, I_{AS} = 600 mA (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 125°C$ POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–1.8	0.6	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	–40	125	°C

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit T_J – T_C to 10°C maximum.

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 350 mA,	See Note 3			0.8	1.1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA			V_{CC} – 0.1	V_{CC}		V
		I_{OH} = –4 mA			V_{CC} – 0.5	V_{CC} – 0.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 µA				0	0.1	V
		I_{OL} = 4 mA				0.2	0.5	
I_{IH}	High-level input current	V_I = V_{CC}					1	µA
I_{IL}	Low-level input current	V_I = 0					–1	µA
$I_{O(chop)}$	Output current at which chopping starts	T_C = 25°C,	See Note 5 and Figures 3 and 4		0.6	0.8	1.1	A
I_{CC}	Logic supply current	I_O = 0,	V_I = V_{CC} or 0			0.5	5	mA
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, V_I = V_{CC} or 0,	I_O = 0, V_{CC} = 5 V,	C_L = 30 pF, See Figure 7		1.3		mA
$I_{(nom)}$	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_{(nom)}$ = I_D, See Notes 5, 6, and 7	T_C = 85°C,		350		mA
I_D	Drain current, off-state	V_{DS} = 40 V,	T_C = 25°C			0.1	1	µA
		V_{DS} = 40 V,	T_C = 125°C			0.2	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 350 mA,	T_C = 25°C	See Notes 5 and 6 and Figures 10 and 11		1	1.5	Ω
		I_D = 350 mA,	T_C = 125°C			1.7	2.5	

NOTES: 5. Technique should limit T_J – T_C to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

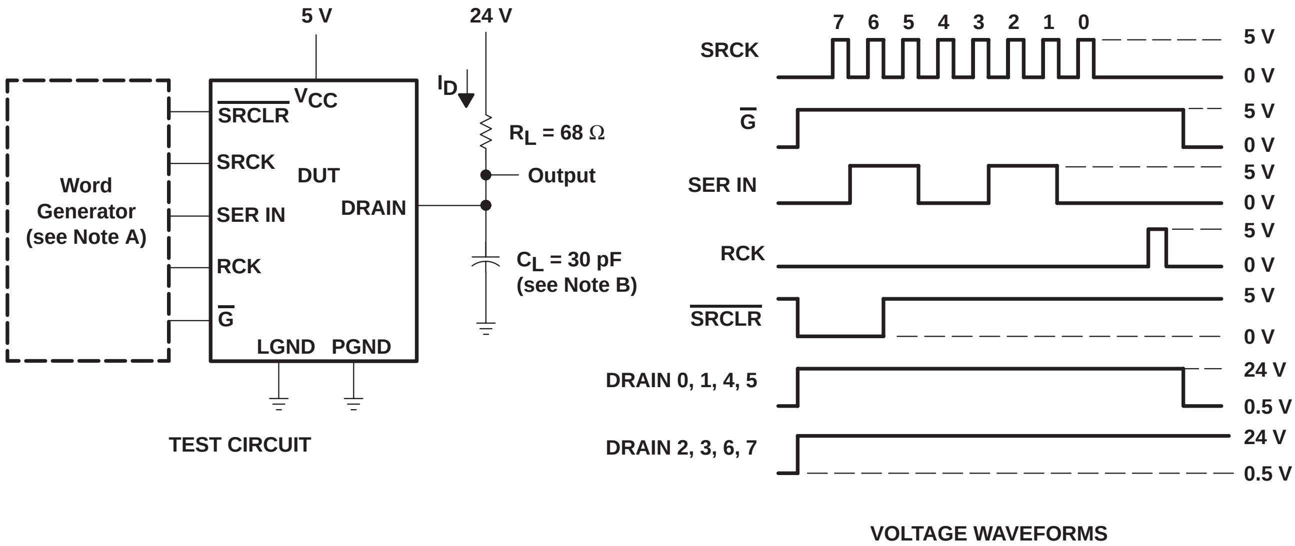
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$	C_L = 30 pF, I_D = 350 mA, See Figures 1, 2, and 12		30		ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$			125		ns
t_r	Rise time, drain output			60		ns
t_f	Fall time, drain output			30		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30 pF, I_D = 350 mA, See Figure 2		20		ns
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 350 mA, See Note 8			10	MHz
t_a	Reverse-recovery-current rise time	I_F = 350 mA, di/dt = 20 A/μs, See Notes 5 and 6 and Figure 5		100		ns
t_{rr}	Reverse-recovery time			300		ns

NOTES: 5. Technique should limit $T_J – T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
8. This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK → SEROUT propagation delay and setup time plus some timing margin.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{θJC}$	Thermal resistance, junction-to-case	DW	All eight outputs with equal power		10	°C/W
		NE			10	
$R_{θJA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		50	°C/W
		NE			50	

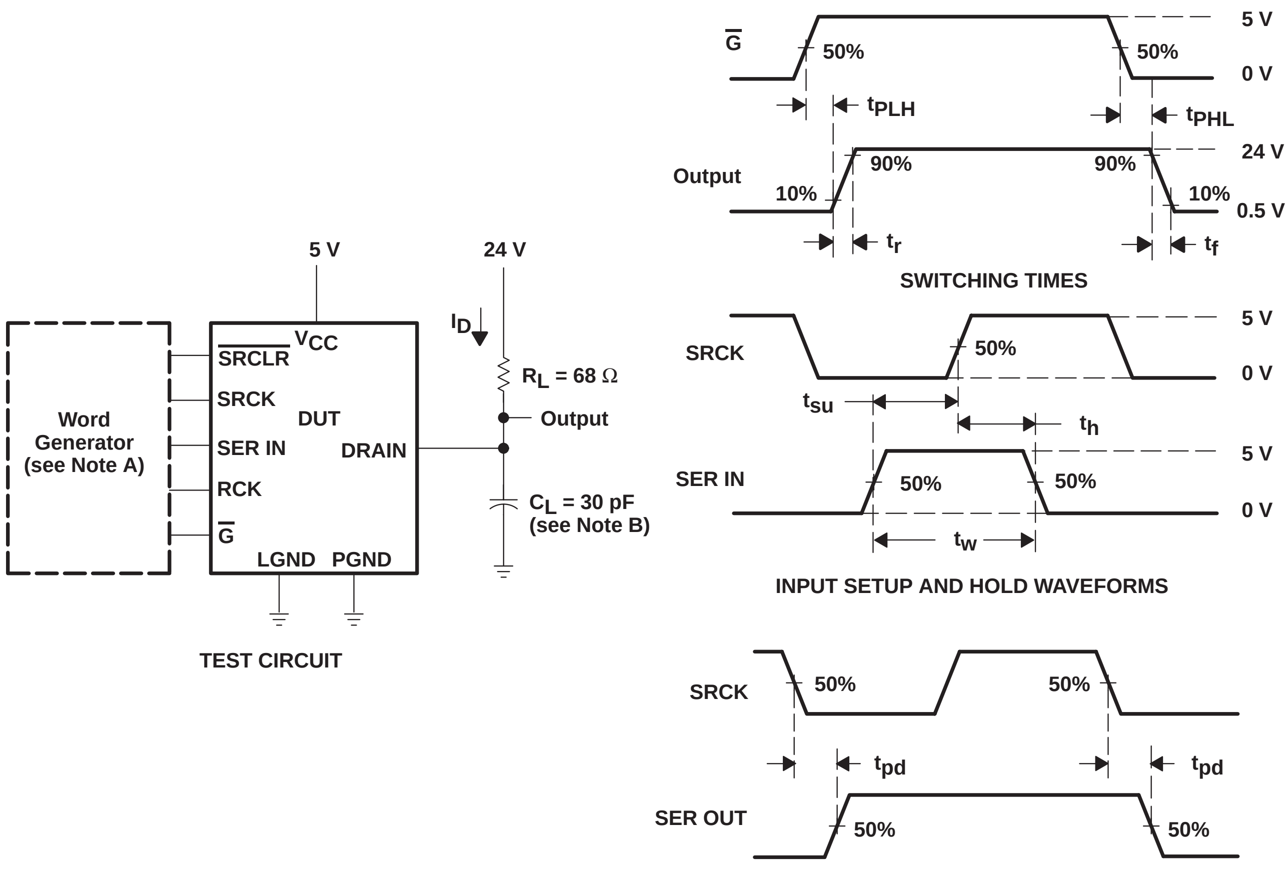
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: t_r ≤ 10 ns, t_f ≤ 10 ns, t_W = 300 ns, pulsed repetition rate (PRR) = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Resistive Load Operation

PARAMETER MEASUREMENT INFORMATION

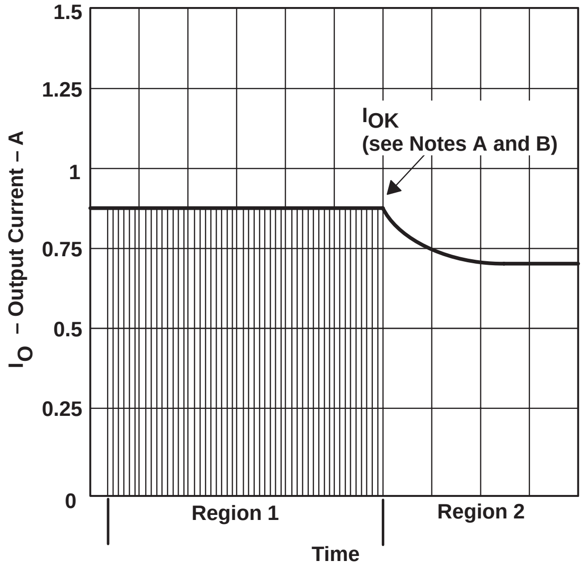


NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

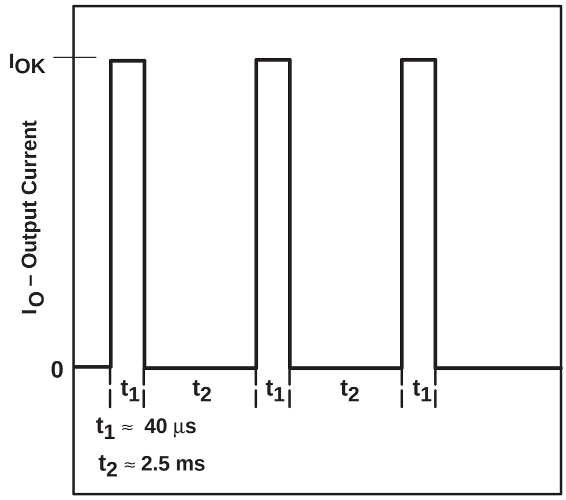
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

OUTPUT CURRENT vs TIME FOR INCREASING LOAD RESISTANCE



REGION 1 CURRENT WAVEFORM



First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

OUTPUT CURRENT LIMIT vs CASE TEMPERATURE

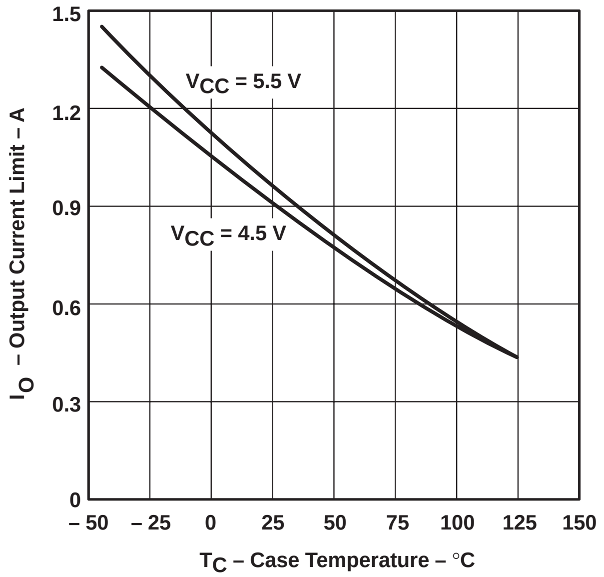
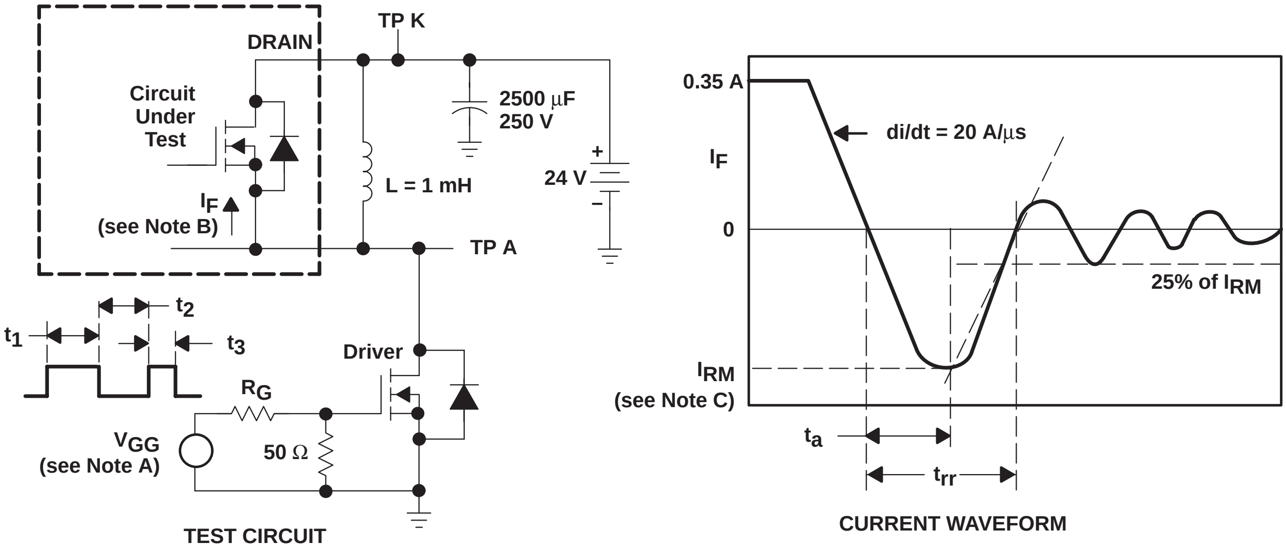


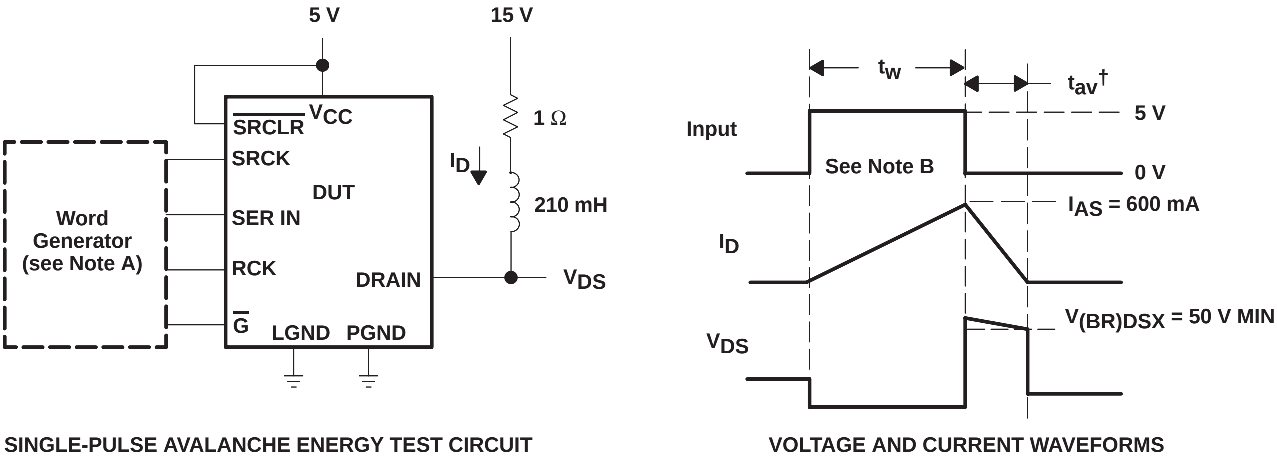
Figure 4

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
C. I_{RM} = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

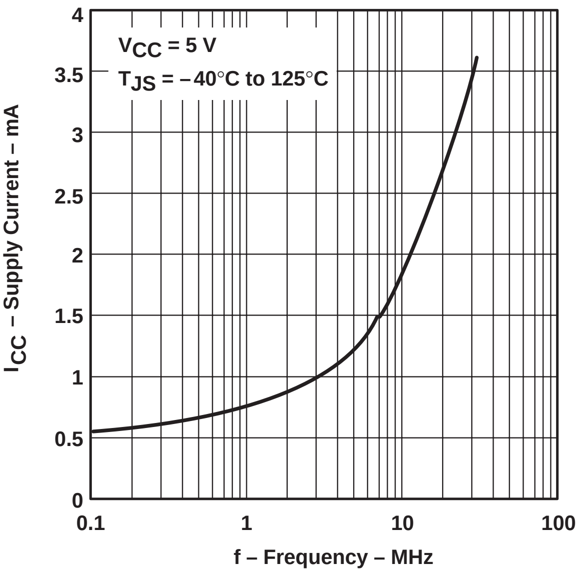


Figure 7

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

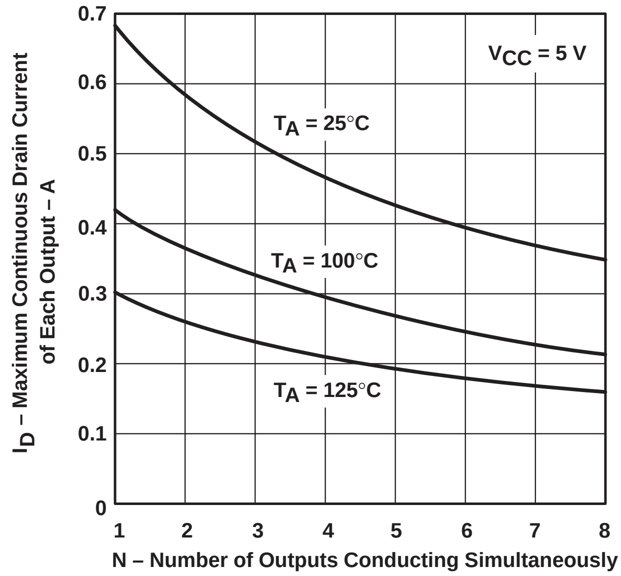


Figure 8

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

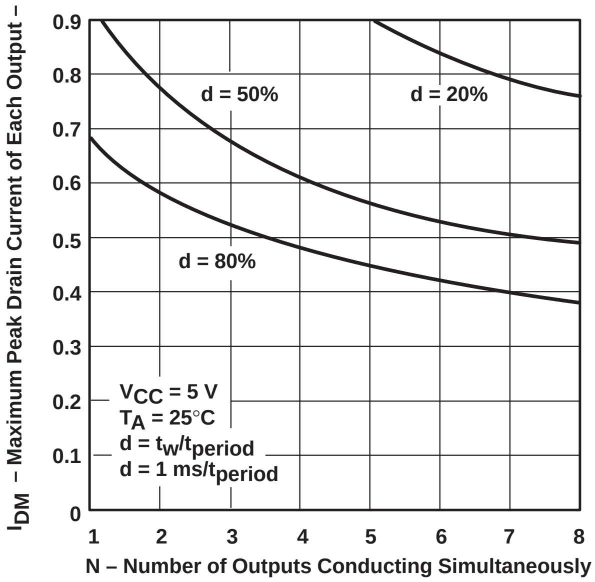
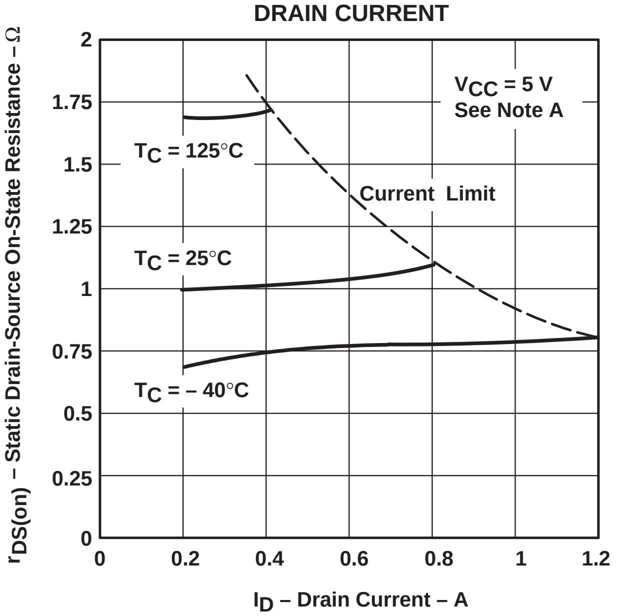


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT



NOTE A: Technique should limit $T_J – T_C$ to 10°C maximum.

Figure 10

TYPICAL CHARACTERISTICS

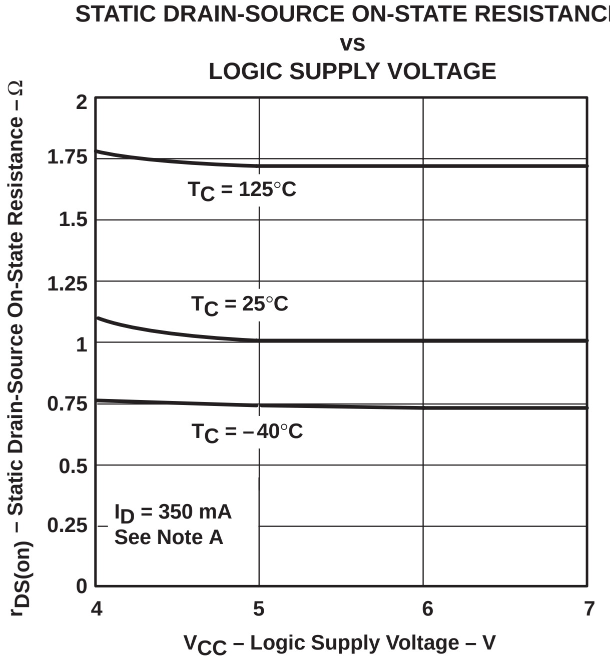


Figure 11

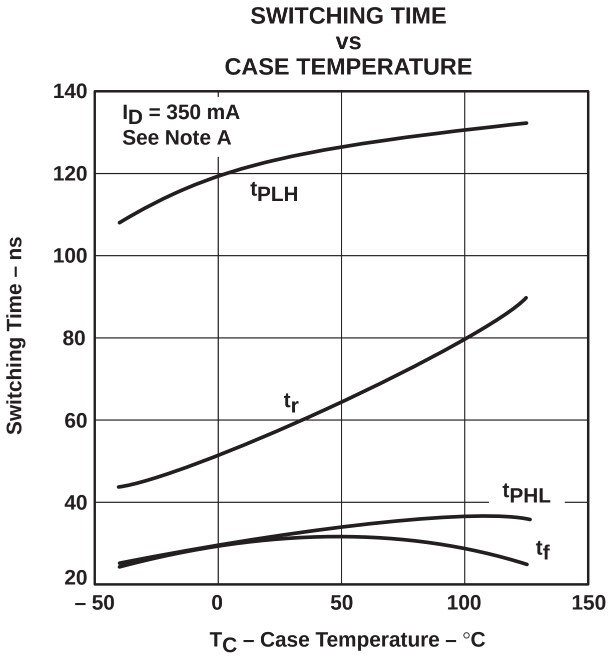


Figure 12

NOTE A: Technique should limit T_J – T_C to 10°C maximum.

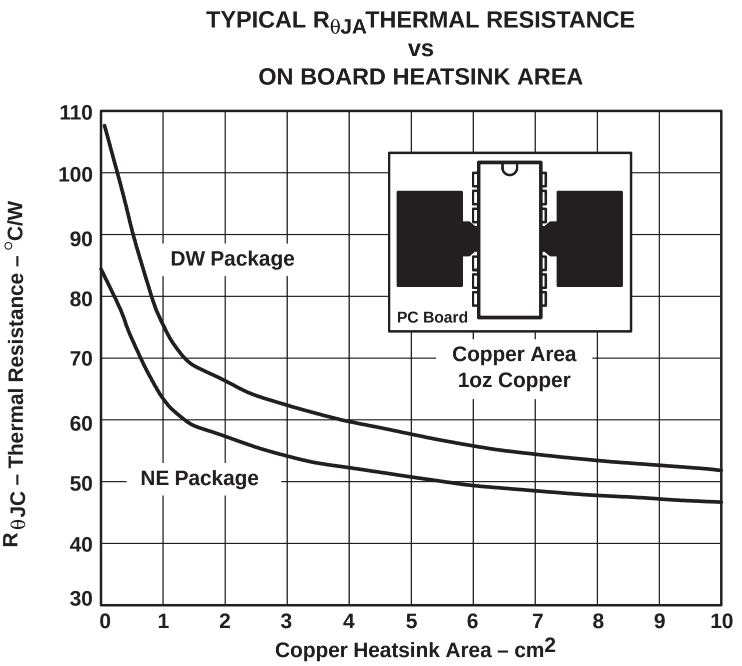
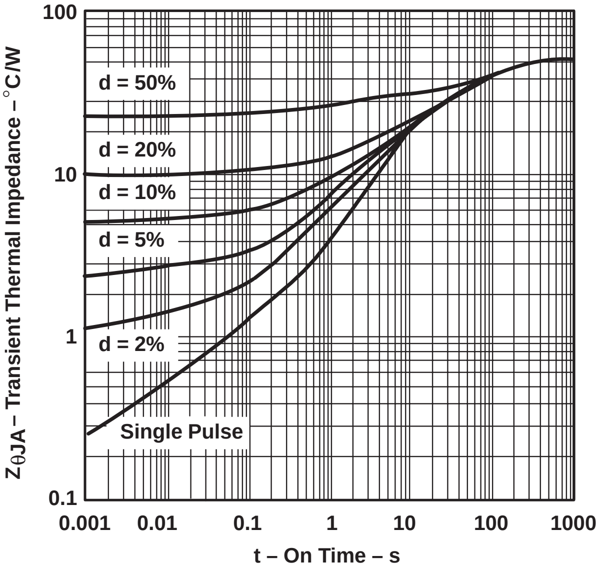


Figure 13

THERMAL INFORMATION

NE PACKAGE
TRANSIENT THERMAL IMPEDANCE
vs
ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left|\frac{t_w}{t_c}\right| R_{\theta JA} + \left|1 - \frac{t_w}{t_c}\right| Z_\theta\left(t_w + t_c\right) + Z_\theta\left(t_w\right) - Z_\theta\left(t_c\right)$$

Where:

$Z_\theta(t_w)$ = the single-pulse thermal impedance for t = t_w seconds

$Z_\theta(t_c)$ = the single-pulse thermal impedance for t = t_c seconds

$Z_\theta(t_w + t_c)$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

$d = t_w/t_c$

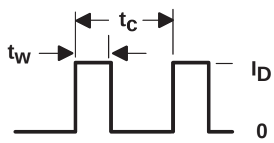


Figure 14

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.