features

- **High-Speed 6 MSPS ADC**
- **4 Single-Ended or 2 Differential Inputs**
- **Simultaneous Sampling of 4 Single-Ended Signals or 2 Differential Signals or Combination of Both**
- **Differential Nonlinearity Error: ±1 LSB**
- **Integral Nonlinearity Error: ±1.5 LSB**
- **Signal-to-Noise and Distortion Ratio: 68 dB at f_I = 2 MHz**
- **Auto-Scan Mode for 2, 3, or 4 Inputs**
- **3-V or 5-V Digital Interface Compatible**
- **Low Power: 216 mW Max**
- **5-V Analog Single Supply Operation**
- **Internal Voltage References . . . 50 PPM/°C and ±5% Accuracy**
- **Glueless DSP Interface**
- **Parallel µC/DSP Interface**
- **Integrated FIFO**
- **Available in TSSOP Package**

applications

- **Radar Applications**
- **Communications**
- **Control Applications**
- **High-Speed DSP Front-End**
- **Automotive Applications**

DA PACKAGE
(TOP VIEW)

D0	1	32	AINP
D1	2	31	AINM
D2	3	30	BINP
D3	4	29	BINM
D4	5	28	REFIN
D5	6	27	REFOUT
BV_{DD}	7	26	REFP
BGND	8	25	REFM
D6	9	24	AGND
D7	10	23	AV_{DD}
D8	11	22	$\overline{\text{CS0}}$
D9	12	21	CS1
D10/RA0	13	20	$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)
D11/RA1	14	19	$\overline{\text{RD}}$
CONV_CLK ($\overline{\text{CONVST}}$)	15	18	DV_{DD}
DATA_AV	16	17	DGND

description

The THS1206 is a CMOS, low-power, 12-bit, 6 MSPS analog-to-digital converter (ADC). The speed, resolution, bandwidth, and single-supply operation are suited for applications in radar, imaging, high-speed acquisition, and communications. A multistage pipelined architecture with output error correction logic provides for no missing codes over the full operating temperature range. Internal control registers are used to program the ADC into the desired mode. The THS1206 consists of four analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured to single-ended or differential inputs. An integrated 16 word deep FIFO allows the storage of data in order to take the load off of the processor connected to the ADC. Internal reference voltages for the ADC (1.5 V and 3.5 V) are provided.

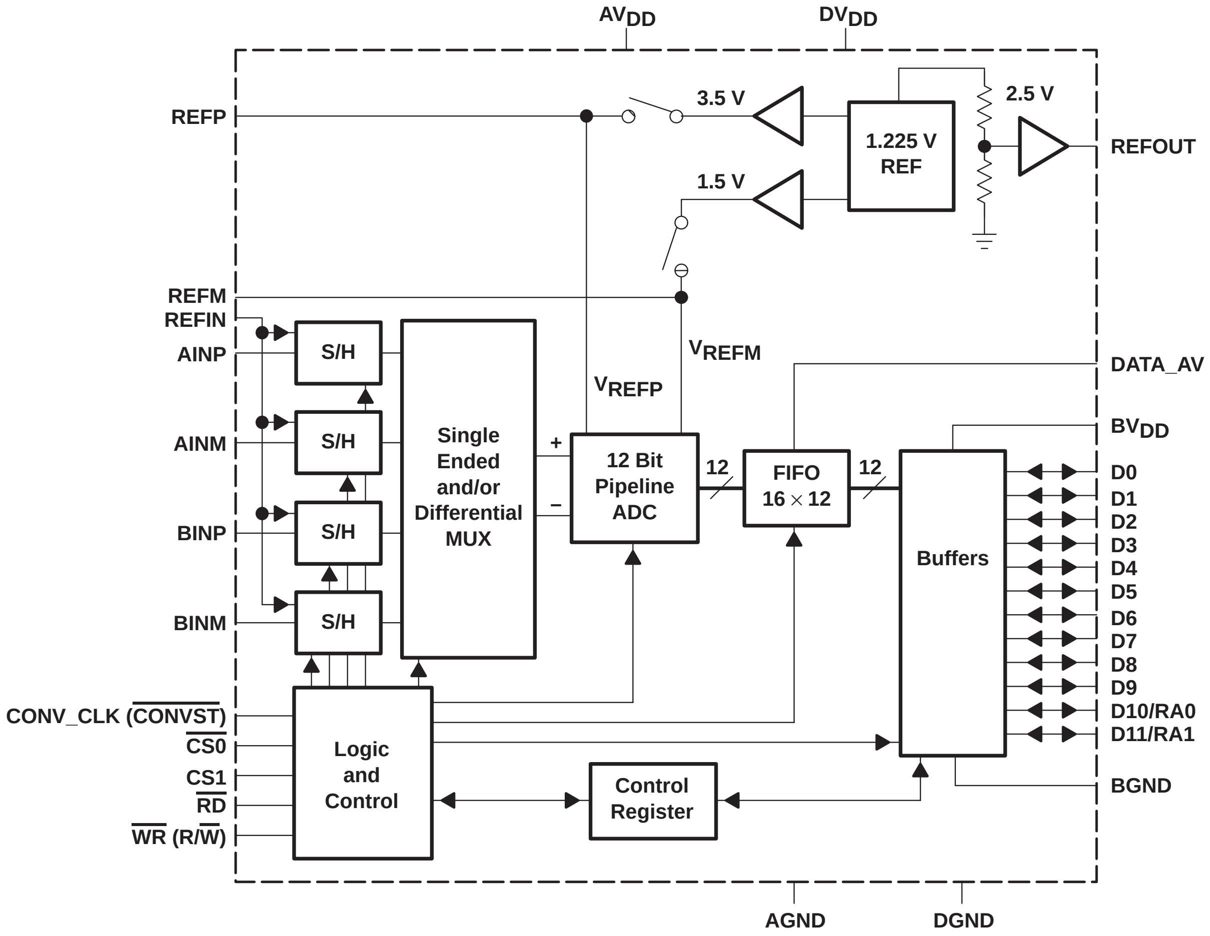
An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. Two different conversion modes can be selected. In single conversion mode, a single and simultaneous conversion of up to four inputs can be initiated by using the single conversion start signal ($\overline{\text{CONVST}}$). The conversion clock in single conversion mode is generated internally using a clock oscillator circuit. In continuous conversion mode, an external clock signal is applied to the CONV_CLK input of the THS1206. The internal clock oscillator is switched off in continuous conversion mode.

The THS1206C is characterized for operation from 0°C to 70°C, the THS1206I is characterized for operation from –40°C to 85°C, the THS1206Q is characterized to meet the rigorous requirements of the automotive environment from –40°C to 125°C, and the THS1206M is characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE TSSOP (DA)
0°C to 70°C	THS1206CDA
–40°C to 85°C	THS1206IDA
–40°C to 125°C	THS1206QDA
–55°C to 125°C	THS1206MDA

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AINP	32	I	Analog input, single-ended or positive input of differential channel A
AINM	31	I	Analog input, single-ended or negative input of differential channel A
BINP	30	I	Analog input, single-ended or positive input of differential channel B
BINM	29	I	Analog input, single-ended or negative input of differential channel B
AV_{DD}	23	I	Analog supply voltage
AGND	24	I	Analog ground
BV_{DD}	7	I	Digital supply voltage for buffer
BGND	8	I	Digital ground for buffer
CONV_CLK ($\overline{CONVST}$)	15	I	Digital input. This input is used to apply an external conversion clock in continuous conversion mode. In single conversion mode, this input functions as the conversion start ($\overline{CONVST}$) input. A high to low transition on this input holds simultaneously the selected analog input channels and initiates a single conversion of all selected analog inputs.
$\overline{CS0}$	22	I	Chip select input (active low)
CS1	21	I	Chip select input (active high)
DATA_AV	16	O	Data available signal, which can be used to generate an interrupt for processors and as a level information of the internal FIFO. This signal can be configured to be active low or high and can be configured as a static level or pulse output. See Table 14.
DGND	17	I	Digital ground. Ground reference for digital circuitry.
DV_{DD}	18	I	Digital supply voltage
D0 – D9	1–6, 9–12	I/O/Z	Digital input, output; D0 = LSB
D10/RA0	13	I/O/Z	Digital input, output. The data line D10 is also used as an address line (RA0) for the control register. This is required for writing to the control register 0 and control register 1. See Table 8.
D11/RA1	14	I/O/Z	Digital input, output (D11 = MSB). The data line D11 is also used as an address line (RA1) for the control register. This is required for writing to control register 0 and control register 1. See Table 8.
REFIN	28	I	Common-mode reference input for the analog input channels. It is recommended that this pin be connected to the reference output REFOUT.
REFP	26	I	Reference input, requires a bypass capacitor of 10 µF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 9.
REFM	25	I	Reference input, requires a bypass capacitor of 10 µF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 9.
REFOUT	27	O	Analog fixed reference output voltage of 2.5 V. Sink and source capability of 250 µA. The reference output requires a capacitor of 10 µF to AGND for filtering and stability.
$\overline{RD}$†	19	I	The $\overline{RD}$ input is used only if the $\overline{WR}$ input is configured as a write only input. In this case, it is a digital input, active low as a data read select from the processor. See timing section.
$\overline{WR}$ (R/$\overline{W}$)†	20	I	This input is programmable. It functions as a read-write input R/W and can also be configured as a write-only input $\overline{WR}$, which is active low and used as data write select from the processor. In this case, the $\overline{RD}$ input is used as a read input from the processor. See timing section.

† The start-conditions of $\overline{RD}$ and $\overline{WR}$ (R/$\overline{W}$) are unknown. The first access to the ADC has to be a write access to initialize the ADC.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, DGND to DV_{DD} . . . . –0.3 V to 6.5 V
BGND to BV_{DD} . . . . –0.3 V to 6.5 V
AGND to AV_{DD} . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . AGND – 0.3 V to AV_{DD} + 1.5 V
Reference input voltage . . . . –0.3 + AGND to AV_{DD} + 0.3 V
Digital input voltage range . . . . –0.3 V to BV_{DD}/DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J . . . . –55°C to 150°C
Operating free-air temperature range, T_A THS1206C . . . . 0°C to 70°C
THS1206I . . . . –40°C to 85°C
THS1206Q . . . . –40°C to 125°C
THS1206M . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DA	1453 mW	11.62 mW/°C	930 mW	756 mW	291 mW

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$). Thermal resistances are not production tested and are for informational purposes only.

recommended operating conditions

power supply

		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DD}	4.75	5	5.25	V
	DV_{DD}	3	3.3	5.25	
	BV_{DD}	3	3.3	5.25	

analog and reference inputs

	MIN	NOM	MAX	UNIT
Analog input voltage in single-ended configuration	V_{REFM}		V_{REFP}	V
Common-mode input voltage V_{CM} in differential configuration	1	2.5	4	V
External reference voltage, V_{REFP} (optional)		3.5	AV_{DD}–1.2	V
External reference voltage, V_{REFM} (optional)	1.4	1.5		V
Input voltage difference, REFP – REFM		2		V

recommended operating conditions (continued)

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	BV_{DD} = 3.3 V	2			V
	BV_{DD} = 5.25 V	2.6			V
Low-level input voltage, V_{IL}	BV_{DD} = 3.3 V			0.6	V
	BV_{DD} = 5.25 V			0.6	V
Input CONV_CLK frequency	DV_{DD} = 3 V to 5.25 V	0.1		6	MHz
CONV_CLK pulse duration, clock high, $t_{w(CONV\_CLKH)}$	DV_{DD} = 3 V to 5.25 V	80	83	5000	ns
CONV_CLK pulse duration, clock low, $t_{w(CONV\_CLKL)}$	DV_{DD} = 3 V to 5.25 V	80	83	5000	ns
Operating free-air temperature, T_A	THS1206CDA	0		70	°C
	THS1206IDA	–40		85	°C
	THS1206QDA	–40		125	°C
	THS1206MDA	–55		125	°C

electrical characteristics over recommended operating conditions, V_{REF} = internal (unless otherwise noted)

digital specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Digital inputs							
I_{IH}	High-level input current	DV_{DD} = digital inputs		–50		50	µA
I_{IL}	Low-level input current	Digital input = 0 V		–50		50	µA
C_i	Input capacitance				5		pF
Digital outputs							
V_{OH}	High-level output voltage	I_{OH} = –50 µA	BV_{DD} = 3.3 V, BV_{DD} = 5 V	BV_{DD}–0.5			V
				BV_{DD}–0.5			V
V_{OL}	Low-level output voltage					0.4	V
						0.4	V
I_{OZ}	High-impedance-state output current	CS1 = DGND,	CS0 = DVDD	–10		10	µA
C_O	Output capacitance				5		pF
C_L	Load capacitance at databus D0 – D11					30	pF

electrical characteristics over recommended operating conditions, V_{REF} = internal (unless otherwise noted) (continued)

dc specifications

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution			12			Bits
Accuracy							
	Integral nonlinearity, INL	C and I suffix				±1.5	LSB
		Q and M suffix				±1.8	
	Differential nonlinearity, DNL					±1	LSB
	Offset error	After calibration in single-ended mode		–15†		15†	mV
		After calibration in differential mode		–5†		5†	mV
	Gain error					1%	FSR
Analog input							
	Input capacitance				15		pF
	Input leakage current	$V_{AIN} = V_{REFM}$ to V_{REFP}				±10	µA
Internal voltage reference							
	Accuracy, V_{REFP}	C and I suffix		3.33	3.5	3.67	V
		Q and M suffix		3.3	3.5	3.7	
	Accuracy, V_{REFM}	C and I suffix		1.42	1.5	1.58	V
		Q and M suffix		1.3	1.5	1.7	
	Temperature coefficient				50		PPM/°C
	Reference noise				100		µV
	Accuracy, REFOUT	C and I suffix		2.475	2.5	2.525	V
		Q and M suffix		2.3	2.5	2.7	
Power supply							
I_{DDA}	Analog supply current	AV_{DD} =5 V, $BV_{DD} = DV_{DD}$ = 3.3 V			36	40	mA
I_{DDD}	Digital supply voltage	AV_{DD} = 5 V, $BV_{DD} = DV_{DD}$ = 3.3 V			0.5	1	mA
I_{DDB}	Buffer supply voltage	AV_{DD} = 5 V, $BV_{DD} = DV_{DD}$ = 3.3 V			1.5	4	mA
I_{DD_P}	Supply current in power-down mode	AV_{DD} = 5 V, $BV_{DD} = DV_{DD}$ = 3.3 V	C and I suffix			7	mA
			Q and M suffix			10	
	Power dissipation	AV_{DD} = 5 V, $DV_{DD} = BV_{DD}$ = 3.3 V			186	216	mW
	Power dissipation in power down	AV_{DD} = 5 V, $DV_{DD} = BV_{DD}$ = 3.3 V			30		mW

† Not production tested for M and Q suffix devices.

electrical characteristics over recommended operating conditions, V_{REF} = internal, f_s = 6 MHz, f_I = 2 MHz at –1dBFS (unless otherwise noted) (continued)

ac specifications, AV_{DD} = 5 V, BV_{DD} = DV_{DD} = 3.3 V, C_L < 30 pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion	Differential mode		63	68		dB
		Single-ended mode (see Note 1)			64		dB
SNR	Signal-to-noise ratio	Differential mode		64	69		dB
		Single-ended mode (see Note 1)			65		dB
THD	Total harmonic distortion	Differential mode	C and I suffix		–73	–69	dB
			Q and M suffix		–73	–67	dB
		Single-ended mode	C and I suffix		–73	–69	dB
			Q and M suffix		–73	–67	dB
ENOB (SNR)	Effective number of bits	Differential mode		10.3	11		Bits
		Single-ended mode (see Note 1)			10.4		Bits
SFDR	Spurious free dynamic range	Differential mode		68	75		dB
		Single-ended mode		68	75		dB
Analog Input							
	Full-power bandwidth with a source impedance of 150 Ω in differential configuration.	FS sinewave, –3 dB			96		MHz
	Full-power bandwidth with a source impedance of 150 Ω in single-ended configuration.	FS sinewave, –3 dB			54		MHz
	Small-signal bandwidth with a source impedance of 150 Ω in differential configuration.	100 mVpp sinewave, –3 dB			96		MHz
	Small-signal bandwidth with a source impedance of 150 Ω in single-ended configuration.	100 mVpp sinewave, –3 dB			54		MHz

NOTE 1: The SNR (ENOB) and SINAD is degraded typically by 2 dB in single-ended mode when the reading of data is asynchronous to the sampling clock.

timing specifications, AV_{DD} = 5 V, BV_{DD} = DV_{DD} = 3.3 V, V_{REF} = internal, C_L < 30 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(DATA\_AV)}$	Delay time			5		ns
$t_{d(o)}$	Delay time			5		ns
t_{pipe}	Latency			5		CONV CLK

timing specification of the single conversion mode†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	Clock cycle of the internal clock oscillator		159	167	175	ns
t_{w1}	Pulse width, $\overline{\text{CONVST}}$		1.5×t_c			ns
t_{dA}	Aperture time			1		ns
t_2	Time between consecutive start of single conversion	1 analog input	2×t_c			ns
		2 analog inputs	3×t_c			
		3 analog inputs	4×t_c			ns
		4 analog inputs	5×t_c			
$t_{d(DATA\_AV)}$	Delay time, DATA_AV becomes active for the trigger level condition: TRIG0 = 0, TRIG1 = 0	1 analog input, TL = 1			6×t_c	ns
		2 analog inputs, TL = 2			7×t_c	
		3 analog inputs, TL = 3			8×t_c	ns
		4 analog inputs, TL = 4			9×t_c	
	Delay time, DATA_AV becomes active for the trigger level condition: TRIG0 = 1, TRIG1 = 0	1 analog input, TL = 4			3×t_2 +6×t_c	ns
		2 analog inputs, TL = 4			t_2 +7×t_c	
		3 analog inputs, TL = 6			t_2 +8×t_c	ns
		4 analog inputs, TL = 8			t_2 +9×t_c	
	Delay time, DATA_AV becomes active for the trigger level condition: TRIG0 = 0, TRIG1 = 1	1 analog input, TL = 8			7×t_2 +6×t_c	ns
		2 analog inputs, TL = 8			3×t_2 +7×t_c	
		3 analog inputs, TL = 9			2×t_2 +8×t_c	ns
		4 analog inputs, TL = 12			2×t_2 +9×t_c	
$t_{d(DATA\_AV)}$	Delay time, DATA_AV becomes active for the trigger level condition: TRIG0 = 1, TRIG1 = 1	1 analog input, TL = 14			13×t_2 +6×t_c	ns
		2 analog inputs, TL = 12			5×t_2 +7×t_c	
		3 analog inputs, TL = 12			3×t_2 +8×t_c	ns

† Timing parameters are ensured by design but are not tested.

detailed description

reference voltage

The THS1206 has a built-in reference, which provides the reference voltages for the ADC. VREFP is set to 3.5 V and VREFM is set to 1.5 V. An external reference can also be used through two reference input pins, REFP and REFM, if the reference source is programmed as external. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively.

analog inputs

The THS1206 consists of 4 analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured as single-ended or differential inputs. The desired analog input channel can be programmed.

converter

The THS1206 uses a 12-bit pipelined multistaged architecture with 4 1-bit stages followed by 4 2-bit stages, which achieves a high sample rate with low power consumption. The THS1206 distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the number of comparators used in a traditional flash ADC. A sample-and-hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the eighth stages operate on the seven preceding samples.

conversion modes

The conversion can be performed in two different conversion modes. In the single conversion mode, the conversion is initiated by an external signal ($\overline{\text{CONVST}}$). An internal oscillator controls the conversion time. In the continuous conversion mode, an external clock signal is applied to the clock input (CONV_CLK). A new conversion is started with every falling edge of the applied clock signal.

sampling rate

The maximum possible conversion rate per channel is dependent on the selected analog input channels. Table 1 shows the maximum conversion rate in the continuous conversion mode for different combinations.

Table 1. Maximum Conversion Rate in Continuous Conversion Mode

CHANNEL CONFIGURATION	NUMBER OF CHANNELS	MAXIMUM CONVERSION RATE PER CHANNEL
1 single-ended channel	1	6 MSPS
2 single-ended channels	2	3 MSPS
3 single-ended channels	3	2 MSPS
4 single-ended channels	4	1.5 MSPS
1 differential channel	1	6 MSPS
2 differential channels	2	3 MSPS
1 single-ended and 1 differential channel	2	3 MSPS
2 single-ended and 1 differential channels	3	2 MSPS

The maximum conversion rate in the continuous conversion mode per channel, fc, is given by:

$$fc = \frac{6\ \text{MSPS}}{\#\ \text{channels}}$$

Table 2 shows the maximum conversion rate in the single conversion mode.

sampling rate (continued)

Table 2. Maximum Conversion Rate in Single Conversion Mode

CHANNEL CONFIGURATION	NUMBER OF CHANNELS	MAXIMUM CONVERSION RATE PER CHANNEL
1 single-ended channel	1	3 MSPS
2 single-ended channels	2	2 MSPS
3 single-ended channels	3	1.5 MSPS
4 single-ended channels	4	1.2 MSPS
1 differential channel	1	3 MSPS
2 differential channels	2	2 MSPS
1 single-ended and 1 differential channel	2	1.5 MSPS
2 single-ended and 1 differential channels	3	1.2 MSPS

single conversion mode

In single conversion mode, a single conversion of the selected analog input channels is performed. The single conversion mode is selected by setting bit 1 of control register 0 to 1.

A single conversion is initiated by pulsing the CONVST input. On the falling edge of CONVST, the sample and hold stages of the selected analog inputs are placed into hold simultaneously, and the conversion sequence for the selected channels is started.

The conversion clock in single conversion mode is generated internally using a clock oscillator circuit. The signal DATA_AV (data available) becomes active when the trigger level is reached and indicates that the converted sample(s) is (are) written into the FIFO and can be read out. The trigger level in the single conversion mode can be selected according to Table 13.

Figure 1 shows the timing of the single conversion mode. In this mode, up to four analog input channels can be selected to be sampled simultaneously (see Table 2).

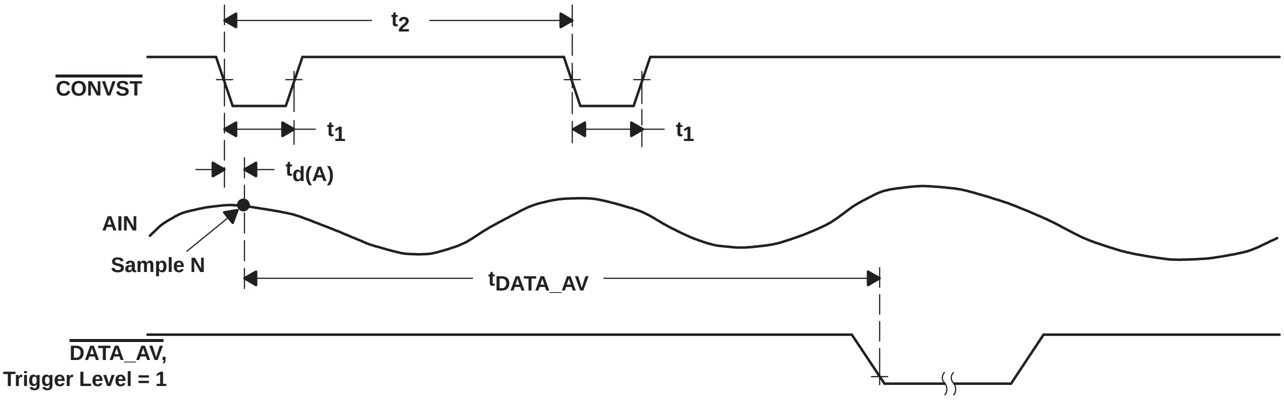


Figure 1. Timing of Single Conversion Mode

The time (t_2) between consecutive starts of single conversions is dependent on the number of selected analog input channels. The time t_{DATA_AV}, until DATA_AV becomes active is given by: $t_{DATA\_AV} = t_{pipe} + n \times t_c$. This equation is valid for a trigger level which is equivalent to the number of selected analog input channels. For all other trigger level conditions refer to the timing specifications of single conversion mode.

continuous conversion mode

The internal clock oscillator used in the single-conversion mode is switched off in continuous conversion mode. In continuous conversion mode, (bit 1 of control register 0 set to 0) the ADC operates with a free running external clock signal CONV_CLK. With every rising edge of the CONV_CLK signal a new converted value is written into the FIFO.

Figure 2 shows the timing of continuous conversion mode when one analog input channel is selected. The maximum throughput rate is 6 MSPS in this mode. The timing of the DATA_AV signal is shown here in the case of a trigger level set to 1 or 4.

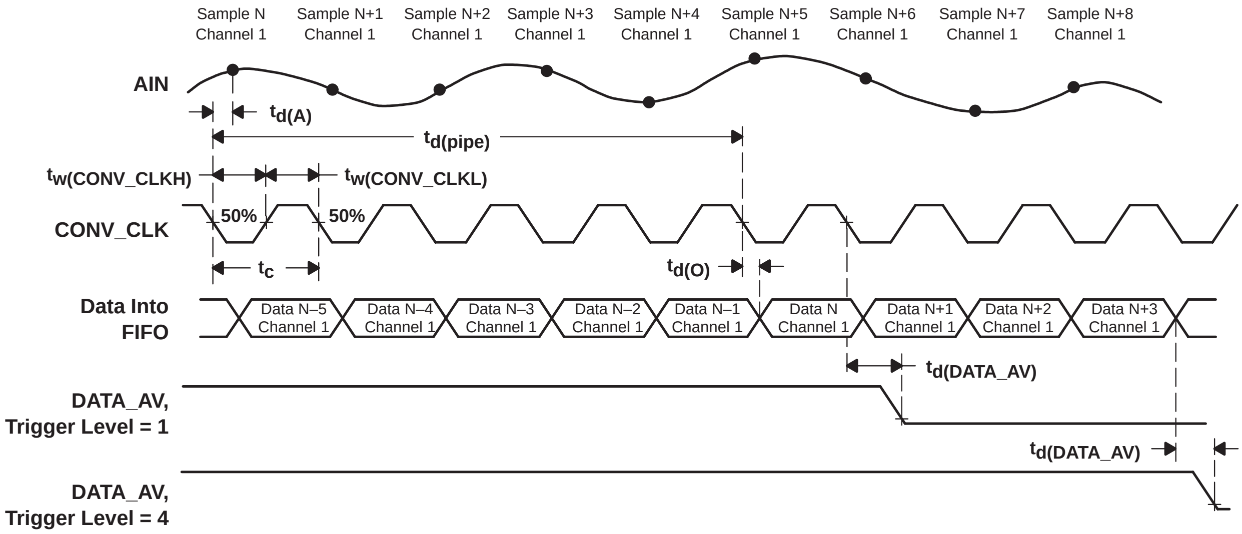


Figure 2. Timing of Continuous Conversion Mode (1-channel operation)

Figure 3 shows the timing of continuous conversion mode when two analog input channels are selected. The maximum throughput rate per channel is 3 MSPS in this mode. The data flow in the bottom of the figure shows the order the converted data is written into the FIFO. The timing of the DATA_AV signal shown here is for a trigger level set to 2 or 4.

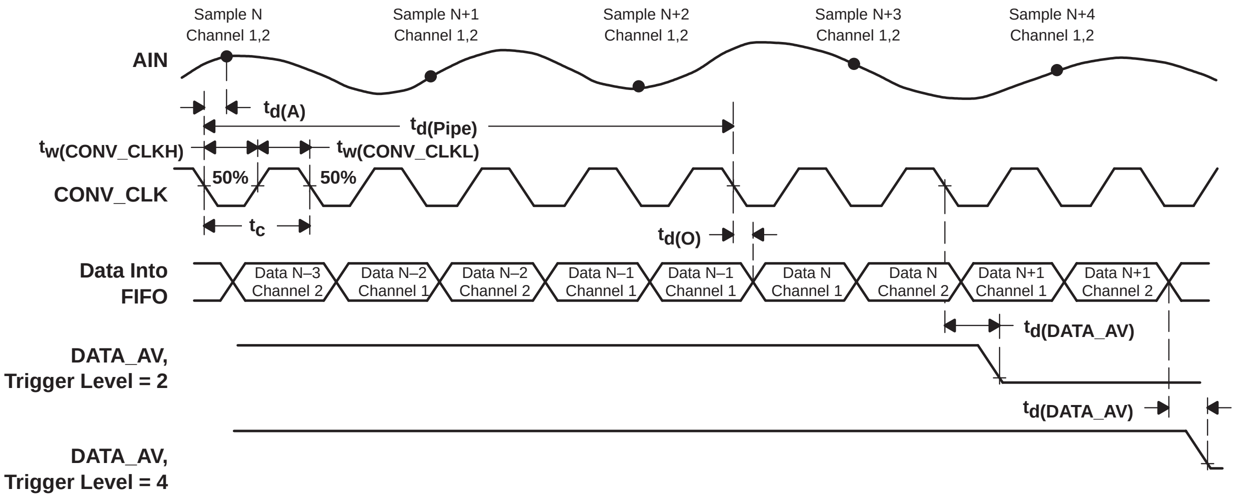


Figure 3. Timing of Continuous Conversion Mode (2-channel operation)

continuous conversion mode (continued)

Figure 4 shows the timing of continuous conversion mode when three analog input channels are selected. The maximum throughput rate per channel is 2 MSPS in this mode. The data flow in the bottom of the figure shows in which order the converted data is written into the FIFO. The timing of the DATA_AV signal shown here is for a trigger level set to 3.

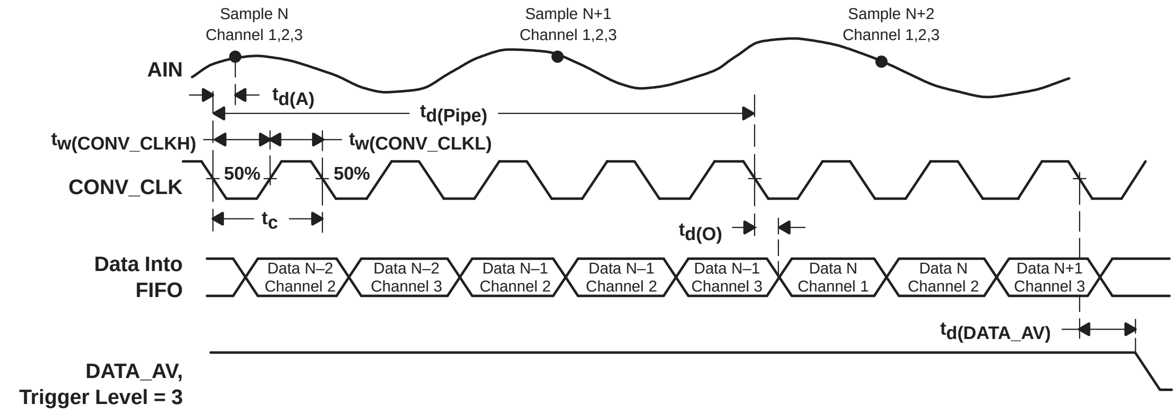


Figure 4. Timing of Continuous Conversion Mode (3-channel operation)

Figure 5 shows the timing of continuous conversion mode when four analog input channels are selected. The maximum throughput rate per channel is 1.5 MSPS in this mode. The data flow in the bottom of the figure shows in which order the converted data is written into the FIFO. The timing of the DATA_AV signal shown here is for a trigger level of 4.

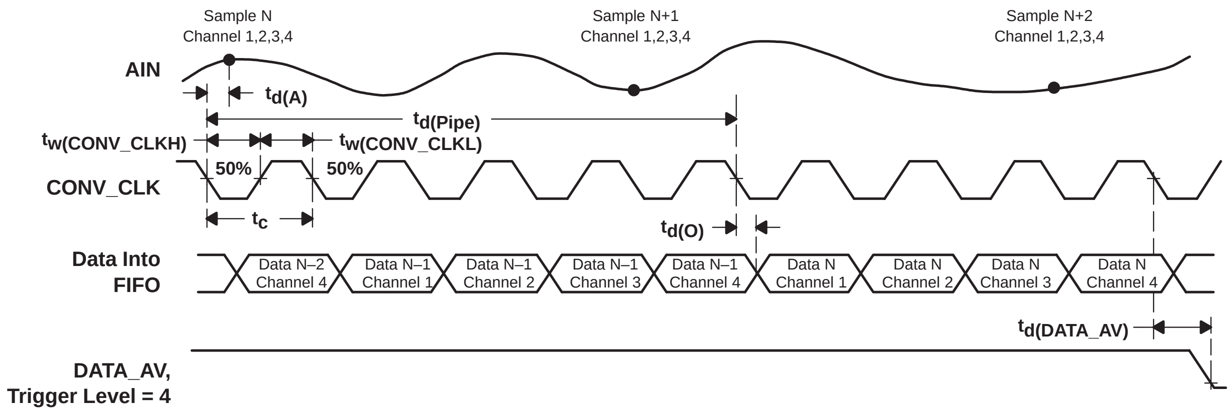


Figure 5. Timing of Continuous Conversion Mode (4-channel operation)

digital output data format

The digital output data format of the THS1206 can either be in binary format or in twos complement format. The following tables list the digital outputs for the analog input voltages.

Table 3. Binary Output Format for Single-Ended Configuration

SINGLE-ENDED, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	**DIGITAL OUTPUT CODE**
AIN = V_{REFP}	FFFh
AIN = $(V_{REFP} + V_{REFM})/2$	800h
AIN = V_{REFM}	000h

Table 4. Two's Complement Output Format for Single-Ended Configuration

SINGLE-ENDED, TWOS COMPLEMENT	
ANALOG INPUT VOLTAGE	**DIGITAL OUTPUT CODE**
AIN = V_{REFP}	7FFh
AIN = $(V_{REFP} + V_{REFM})/2$	000h
AIN = V_{REFM}	800h

Table 5. Binary Output Format for Differential Configuration

DIFFERENTIAL, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	**DIGITAL OUTPUT CODE**
V_{in} = AINP – AINM $V_{REF} = V_{REFP} - V_{REFM}$	
$V_{in} = V_{REF}$	FFFh
$V_{in} = 0$	800h
$V_{in} = -V_{REF}$	000h

Table 6. Two's Complement Output Format for Differential Configuration

DIFFERENTIAL, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	**DIGITAL OUTPUT CODE**
V_{in} = AINP – AINM $V_{REF} = V_{REFP} - V_{REFM}$	
$V_{in} = V_{REF}$	7FFh
$V_{in} = 0$	000h
$V_{in} = -V_{REF}$	800h

FIFO description

In order to facilitate an efficient connection to today's processors, the THS1206 is supplied with a FIFO. This integrated FIFO enables a problem-free processing of data with today's processors. The FIFO is provided as a flexible circular buffer. The circular buffer integrated in the THS1206 can store up to 16 conversion values. Therefore, the amount of interrupts to be served by a processor can be reduced significantly.

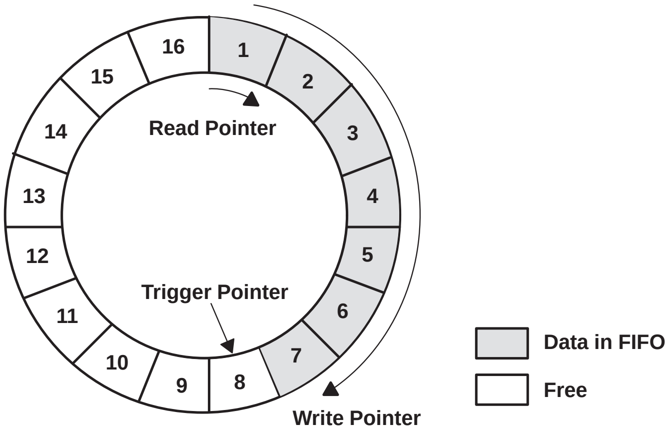


Figure 6. Circular Buffer

The converted data of the THS1206 is automatically written into the FIFO. To control the writing and reading process, a write pointer, a read pointer and a trigger pointer are used. The read pointer always shows the location which will be read next. The write pointer indicates the location which contains the last written sample. With a selection of multiple analog input channels, the converted values are written in a predefined sequence to the circular buffer (Autoscan Mode). In this way, the channel information for the reading processor is continually maintained.

The FIFO can be programmed through the control register of the ADC. The user has the ability to select a specific trigger level according to Table 13 in order to choose the configuration which best fits the application. The FIFO provides the signal DATA_AV, which signals the processor to read the amount of data equal to the trigger level selected in Table 13. The signal DATA_AV becomes active when the trigger condition is satisfied. The trigger condition is satisfied when as many values as selected for the trigger level where written into the FIFO.

The signal DATA_AV could be connected to an interrupt input of a processor. In every interrupt service routine call, the processor must read the amount of data equal to the trigger level from the ADC. The first data represents the first channel according to the autoscan mode, which is shown in Table 10. The channel information is therefore always maintained.

Reading data from the FIFO

The THS1206 informs the connected processor via the digital output DATA_AV (data available) that a block of conversion values are ready to be read. The block size to be read is always equal to the setting of the trigger level. The selectable trigger levels depend on the number of selected analog input channels. For example, when choosing one analog input, a trigger level of 1, 4, 8 and 14 can be selected. The following figures demonstrate the principle of reading the data.

In Figure 7, a trigger level of 1 is selected. The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 1 value from the ADC after every DATA_AV low pulse.

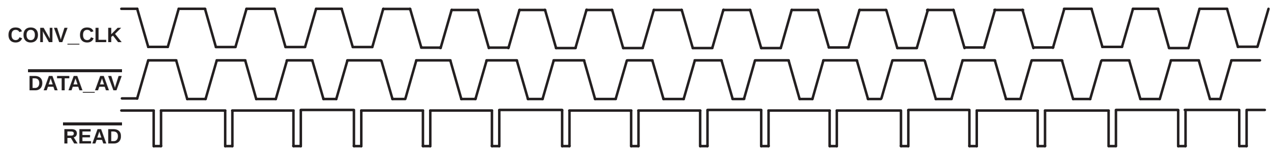


Figure 7. Trigger Level 1 Selected

In Figure 8, a trigger level of 4 is selected. The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 4 values from the ADC after every DATA_AV low pulse.

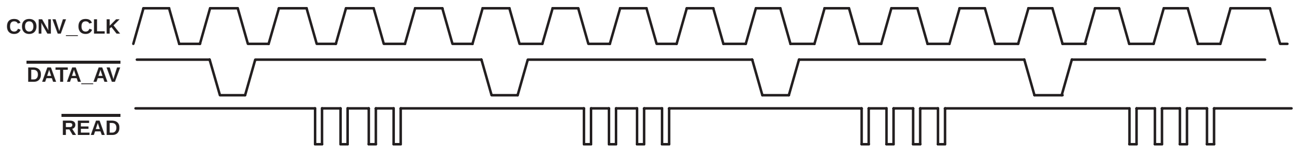


Figure 8. Trigger Level 4 Selected

In Figure 9, a trigger level of 8 is selected. The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 8 values from the ADC after every DATA_AV low pulse.

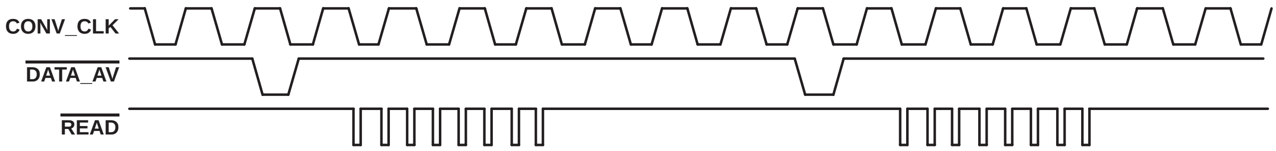


Figure 9. Trigger Level 8 Selected

In Figure 10, a trigger level of 14 is selected. The control signal DATA_AV is set to an active low pulse. This means that the connected processor has the task to read 14 values from the ADC after every DATA_AV low pulse.

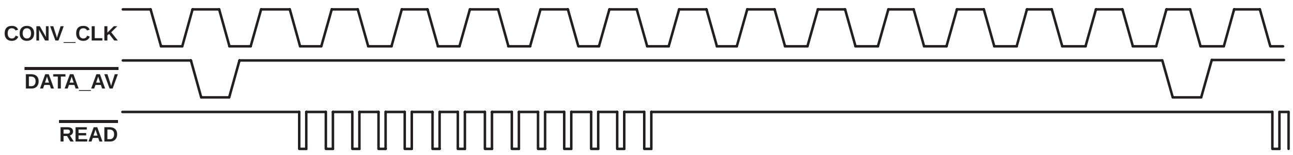


Figure 10. Trigger Level 14 Selected

READ is always the logical combination of $\overline{CS0}$, CS1 and $\overline{RD}$.

ADC Control Register

The THS1206 contains two 10-bit wide control registers (CR0, CR1) in order to program the device into the desired mode. The bit definitions of both control registers are shown in Table 7.

Table 7. Bit Definitions of Control Register CR0 and CR1

BIT	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	MODE	VREF
CR1	RBACK	OFFSET	BIN/2's	R/W	DATA_P	DATA_T	TRIG1	TRIG0	OVFL/FRST	RESET

Writing to control register 0 and control register 1

The 10-bit wide control register 0 and control register 1 can be programmed by addressing the desired control register and writing the register value to the ADC. The addressing is performed with the upper data bits D10 and D11, which function in this case as address lines RA0 and RA1. During this write process, the data bits D0 to D9 contain the desired control register value. Table 8 shows the addressing of each control register.

Table 8. Control Register Addressing

D0 – D9	D10/RA0	D11/RA1	Addressed Control Register
Desired register value	0	0	Control Register 0
Desired register value	1	0	Control Register 1
Desired register value	0	1	Reserved for future
Desired register value	1	1	Reserved for future

initialization of the THS1206

The initialization of the THS1206 should be done according to the configuration flow shown in Figure 11.

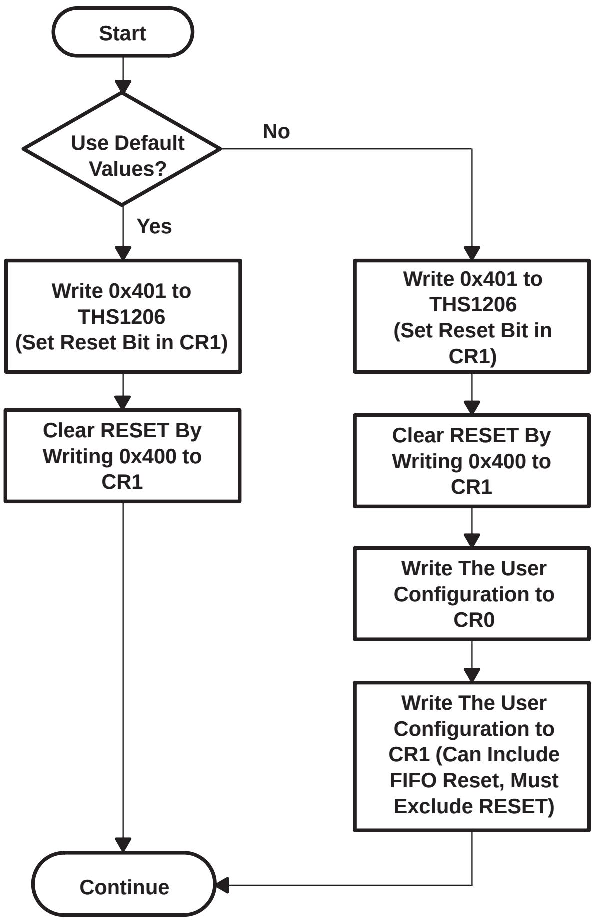


Figure 11. THS1206 Configuration Flow

ADC control registers

control register 0 (see Table 8)

–	–	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
–	–	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	MODE	VREF

Table 9. Control Register 0 Bit Functions

BITS	RESET VALUE	NAME	FUNCTION
0	0	VREF	Vref select: Bit 0 = 0 → The internal reference is selected Bit 0 = 1 → The external reference voltage is selected
1	0	MODE	Continuous conversion mode/single conversion mode Bit 1 = 0 → Continuous conversion mode is selected An external clock signal is applied to the CONV_CLK input in this mode. With every falling edge of the CONV_CLK signal a new converted value is written into the FIFO. Bit 1 = 1 → Single conversion mode is selected In this mode, the CONV_CLK input functions as a $\overline{\text{CONVST}}$ input. A single conversion is initiated on the THS1206 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the sample and hold stages of the selected analog inputs are placed into hold simultaneously, and the conversion sequence for the selected channels is started. The signal DATA_AV (data available) becomes active when the trigger condition is satisfied.
2	0	PD	Power down. Bit 2 = 0 → The ADC is active Bit 2 = 1 → Power down The reading and writing to and from the digital outputs is possible during power down. It is also possible to read out the FIFO.
3, 4	0,0	CHSEL0, CHSEL1	Channel select Bit 3 and bit 4 select the analog input channel of the ADC. Refer to Table 10.
5,6	1,0	DIFF0, DIFF1	Number of differential channels Bit 5 and bit 6 contain information about the number of selected differential channels. Refer to Table 10.
7	0	SCAN	Autoscan enable Bit 7 enables or disables the autoscan function of the ADC. Refer to Table 10.
8,9	0,0	TEST0, TEST1	Test input enable Bit 8 and bit 9 control the test function of the ADC. Three different test voltages can be measured. This feedback allows the check of all hardware connections and the ADC operation. Refer to Table 11 for selection of the three different test voltages.

analog input channel selection

The analog input channels of the THS1206 can be selected via bits 3 to 7 of control register 0. One single channel (single-ended or differential) is selected via bit 3 and bit 4 of control register 0. Bit 5 controls the selection between single-ended and differential configuration. Bit 6 and bit 7 select the autoscan mode, if more than one input channel is selected. Table 10 shows the possible selections.

Table 10. Analog Input Channel Configurations

BIT 7 SCAN	BIT 6 DIFF1	BIT 5 DIFF0	BIT 4 CHSEL1	BIT 3 CHSEL0	DESCRIPTION OF THE SELECTED INPUTS
0	0	0	0	0	Analog input AINP (single ended)
0	0	0	0	1	Analog input AINM (single ended)
0	0	0	1	0	Analog input BINP (single ended)
0	0	0	1	1	Analog input BINM (single ended)
0	0	1	0	0	Differential channel (AINP–AINM)
0	0	1	0	1	Differential channel (BINP–BINM)
1	0	0	0	1	Autoscan two single ended channels: AINP, AINM, AINP, …
1	0	0	1	0	Autoscan three single ended channels: AINP, AINM, BINP, AINP, …
1	0	0	1	1	Autoscan four single ended channels: AINP, AINM, BINP, BINM, AINP, …
1	0	1	0	1	Autoscan one differential channel and one single ended channel AINP, (BINP–BINM), AINP, (BINP–BINM), …
1	0	1	1	0	Autoscan one differential channel and two single ended channel AINP, AINM, (BINP–BINM), AINP, …
1	1	0	0	1	Autoscan two differential channels (AINP–AINM), (BINP–BINM), (AINP–AINM), …
0	0	1	1	0	Reserved
0	0	1	1	1	Reserved
1	0	0	0	0	Reserved
1	0	1	0	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

analog input channel selection (continued)

test mode

The test mode of the ADC is selected via bit 8 and bit 9 of control register 0. The different selections are shown in Table 11.

Table 11. Test Mode

BIT 9 TEST1	BIT 8 TEST0	OUTPUT RESULT
0	0	Normal mode
0	1	V_{REFP}
1	0	$((V_{REFM})+(V_{REFP}))/2$
1	1	V_{REFM}

Three different options can be selected. This feature allows support testing of hardware connections between the ADC and the processor.

analog input channel selection (continued)

control register 1 (see Table 8)

–	–	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
–	–	RBACK	OFFSET	BIN/2s	R/$\overline{\text{W}}$	DATA_P	DATA_T	TRIG1	TRIG0	OVFL/FRST	RESET

Table 12. Control Register 1 Bit Functions

BITS	RESET VALUE	NAME	FUNCTION
0	0	RESET	Reset Writing a 1 into this bit resets the device and sets the control register 0 and control register 1 to the reset values. In addition the FIFO pointer and offset register is reset. After reset, it takes 5 clock cycles until the first value is converted and written into the FIFO.
1	0	OVFL (read only) FRST (write only)	Overflow flag (read only) Bit 1 of control register 1 indicates an overflow in the FIFO. Bit 1 = 0 → no overflow occurred. Bit 1 = 1 → an overflow occurred. This bit is reset to 0, after this control register is read from the processor. FRST: FIFO reset (write only) By writing a 1 into this bit, the FIFO is reset.
2, 3	0,0	TRIG0, TRIG1	FIFO trigger level Bit 2 and bit 3 of control register 1 are used to set the trigger level for the FIFO. If the trigger level is reached, the signal DATA_AV (data available) becomes active according to the settings of DATA_T and DATA_P. This indicates to the processor that the ADC values can be read. Refer to Table 13.
4	1	DATA_T	DATA_AV type Bit 4 of control register 1 controls whether the DATA_AV signal is a pulse or static (e.g for edge or level sensitive interrupt inputs). If it is set to 0, the DATA_AV signal is static. If it is set to 1, the DATA_AV signal is a pulse. Refer to Table 14.
5	1	DATA_P	DATA_AV polarity Bit 5 of control register 1 controls the polarity of DATA_AV. If it is set to 1, DATA_AV is active high. If it is set to 0, DATA_AV is active low. Refer to Table 14.
6	0	R/$\overline{\text{W}}$	R/$\overline{\text{W}}$, RD/$\overline{\text{WR}}$ selection Bit 6 of control register 1 controls the function of the inputs $\overline{\text{RD}}$ and $\overline{\text{WR}}$. When bit 6 in control register 1 is set to 1, $\overline{\text{WR}}$ becomes a R/$\overline{\text{W}}$ input and $\overline{\text{RD}}$ is disabled. From now on a read is signalled with R/W high and a write with R/W as a low signal. If bit 6 in control register 1 is set to 0, the input $\overline{\text{RD}}$ becomes a read input and the input $\overline{\text{WR}}$ becomes a write input.
7	0	BIN/2s	Complement select If bit 7 of control register 1 is set to 0, the output value of the ADC is in twos complement. If bit 7 of control register 1 is set to 1, the output value of the ADC is in binary format. Refer to Table 3 through Table 6.
8	0	OFFSET	Offset cancellation mode Bit 8 = 0 → normal conversion mode Bit 8 = 1 → offset calibration mode If a 1 is written into bit 8 of control register 1, the device internally sets the inputs to zero and does a conversion. The conversion result is stored in an offset register and subtracted from all conversions in order to reduce the offset error.
9	0	RBACK	Debug mode Bit 9 = 0 → normal conversion mode Bit 9 = 1 → enable debug mode When bit 9 of control register 1 is set to 1, debug mode is enabled. In this mode, the contents of control register 0 and control register 1 can be read back. The first read after bit 9 is set to 1 contains the value of control register 0. The second read after bit 9 is set to 1 contains the value of control register 1.

FIFO trigger level

Bit 2 and bit 3 (TRIG1, TRIG0) of control register 1 are used to set the trigger level of the FIFO (see Table 13). If the trigger level is reached, the DATA_AV (data available) signal becomes active according to the setting of the signal DATA_AV to indicate to the processor that the ADC values can be read.

Table 13 shows four different programmable trigger levels for each configuration. The FIFO trigger level, which can be selected, is dependent on the number of input channels. Both, a differential or a single-ended input is considered as one channel. The processor therefore always reads the data from the FIFO in the same order and is able to distinguish between the channels.

Table 13. FIFO Trigger Level

BIT 3 TRIG1	BIT 2 TRIG0	TRIGGER LEVEL FOR 1 CHANNEL (ADC values)	TRIGGER LEVEL FOR 2 CHANNELS (ADC values)	TRIGGER LEVEL FOR 3 CHANNEL (ADC values)	TRIGGER LEVEL FOR 4 CHANNELS (ADC values)
0	0	01	02	03	04
0	1	04	04	06	08
1	0	08	08	09	12
1	1	14	12	12	Reserved

Timing and Signal Description of the THS1206

The reading from the THS1206 and writing to the THS1206 is perfomed by using the chip select inputs ($\overline{\text{CS0}}$, CS1), the write input $\overline{\text{WR}}$ and the read input $\overline{\text{RD}}$. The write input is configurable to a combined read/write input (R/$\overline{\text{W}}$). This is desired in cases where the connected processor consists of a combined read/write ouput signal (R/$\overline{\text{W}}$). The two chip select inputs can be used to interface easily to a processor.

Reading from the THS1206 takes place by an internal $\overline{\text{RD}}_{int}$ signal, which is generated from the logical combination of the external signals $\overline{\text{CS0}}$, CS1 and $\overline{\text{RD}}$ (see Figure 12). This signal is then used to strobe the words out of the FIFO and to enable the output buffers. The last external signal (either $\overline{\text{CS0}}$, CS1 or $\overline{\text{RD}}$) to become valid will make $\overline{\text{RD}}_{int}$ active while the write input ($\overline{\text{WR}}$) is inactive. The first of those external signals going to its inactive state will then deactivate $\overline{\text{RD}}_{int}$ again.

Writing to the THS1206 takes place by an internal $\overline{\text{WR}}_{int}$ signal, which is generated from the logical combination of the external signals $\overline{\text{CS0}}$, CS1 and $\overline{\text{WR}}$. This signal is then used to strobe the control words into the control registers 0 and 1. The last external signal (either $\overline{\text{CS0}}$, CS1 or $\overline{\text{WR}}$) to become valid will make $\overline{\text{WR}}_{int}$ active while the read input (RD) is inactive. The first of those external signals going to its inactive state will then deactivate $\overline{\text{WR}}_{int}$ again.

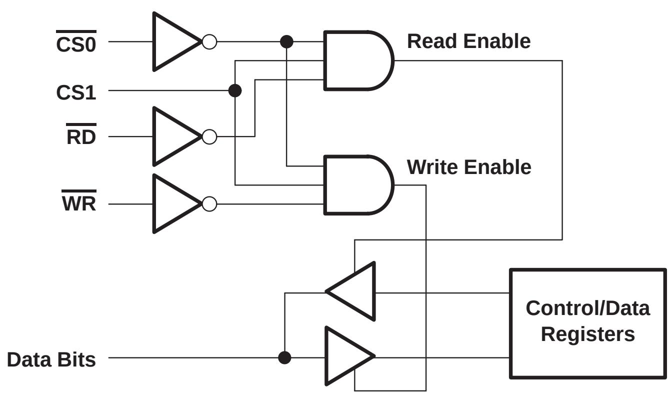


Figure 12. Logical Combination of $\overline{\text{CS0}}$, CS1, $\overline{\text{RD}}$, and $\overline{\text{WR}}$

DATA_AV type

Bit 4 and bit 5 (DATA_T, DATA_P) of control register 1 are used to program the signal DATA_AV. Bit 4 of control register 1 determines whether the DATA_AV signal is static or a pulse. Bit 5 of the control register determines the polarity of DATA_AV. This is shown in Table 14.

Table 14. DATA_AV Type

BIT 5 DATA_P	BIT 4 DATA_T	DATA_AV TYPE
0	0	Active low level
0	1	Active low pulse
1	0	Active high level
1	1	Active high pulse

The signal DATA_AV is set to active when the trigger condition is satisified. It is set back inactive independent of the DATA_T selection (pulse or level).

If level mode is chosen, DATA_AV is set inactive after the first of the TL (TL = trigger level) reads (with the falling edge of READ). The trigger condition is checked again after TL reads.

If pulse mode is chosen, the signal DATA_AV is a pulse with a width of one half of a CONV_CLK cycle in continuous conversion mode and one half of a clock cycle of the internal oscillator in single conversion mode. The next DATA_AV pulse (when the trigger condition is satisfied) is sent out the earliest, when the TL values, written into the FIFO before, were read out by the processor.

timing and signal description of the THS1206

read timing (using R/$\overline{\text{W}}$, $\overline{\text{CS0}}$-controlled)

Figure 13 shows the read-timing behavior when the $\overline{\text{WR}}$(R/$\overline{\text{W}}$) input is programmed as a combined read-write input R/$\overline{\text{W}}$. The $\overline{\text{RD}}$ input has to be tied to high-level in this configuration. This timing is called $\overline{\text{CS0}}$-controlled because $\overline{\text{CS0}}$ is the last external signal of $\overline{\text{CS0}}$, CS1, and R/$\overline{\text{W}}$ which becomes valid.

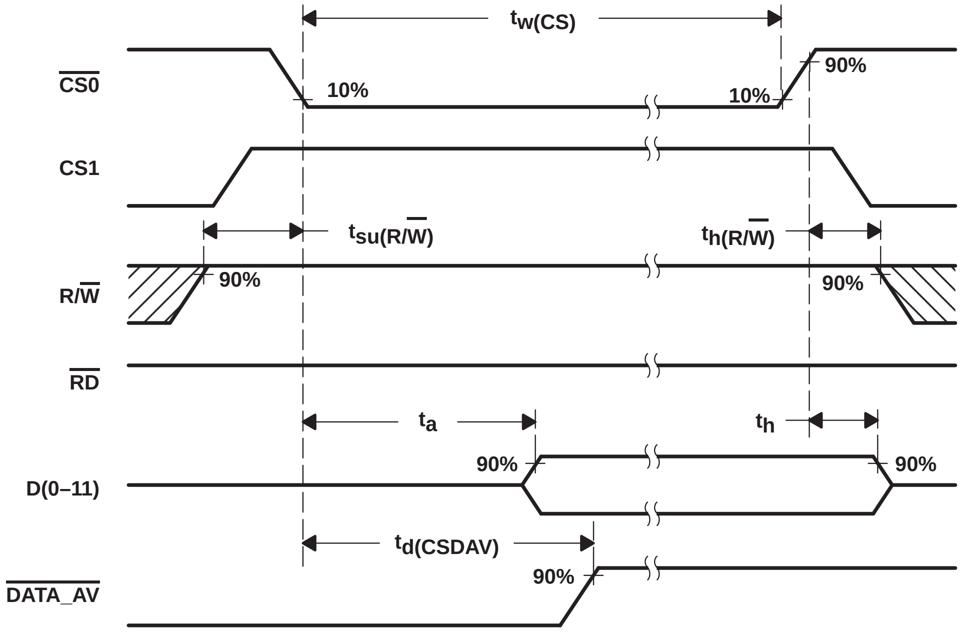


Figure 13. Read Timing Diagram Using R/$\overline{\text{W}}$ ($\overline{\text{CS0}}$-controlled)

read timing parameter ($\overline{\text{CS0}}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(R/\overline{W})}$	Setup time, R/$\overline{\text{W}}$ high to last CS valid	0			ns
t_a	Access time, last CS valid to data valid	0		10	ns
$t_{d(CSDAV)}$	Delay time, last CS valid to DATA_AV inactive		12		ns
t_h	Hold time, first CS invalid to data invalid	0		5	ns
$t_{h(R/\overline{W})}$	Hold time, first external CS invalid to R/$\overline{\text{W}}$ change	5			ns
$t_{w(CS)}$	Pulse duration, CS active	10			ns

timing and signal description of the THS1206 (continued)

write timing (using R/$\overline{W}$, $\overline{CS0}$-controlled)

Figure 14 shows the write-timing behavior when the $\overline{WR}$(R/$\overline{W}$) input is programmed as a combined read-write input R/$\overline{W}$. The $\overline{RD}$ input has to be tied to high-level in this configuration. This timing is called $\overline{CS0}$-controlled because $\overline{CS0}$ is the last external signal of $\overline{CS0}$, CS1, and R/$\overline{W}$ which becomes valid.

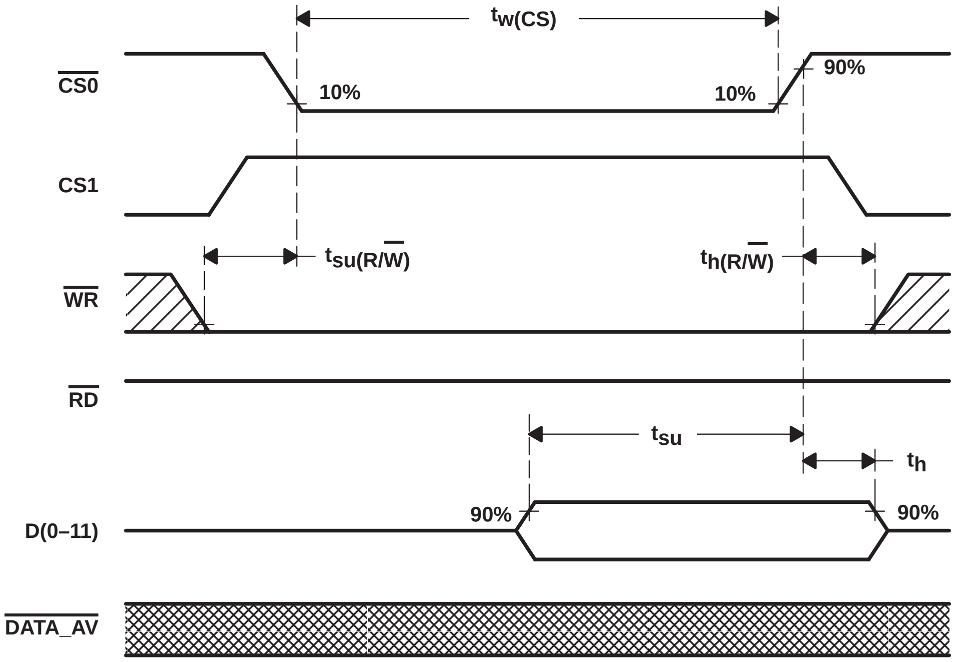


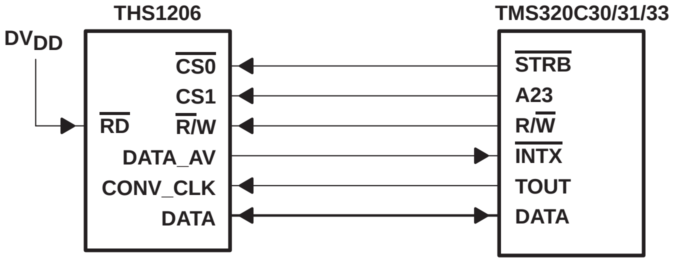
Figure 14. Write Timing Diagram Using R/$\overline{W}$ ($\overline{CS0}$-controlled)

write timing parameter ($\overline{RD}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(R/\overline{W})}$	Setup time, R/$\overline{W}$ stable to last CS valid	0			ns
t_{su}	Setup time, data valid to first CS invalid	5			ns
t_h	Hold time, first CS invalid to data invalid	5			ns
$t_{h(R/\overline{W})}$	Hold time, first CS invalid to R/$\overline{W}$ change	5			ns
$t_{w(CS)}$	Pulse duration, CS active	10			ns

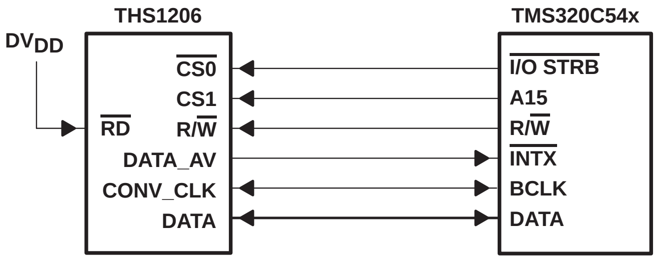
interfacing the THS1206 to the TMS320C30/31/33 DSP

The following application circuit shows an interface of the THS1206 to the TMS320C30/31/33 DSPs. The read and write timings (using R/$\overline{W}$, $\overline{CS0}$-controlled) shown before are valid for this specific interface.



interfacing the THS1206 to the TMS320C54x using I/O strobe

The following application circuit shows an interface of the THS1206 to the TMS320C54x. The read and write timings (using R/$\overline{W}$, $\overline{CS0}$-controlled) shown before are valid for this specific interface.



timing and signal description of the THS1206 (continued)

read timing (using $\overline{RD}$, $\overline{RD}$-controlled)

Figure 15 shows the read-timing behavior when the $\overline{WR}$(R/$\overline{W}$) input is programmed as a write-input only. The input $\overline{RD}$ acts as the read-input in this configuration. This timing is called $\overline{RD}$-controlled because $\overline{RD}$ is the last external signal of $\overline{CS0}$, CS1, and $\overline{RD}$ which becomes valid.

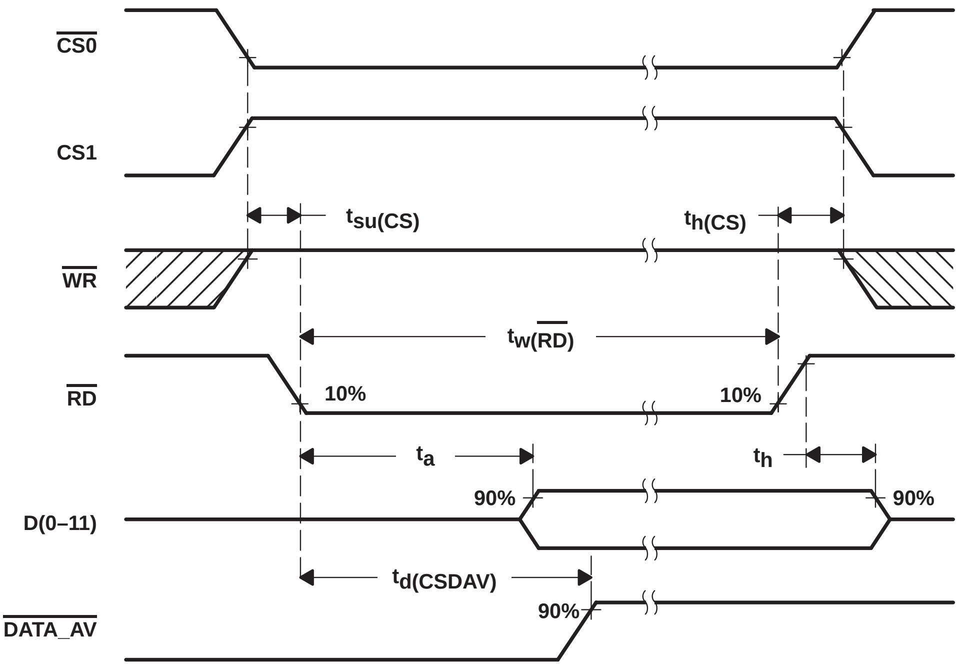


Figure 15. Read Timing Diagram Using $\overline{RD}$ ($\overline{RD}$-controlled)

read timing parameter ($\overline{RD}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(CS)}$	Setup time, $\overline{RD}$ low to last CS valid	0			ns
t_a	Access time, last CS valid to data valid	0		10	ns
$t_{d(CSDAV)}$	Delay time, last CS valid to DATA_AV inactive		12		ns
t_h	Hold time, first CS invalid to data invalid	0		5	ns
$t_{h(CS)}$	Hold time, $\overline{RD}$ change to first CS invalid	5			ns
$t_{w(\overline{RD})}$	Pulse duration, $\overline{RD}$ active	10			ns

timing and signal description of the THS1206 (continued)

write timing (using $\overline{WR}$, $\overline{WR}$-controlled)

Figure 16 shows the write-timing behavior when the $\overline{WR}$(R/$\overline{W}$) input is programmed as a write input $\overline{WR}$ only. The input $\overline{RD}$ acts as the read input in this configuration. This timing is called $\overline{WR}$-controlled because $\overline{WR}$ is the last external signal of $\overline{CS0}$, CS1, and $\overline{WR}$ which becomes valid.

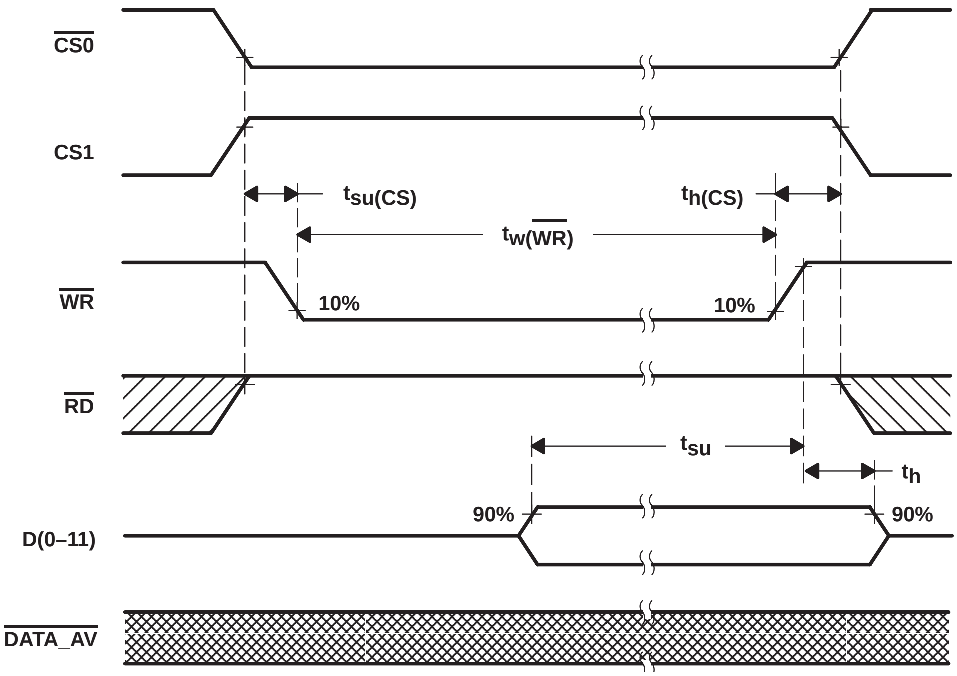


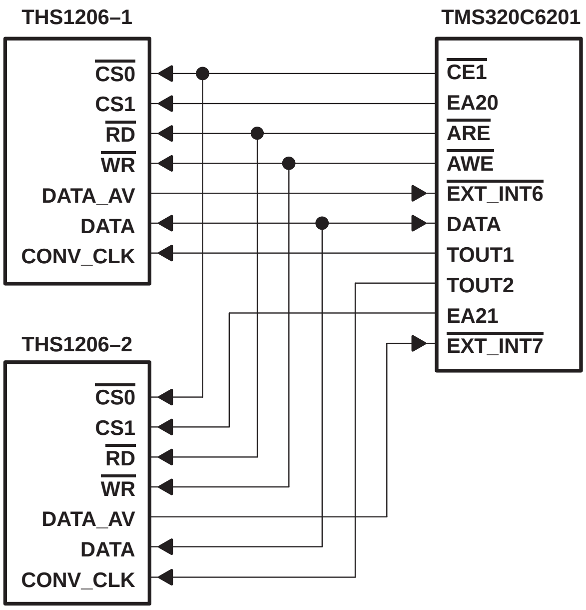
Figure 16. Write Timing Diagram Using $\overline{WR}$ ($\overline{WR}$-controlled)

write timing parameter using $\overline{WR}$ ($\overline{WR}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(CS)}$	Setup time, CS stable to last $\overline{WR}$ valid	0			ns
t_{su}	Setup time, data valid to first $\overline{WR}$ invalid	5			ns
t_h	Hold time, $\overline{WR}$ invalid to data invalid	5			ns
$t_{h(CS)}$	Hold time, $\overline{WR}$ invalid to CS change	5			ns
$t_{w(\overline{WR})}$	Pulse duration, $\overline{WR}$ active	10			ns

interfacing the THS1206 to the TMS320C6201 DSP

The following application circuit shows an interface of the THS1206 to the TMS320C6201. The read (using $\overline{RD}$, $\overline{RD}$-controlled) and write timings (using $\overline{WR}$, $\overline{WR}$-controlled) shown before are valid for this specific interface.



analog input configuration and reference voltage

The THS1206 features four analog input channels. These can be configured for either single-ended or differential operation. Best performance is achieved in differential mode. Figure 17 shows a simplified model, where a single-ended configuration for channel AINP is selected. The reference voltages for the ADC itself are V_{REFP} and V_{REFM} (either internal or exteral reference voltage). The analog input voltage range goes from V_{REFM} to V_{REFP}. This means that V_{REFM} defines the minimum voltage, which can be applied to the ADC. V_{REFP} defines the maximum voltage, which can be applied to the ADC. The internal reference source provides the voltage V_{REFM} of 1.5 V and the voltage V_{REFP} of 3.5 V. The resulting analog input voltage swing of 2 V can be expressed by:

$$V_{REFM} \le AINP \le V_{REFP} \tag{1}$$

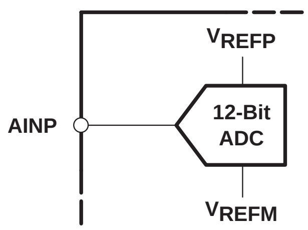


Figure 17. Single-Ended Input Stage

analog input configuration and reference voltage (continued)

A differential operation is desired for many applications. Figure 18 shows a simplified model for the analog inputs AINM and AINP, which are configured for differential operation. This configuration has a few advantages, which are discussed in the following paragraphs.

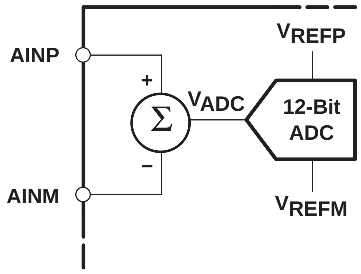


Figure 18. Differential Input Stage

In comparison to the single-ended configuration it can be seen that the voltage, V_{ADC}, which is applied at the input of the ADC is the difference between the input AINP and AINM. This means that V_{REFM} defines the minimum voltage (V_{ADC}) which can be applied to the ADC. V_{REFP} defines the maximum voltage (VADC) which can be applied to the ADC. The voltage V_{ADC} can be calculated as follows:

$$V_{ADC} = ABS(AINP–AINM) \qquad (2)$$

An advantage to single-ended operation is that the common-mode voltage

$$V_{CM} = \frac{AINM + AINP}{2} \qquad (3)$$

can be rejected in the differential configuration, if the following condition for the analog input voltages is true:

$$AGND \le AINM,\ AINP \le AV_{DD} \qquad (4)$$

$$1\ V \le V_{CM} \le 4\ V \qquad (5)$$

In addition to the common-mode voltage rejection, the differential operation allows a dc-offset rejection which is common to both analog inputs. See also Figure 20.

single-ended mode of operation

The THS1206 can be configured for single-ended operation using dc or ac coupling. In either case, the input of the THS1206 must be driven from an operational amplifier that does not degrade the ADC performance. Because the THS1206 operates from a 5-V single supply, it is necessary to level-shift ground-based bipolar signals to comply with its input requirements. This can be achieved with dc and ac coupling. An application example is shown for dc-coupled level shifting in the following section, dc coupling.

dc coupling

An operational amplifier can be configured to shift the signal level according to the analog input voltage range of the THS1206. The analog input voltage range of the THS1206 goes from 1.5 V to 3.5 V. An op-amp specified for 5-V single supply can be used as shown in Figure 19.

Figure 19 shows an application example where the analog input signal in the range from –1 V up to 1 V is shifted by an op-amp to the analog input range of the THS1206 (1.5 V to 3.5 V). The op-amp is configured as an inverting amplifier with a gain of –1. The required dc voltage of 1.25 V at the noninverting input is derived from the 2.5-V output reference REFOUT of the THS1206 by using a resistor divider. Therefore, the op-amp output voltage is centered at 2.5 V. The use of ratio matched, thin-film resistor networks minimizes gain and offset errors.

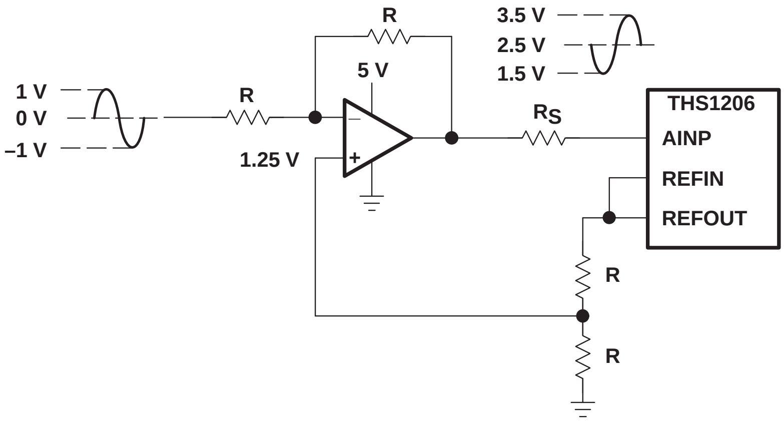


Figure 19. Level-Shift for DC-Coupled Input

differential mode of operation

For the differential mode of operation, a conversion from single-ended to differential is required. A conversion to differential signals can be achieved by using an RF-transformer, which provides a center tap. Best performance is achieved in differential mode.

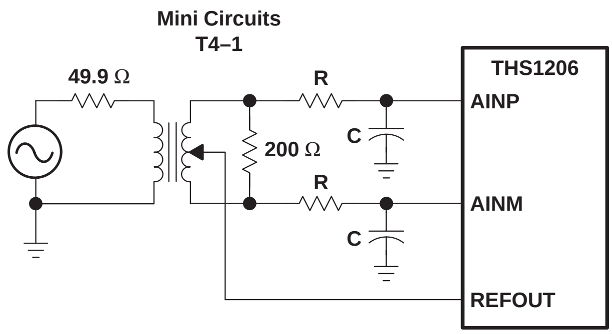


Figure 20. Transformer Coupled Input

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs SAMPLING FREQUENCY (SINGLE-ENDED)

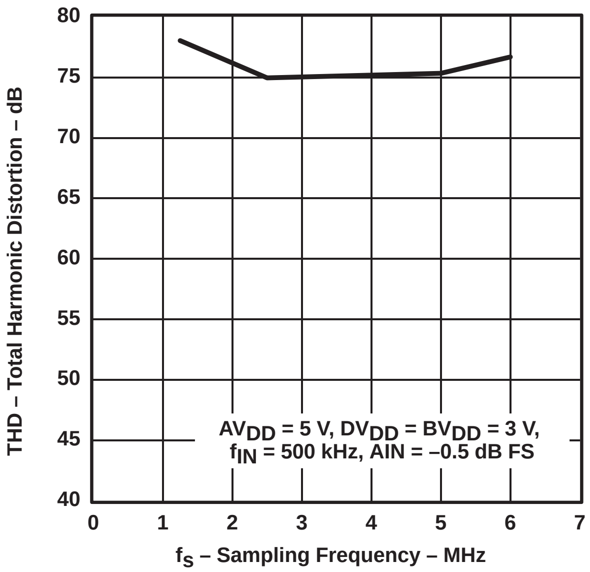


Figure 21

SIGNAL-TO-NOISE AND DISTORTION vs SAMPLING FREQUENCY (SINGLE-ENDED)

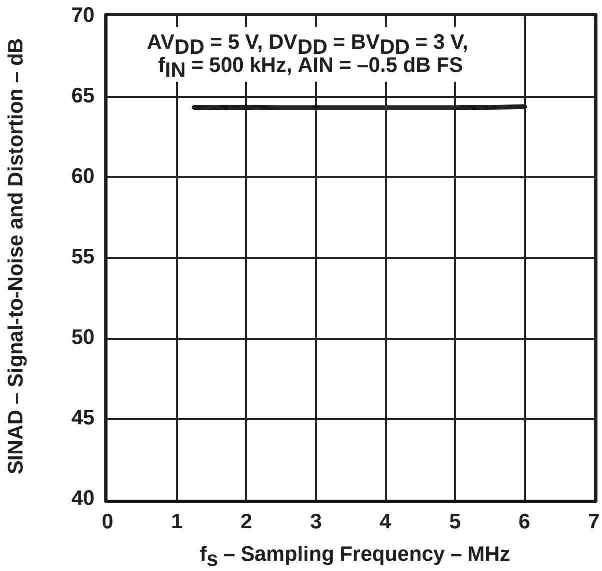


Figure 22

SPURIOUS FREE DYNAMIC RANGE vs SAMPLING FREQUENCY (SINGLE-ENDED)

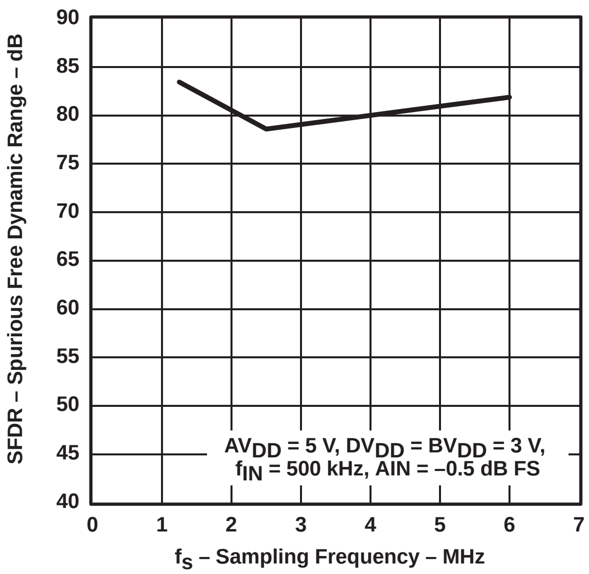


Figure 23

SIGNAL-TO-NOISE vs SAMPLING FREQUENCY (SINGLE-ENDED)

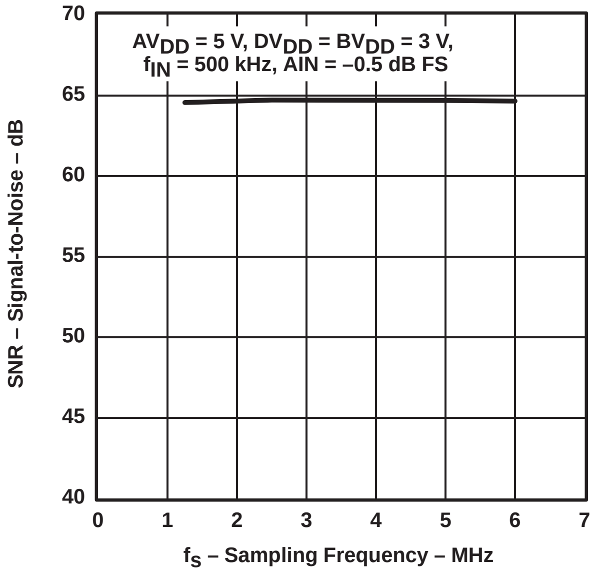


Figure 24

TYPICAL CHARACTERISTICS

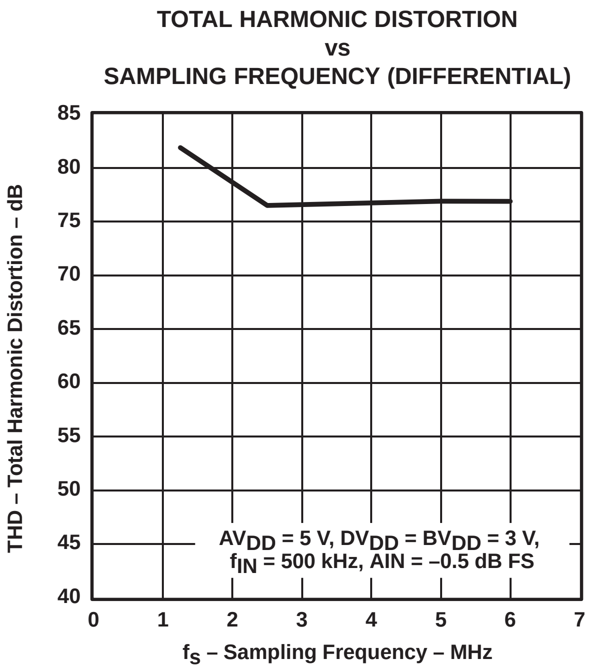


Figure 25

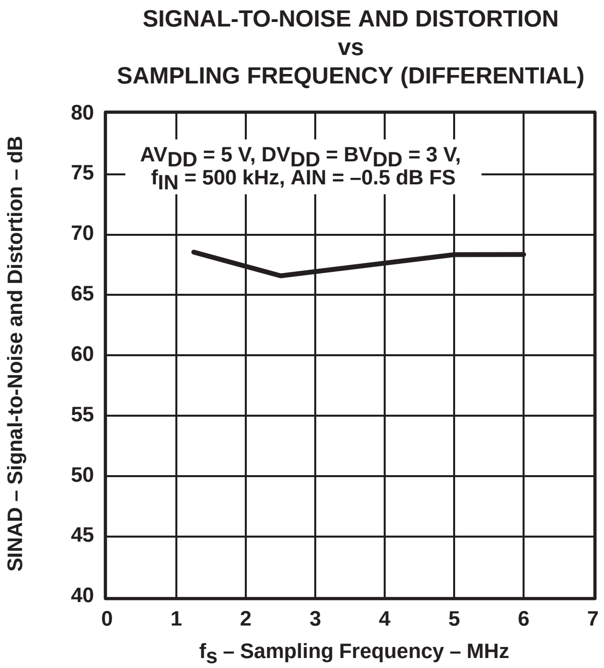


Figure 26

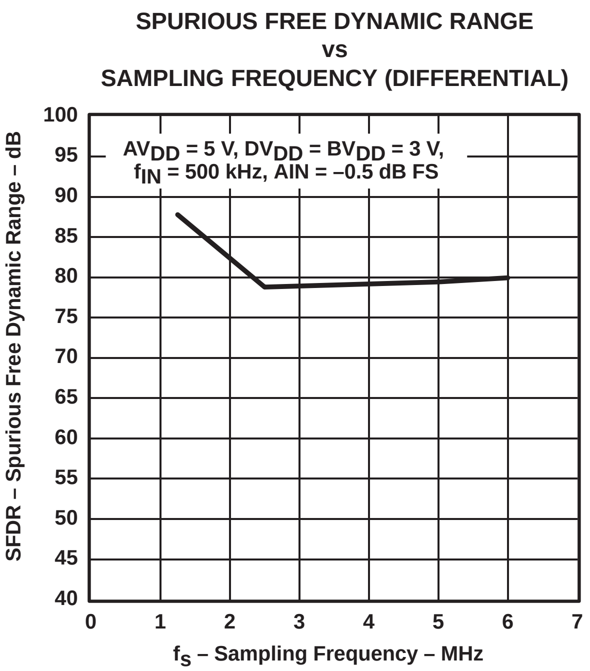


Figure 27

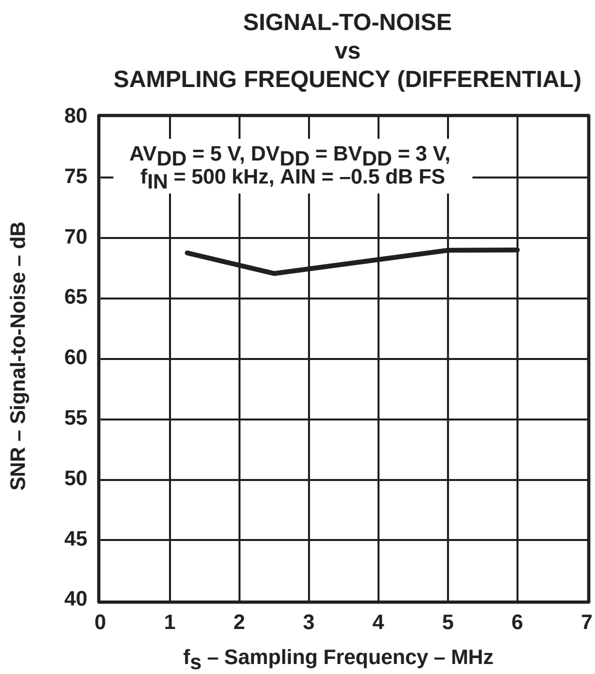


Figure 28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY (SINGLE-ENDED)

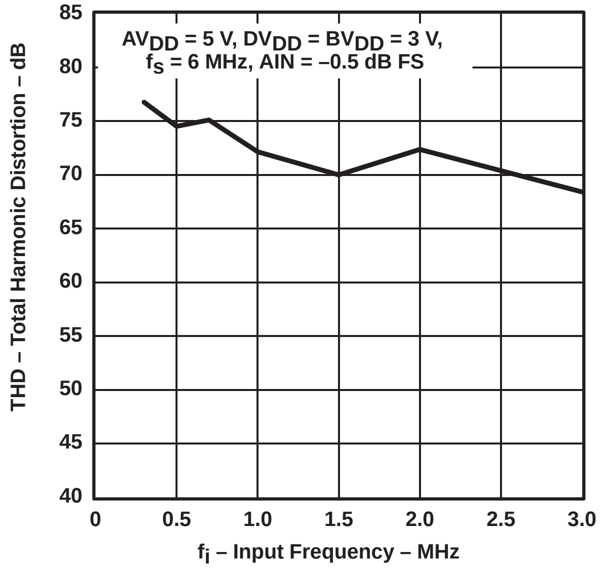


Figure 29

SIGNAL-TO-NOISE AND DISTORTION
vs
INPUT FREQUENCY (SINGLE-ENDED)

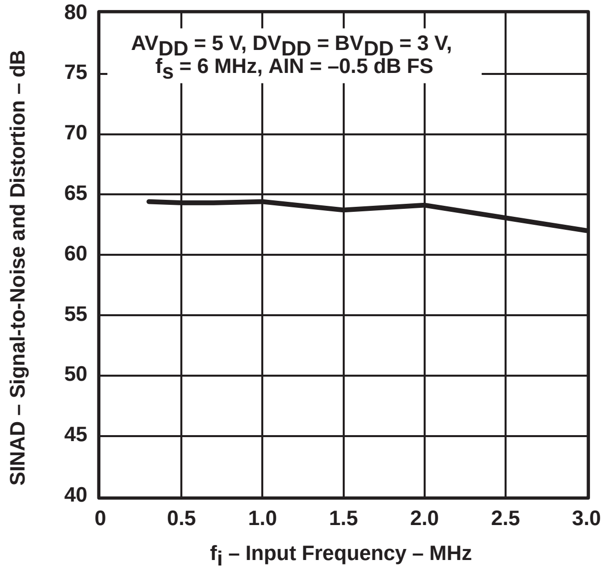


Figure 30

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY (SINGLE-ENDED)

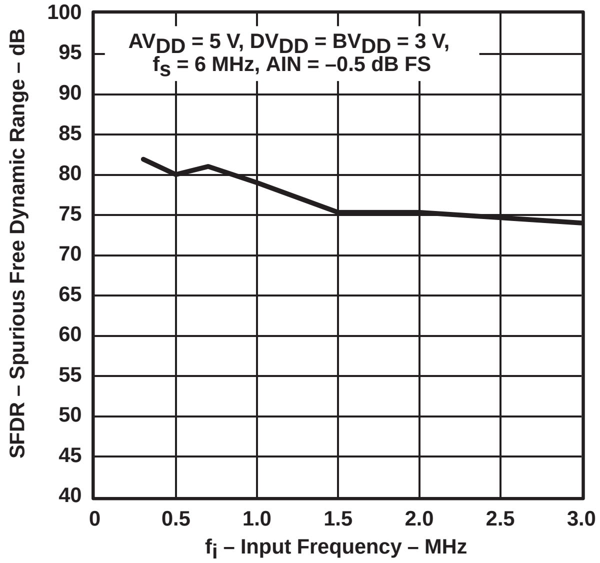


Figure 31

SIGNAL-TO-NOISE
vs
INPUT FREQUENCY (SINGLE-ENDED)

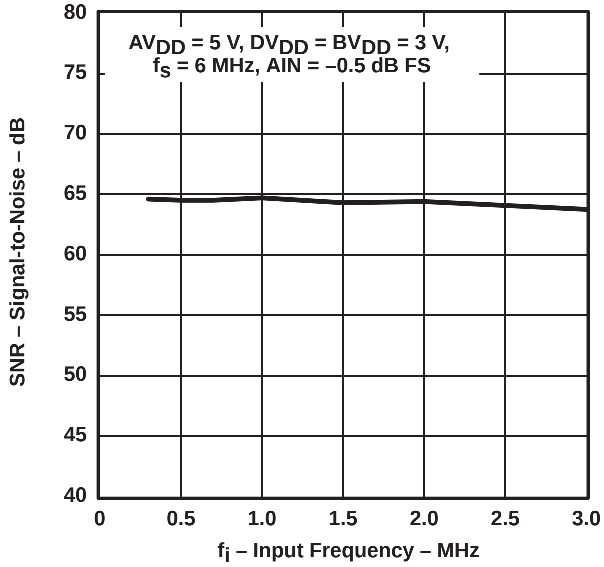


Figure 32

TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY (DIFFERENTIAL)**

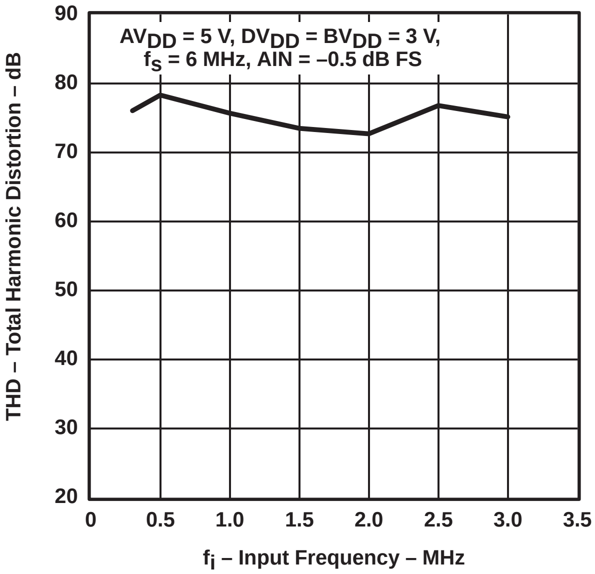


Figure 33

**SIGNAL-TO-NOISE AND DISTORTION
vs
INPUT FREQUENCY (DIFFERENTIAL)**

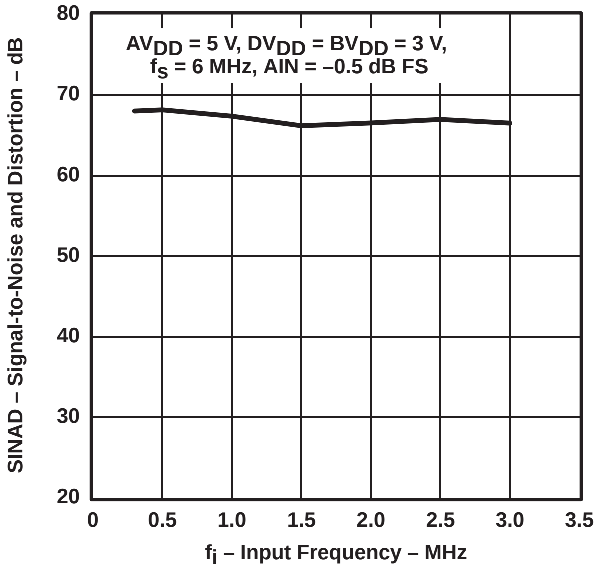


Figure 34

**SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY (DIFFERENTIAL)**

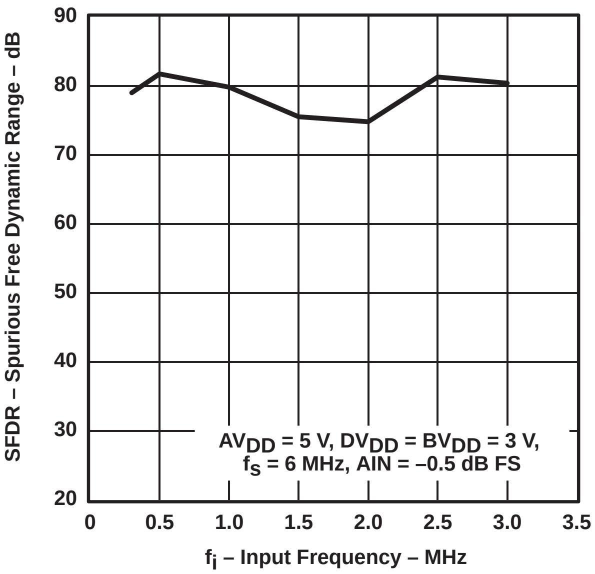


Figure 35

**SIGNAL-TO-NOISE
vs
INPUT FREQUENCY (DIFFERENTIAL)**

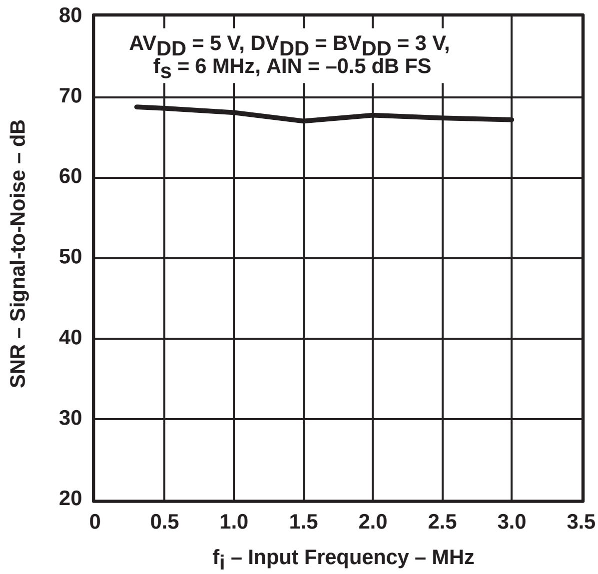


Figure 36

TYPICAL CHARACTERISTICS

EFFECTIVE NUMBER OF BITS
vs
SAMPLING FREQUENCY (SINGLE-ENDED)

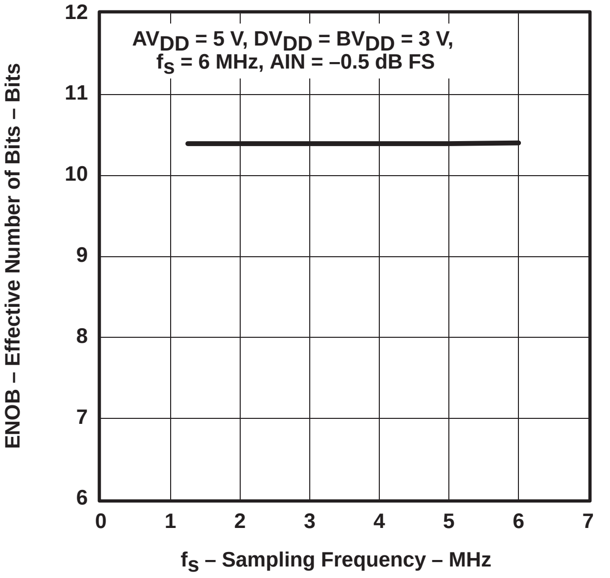


Figure 37

EFFECTIVE NUMBER OF BITS
vs
SAMPLING FREQUENCY (DIFFERENTIAL)

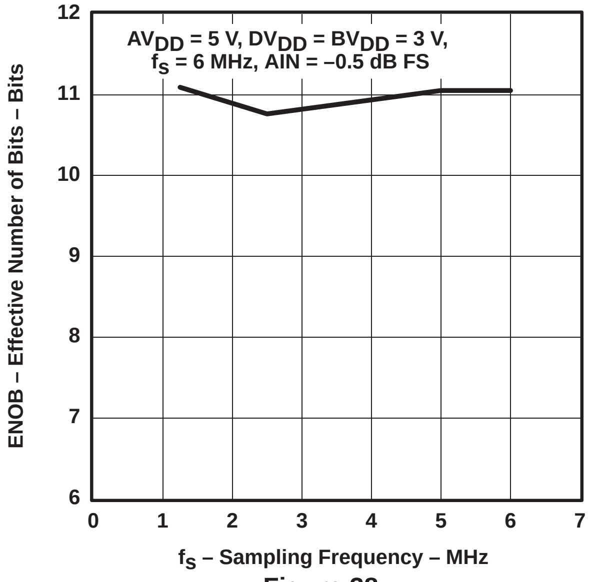


Figure 38

EFFECTIVE NUMBER OF BITS
vs
INPUT FREQUENCY (SINGLE-ENDED)

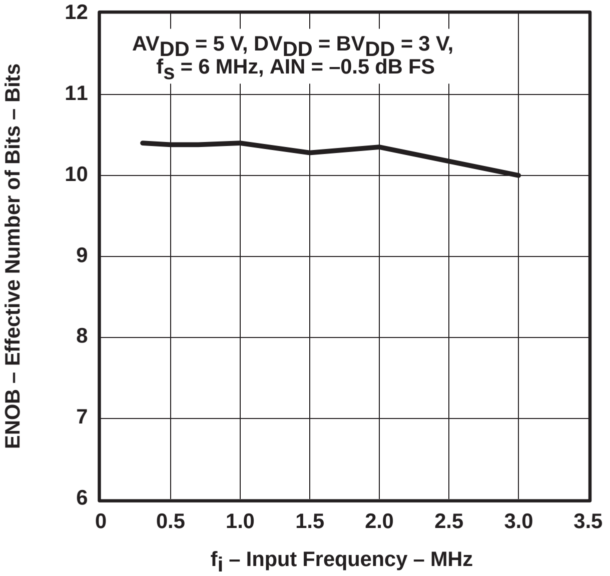


Figure 39

EFFECTIVE NUMBER OF BITS
vs
INPUT FREQUENCY (DIFFERENTIAL)

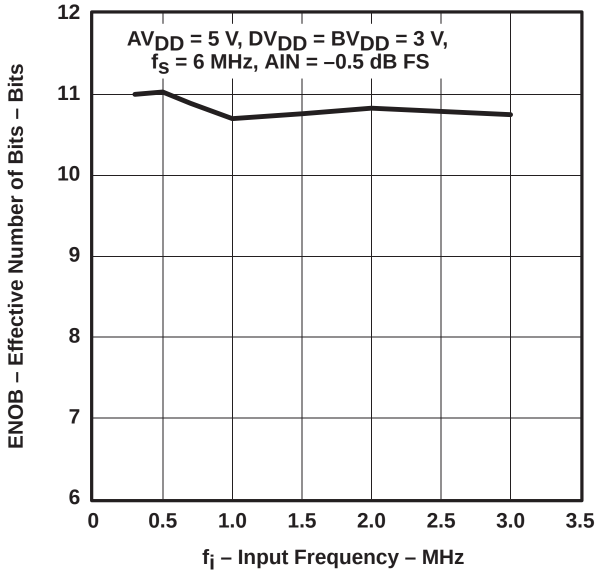


Figure 40

TYPICAL CHARACTERISTICS

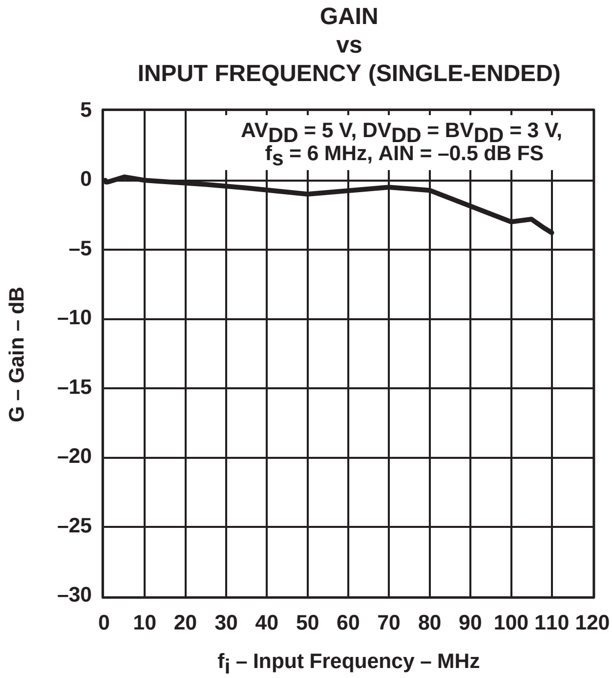


Figure 41

TYPICAL CHARACTERISTICS

FAST FOURIER TRANSFORM (4096 POINTS)
(SINGLE-ENDED)
vs
FREQUENCY

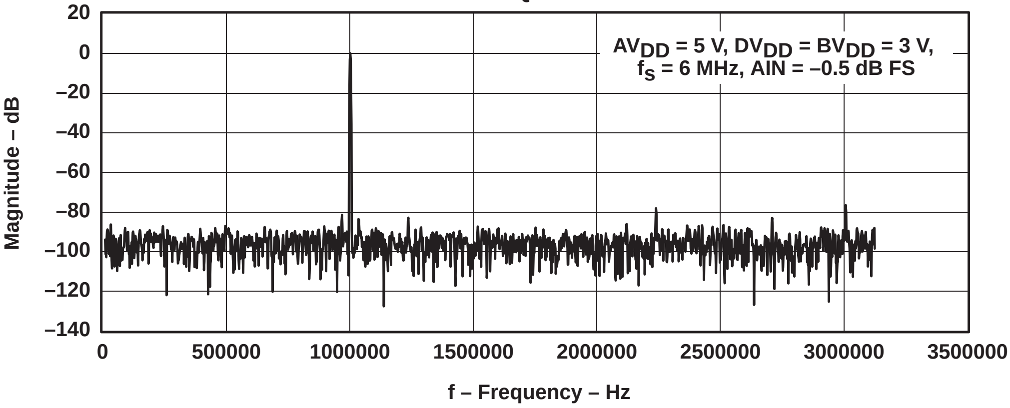


Figure 42

FAST FOURIER TRANSFORM (4096 POINTS)
(DIFFERENTIAL)
vs
FREQUENCY

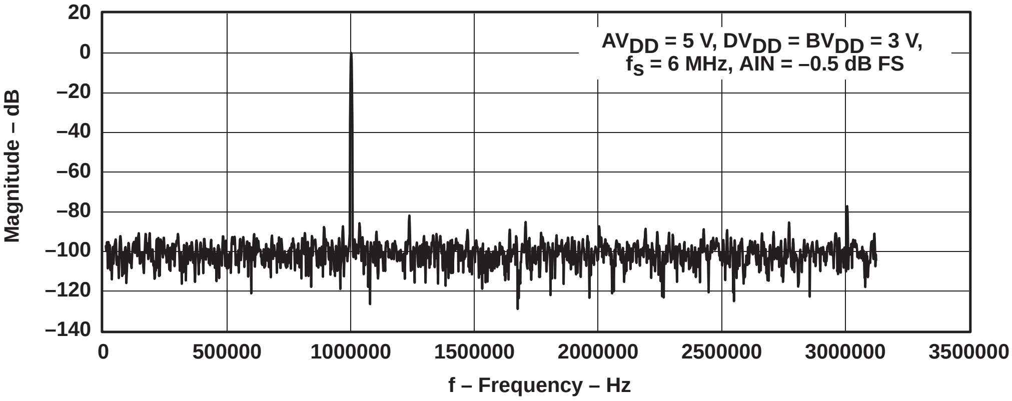


Figure 43

APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

zero offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = \frac{(SINAD - 1.76)}{6.02}$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

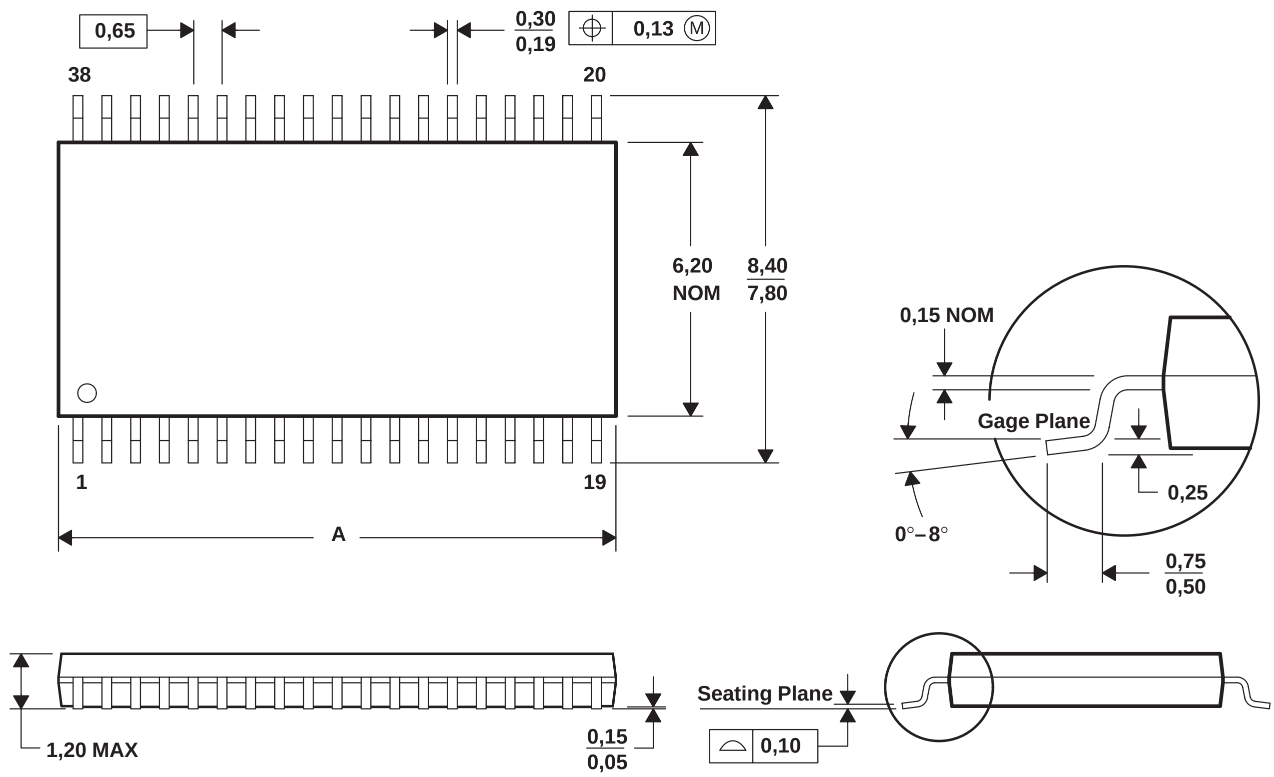
spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

MECHANICAL DATA

DA (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

38 PINS SHOWN



PINS ** / DIM	28	30	32	38
A MAX	9,80	11,10	11,10	12,60
A MIN	9,60	10,90	10,90	12,40

4040066 / D 11/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

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