

# THS1050

## 10-BIT 50 MSPS IF SAMPLING COMMUNICATIONS ANALOG-TO-DIGITAL CONVERTER

SLAS278 – APRIL 2000

### features

- 50 MSPS Maximum Sample Rate
- 10-Bit Resolution
- No Missing Codes
- On-Chip Sample and Hold
- 73 dB Spurious Free Dynamic Range at  $f_{in} = 15.5$  MHz
- 5 V Analog and Digital Supply
- 3 V and 5 V CMOS Compatible Digital Output
- 9.7 Bit ENOB at  $f_{IN} = 31$  MHz
- 60 dB SNR at  $f_{IN} = 31$  MHz
- 82 MHz Bandwidth
- Internal or External Reference
- Buffered 900  $\Omega$  Differential Analog Input

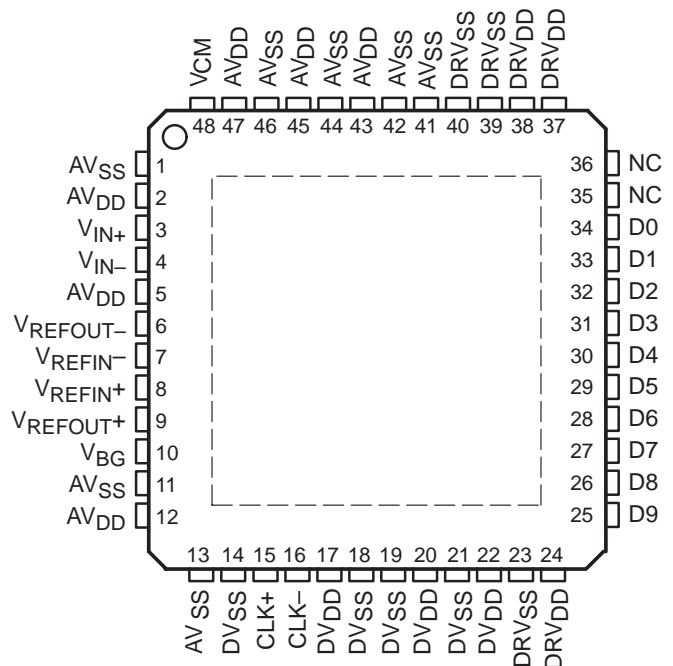
### applications

- Wireless Local Loop
- Wireless Internet Access
- Cable Modem Receivers
- Medical Ultrasound
- Magnetic Resonant Imaging

### description

The THS1050 is a high speed low noise 10-bit CMOS pipelined analog-to-digital converter. A differential sample and hold minimizes even order harmonics and allows for a high degree of common mode rejection at the analog input. A buffered analog input enables operation with a constant analog input impedance, and prevents transient voltage spikes from feeding backward to the analog input source. Full temperature DNL performance allows for industrial application with the assurance of no missing codes. The typical integral nonlinearity (INL) for the THS1050 is less than one LSB. The superior INL curve of the THS1050 results in SFDR performance that is exceptional for a 10-bit analog-to-digital converter. The THS1050 can operate with either internal or external references. Internal reference usage selection is accomplished simply by externally connecting reference output terminals to reference input terminals.

48 PHP PACKAGE  
(TOP VIEW)



### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE
	48-TQFP (PHP)
-40°C to 85°C	THS1050I
0°C to 70°C	THS1050C



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**TEXAS  
INSTRUMENTS**

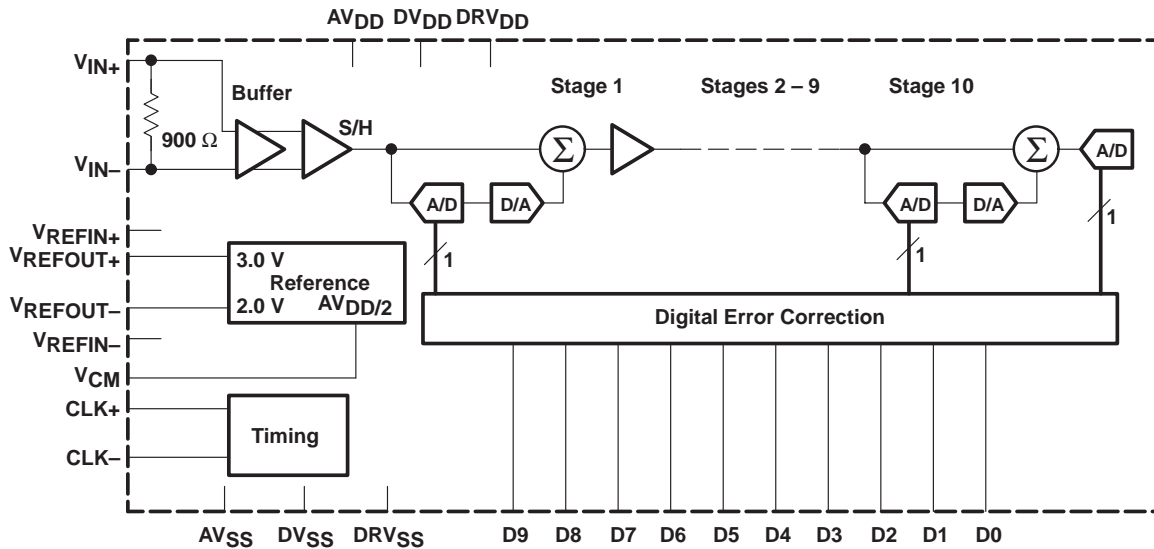
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**functional block diagram**



**Terminal Functions**

TERMINAL NAME	NO.	I/O	DESCRIPTION
AVDD	2, 5, 12, 43, 45, 47	I	Analog power supply
AVSS	1, 11, 13, 41, 42, 44, 46	I	Analog ground return for internal analog circuitry
CLK+	15	I	Clock input
CLK-	16	I	Complementary clock input
D9–D0	25–34	O	Digital data output bits; LSB= D0, MSB = D9 (2s complement output format)
DRVDD	24, 37, 38	I	Digital output driver supply
DRVSS	23, 39, 40	I	Digital output driver ground return
DVDD	17, 20, 22	I	Positive digital supply
DVSS	18, 19, 21	I	Digital ground return
VBG	10	O	Band gap reference. Bypass to ground with a 1 μF and a 0.01 μF chip capacitor.
VCM	48	O	Common mode voltage output. Bypass to ground with a 0.1 μF and a 0.01 μF chip device capacitor.
VIN+	3	I	Analog signal input
VIN-	4	I	Complementary analog signal input
VREFIN-	7	I	External reference input low
VREFIN+	8	I	External reference input high
VREFOUT+	9	O	Internal reference output. Compensate with a 1 μF and a 0.01 μF chip capacitor.
VREFOUT-	6	O	Internal reference output. Compensate with a 1 μF and a 0.01 μF chip capacitor.



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### detailed description

The THS1050 uses a differential pipeline architecture and assures no missing codes over the full operating temperature range. The device uses a 1 bit per stage architecture in order to achieve the highest possible bandwidth. The differential analog inputs are terminated with a 900-Ω resistor. The inputs are then fed to a unity gain buffer followed by the S/H (sample and hold) stage. This S/H stage is a switched capacitor operational amplifier based circuit, see Figure 3. The pipeline is a typical 1 bit per stage pipeline as shown in the functional block diagram. The digital output of the 10 stages and the last 1 bit flash are sent to a digital correction logic block which then outputs the final 10 bits.

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: $AV_{DD}$ .....	-0.5 V to 7 V
$DV_{DD}$ .....	-0.5 V to 7 V
$DRV_{DD}$ .....	-0.5 V to 7 V
Voltage between $AV_{SS}$ and $DV_{SS}$ .....	-0.3 V to 0.5 V
Voltage between $DRV_{DD}$ and $DV_{DD}$ .....	-0.5 V to 5 V
Voltage between $AV_{DD}$ and $DV_{DD}$ .....	-0.5 V to 5 V
Digital data output .....	-0.3 V to $DV_{DD}+0.3$ V
CLK peak input current .....	20 mA
Peak total input current (all inputs) .....	-30 mA
Operating free-air temperature range, $T_A$ : THS1050C .....	0°C to 70°C
THS1050I .....	-40°C to 85°C
Storage temperature range .....	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Sample rate		1		50	MSPS
Analog supply voltage, $AV_{DD}$		4.75	5	5.25	V
Digital supply voltage, $DV_{DD}$		4.75	5	5.25	V
Digital output driver supply voltage, $DRV_{DD}$		3	3.3	5.25	V
CLK + high level input voltage, $V_{IH}$		4	5	5.5	V
CLK + low-level input voltage, $V_{IL}$			0	1	V
CLK – high-level input voltage, $V_{IH}$		4	5	5.5	V
CLK – low-level input voltage, $V_{IL}$			0	1	V
CLK pulse-width high, $t_{p(H)}$		9	10		ns
CLK pulse-width low, $t_{p(L)}$		9	10		ns
Operating free-air temperature range, $T_A$	THS1050C	0		70	°C
Operating free-air temperature range, $T_A$	THS1050I	-40		85	°C



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electrical characteristics over recommended operating free-air temperature range,  
 $AV_{DD} = DV_{DD} = 5\text{ V}$ ,  $DRV_{DD} = 3.3\text{ V}$ , internal references,  $CLK = 50\text{ MHz}$  (unless otherwise noted)†

#### dc accuracy

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
DNL	Differential nonlinearity			±0.3	±0.6	LSB
	No missing codes			Assured		
INL	Integral nonlinearity			±0.9	±2.5	LSB
$E_O$	Offset error			14	29	mV
$E_G$	Gain error			-7	-10	%FSR

† All typical values are at  $T_A = 25^\circ\text{C}$ .

#### power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I(AV_{DD})$	Analog supply current	$V(V_{IN}) = V(V_{CM})$		100	145	mA
$I(DV_{DD})$	Digital supply current	$V(V_{IN}) = V(V_{CM})$		2	5	mA
$I(DRV_{DD})$	Output driver supply current	$V(V_{IN}) = V(V_{CM})$		2	6	mA
$P_D$	Power dissipation	$V(V_{IN}) = V(V_{CM})$		0.5		W

† All typical values are at  $T_A = 25^\circ\text{C}$ .

#### reference

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REFOUT-}$	Negative reference output voltage		1.95	2	2.05	V
$V_{REFOUT+}$	Positive reference output voltage		2.95	3	3.05	V
$V_{REFIN-}$	External reference supplied			2		V
$V_{REFIN+}$	External reference supplied			3		V
$V(V_{CM})$	Common mode output voltage			$AV_{DD}/2$		V
$I(V_{CM})$	Common mode output current			10		$\mu\text{A}$

† All typical values are at  $T_A = 25^\circ\text{C}$ .

#### analog input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_I$	Differential input resistance			900		$\Omega$
$C_I$	Differential input capacitance			4		pF
$V_I$	Analog input common mode range			$V_{CM} \pm 0.05$		V
$V_{ID}$	Differential input voltage range			2		V p-p
BW	Analog input bandwidth (large signal)	-3 dB		82		MHz

† All typical values are at  $T_A = 25^\circ\text{C}$ .

#### digital outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -50\ \mu\text{A}$	0.8 $DRV_{DD}$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 50\ \mu\text{A}$			0.2 $DRV_{DD}$	$V_{DD}$
$C_L$	Output load capacitance				15	pF

† All typical values are at  $T_A = 25^\circ\text{C}$ .



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ac specifications over recommended operating free-air temperature range,  $AV_{DD} = DV_{DD} = 5\text{ V}$ ,  $DRV_{DD} = 3.3\text{ V}$ , internal references,  $CLK = 50\text{ MHz}$ , analog input at  $-2\text{ dBFS}$  (unless otherwise noted)<sup>†</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	$f_{IN} = 2.2\text{ MHz}$		61		dBFS
		$f_{IN} = 15.5\text{ MHz}$	58	61		
		$f_{IN} = 31\text{ MHz}$		60.5		
SINAD	Signal-to-noise and distortion	$f_{IN} = 2.2\text{ MHz}$		60.5		dBFS
		$f_{IN} = 15.5\text{ MHz}$	56	60.8		
		$f_{IN} = 31\text{ MHz}$		60.2		
ENOB	Effective number of bits	$f_{IN} = 15.5\text{ MHz}$	9.3	9.8		bits
THD	Total harmonic distortion	$f_{IN} = 15.5\text{ MHz}$		-72	-63	dBc
SFDR	Spurious-free dynamic range	$f_{IN} = 15.5\text{ MHz}$	65	73		
2 <sup>nd</sup> Harmonic	Distortion	$f_{IN} = 2.2\text{ MHz}$		-83		dBc
		$f_{IN} = 15.5\text{ MHz}$		-89	-65	
		$f_{IN} = 31\text{ MHz}$		-77		
3 <sup>rd</sup> Harmonic	Distortion	$f_{IN} = 2.2\text{ MHz}$		-68		dBc
		$f_{IN} = 15.5\text{ MHz}$		-73	-65	
		$f_{IN} = 31\text{ MHz}$		-80		
Two tone SFDR		$F1 = 14.9\text{ MHz}$ , $F2 = 15.6\text{ MHz}$ , Analog inputs at $-8\text{ dBFS}$ each		72		dBc

<sup>†</sup> All typical values are at  $T_A = 25^\circ\text{C}$ .

operating characteristics over recommended operating conditions,  $AV_{DD} = DV_{DD} = 5\text{ V}$ ,  $DRV_{DD} = 3.3\text{ V}$ <sup>†</sup>

**switching specifications**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Aperture delay, $t_{d(A)}$			120		ps
Aperture jitter			1		ps RMS
Output delay $t_{d(O)}$	After falling edge of CLK+			13	ns
Pipeline delay $t_{d(PIPE)}$			6.5		CLK Cycle

<sup>†</sup> All typical values are at  $T_A = 25^\circ\text{C}$ .



# THS1050

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#### definitions of specifications

##### **analog bandwidth**

The analog input frequency at which the spectral power of the fundamental frequency of a large input signal is reduced by 3 dB.

##### **aperture delay**

The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

##### **aperture uncertainty (jitter)**

The sample-to-sample variation in aperture delay

##### **differential nonlinearity**

The average deviation of any output code from the ideal width of 1 LSB.

##### **clock pulse width/duty cycle**

Pulse width high is the minimum amount of time that the clock pulse should be left in logic 1 state to achieve rated performance; pulse width low is the minimum time clock pulse should be left in low state. At a given clock rate, these specs define acceptable clock duty cycles.

##### **offset error**

The difference between the analog input voltage at which the analog-to-digital converter output changes from negative full scale, to one LSB above negative full scale, and the ideal voltage at which this transition should occur.

##### **gain error**

The maximum error in LSBs between a digitized ideal full scale low frequency offset corrected triangle wave analog input, from the ideal digitized full scale triangle wave, divided by the full scale range, in this case 1024.

##### **harmonic distortion**

The ratio of the power of the fundamental to a given harmonic component reported in dBc.

##### **integral nonlinearity**

The deviation of the transfer function from an end-point adjusted reference line measured in fractions of 1 LSB. Also the integral of the DNL curve.

##### **output delay**

The delay between the 50% point of the falling edge of the clock and signal and the time when all output data bits are within valid logic levels (not including pipeline delay).

##### **signal-to-noise-and distortion (SINAD)**

When tested with a single tone, the ratio of the signal power to the sum of the power of all other spectral components, excluding dc, referenced to full scale.

##### **signal-to-noise ratio (SNR)**

When tested with a single tone, the ratio of the signal power to the sum of the power of all other power spectral components, excluding dc and the first 9 harmonics, referenced to full scale.

##### **effective number of bits (ENOB)**

For a sine wave, SINAD can be expressed in terms of the effective number of bits, using the following formula,

$$\text{ENOB} = \frac{(\text{SINAD} - 1.76)}{6.02}$$

##### **spurious-free dynamic range (SFDR)**

The ratio of the signal power to the power of the worst spur, excluding dc. The worst spurious component may or may not be a harmonic. The ratio is reported in dBc (that is, degrades as signal levels are lowered).



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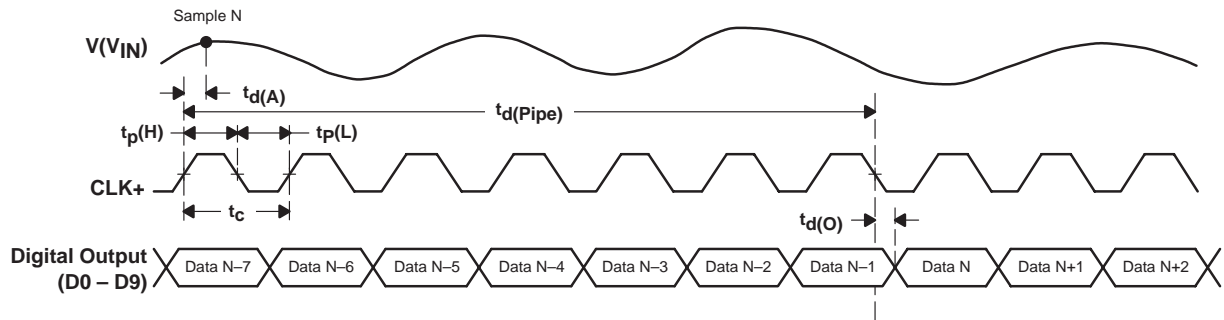


Figure 1. Timing Diagram

equivalent circuits

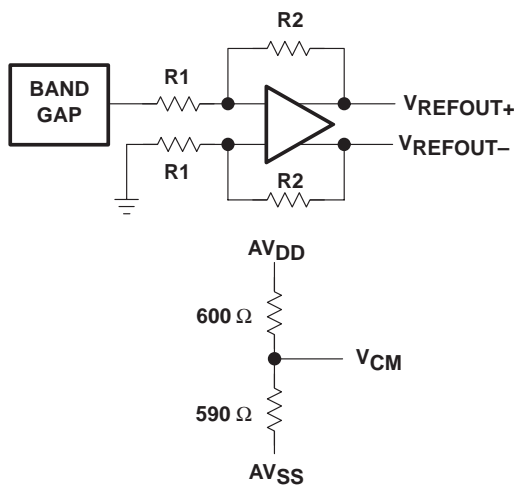


Figure 2. References

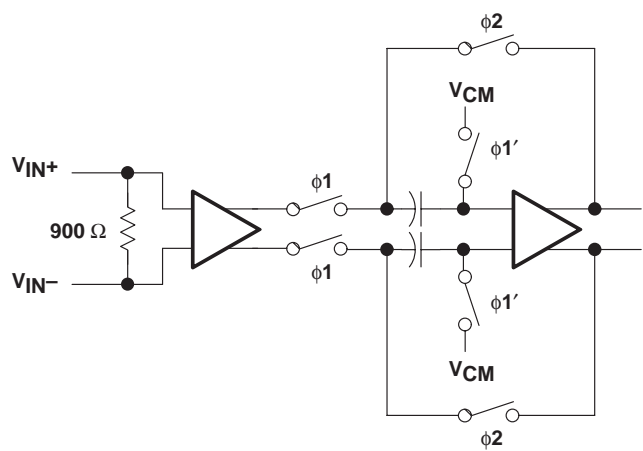


Figure 3. Analog Input Stage

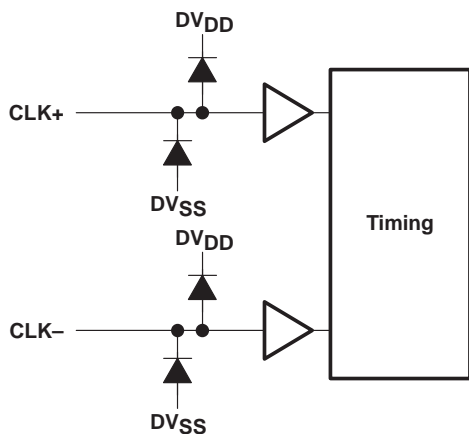


Figure 4. Clock Inputs

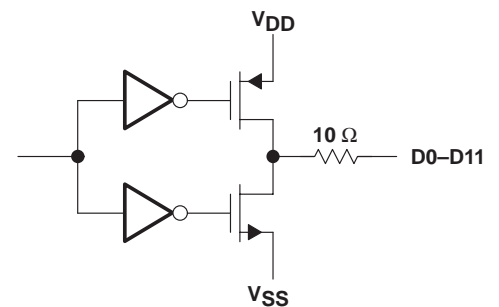


Figure 5. Digital Outputs

TYPICAL CHARACTERISTICS†

OUTPUT POWER SPECTRUM  
 VS  
 FREQUENCY

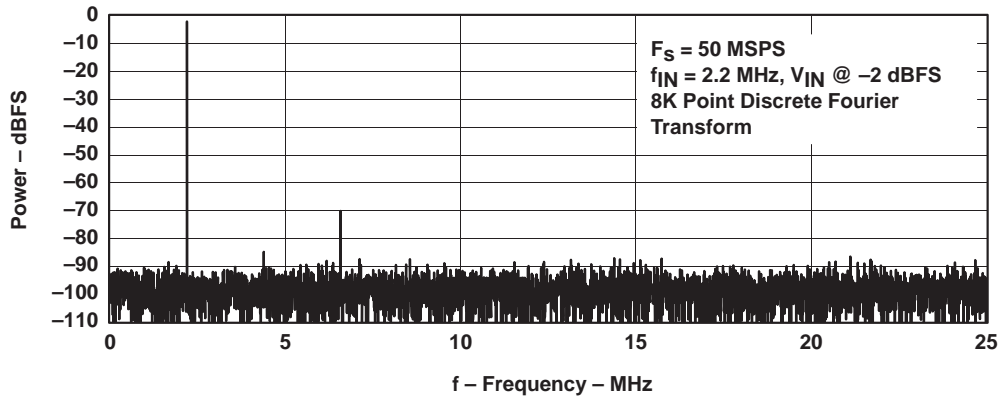


Figure 6

OUTPUT POWER SPECTRUM  
 VS  
 FREQUENCY

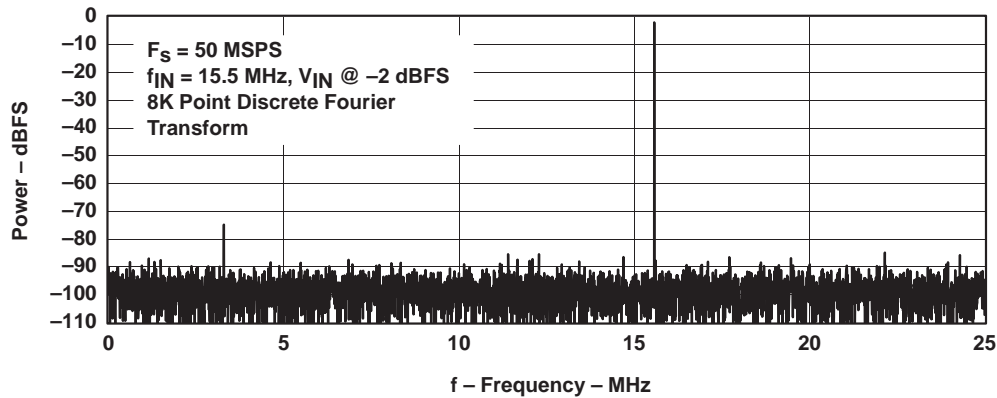


Figure 7

† AV<sub>DD</sub> = 5 V, DV<sub>DD</sub> = 5 V, DRV<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C (unless otherwise noted)



TYPICAL CHARACTERISTICS

OUTPUT POWER SPECTRUM  
vs  
FREQUENCY

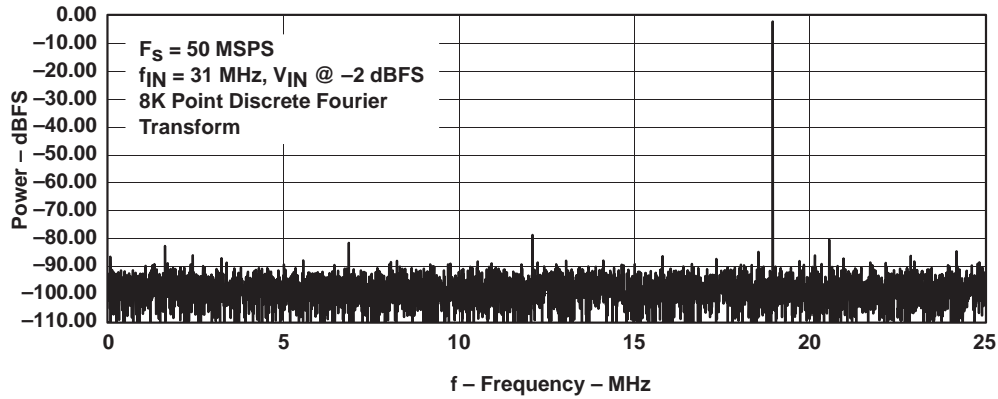


Figure 8

OUTPUT POWER SPECTRUM  
vs  
FREQUENCY

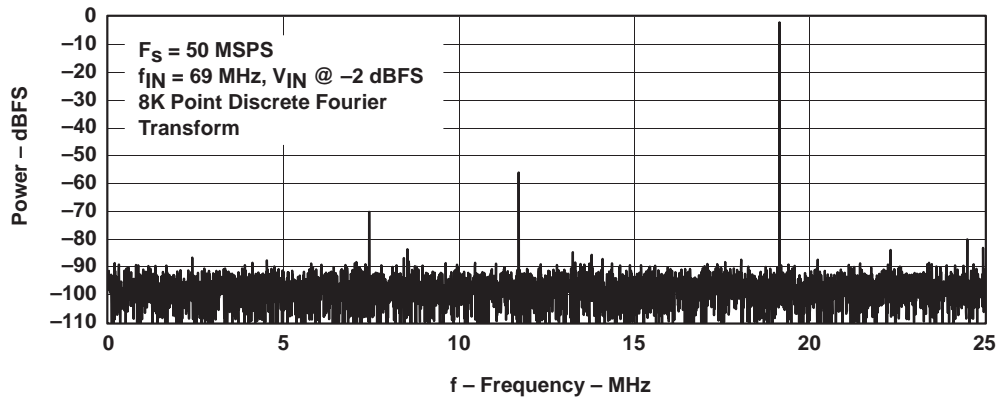


Figure 9

TYPICAL CHARACTERISTICS

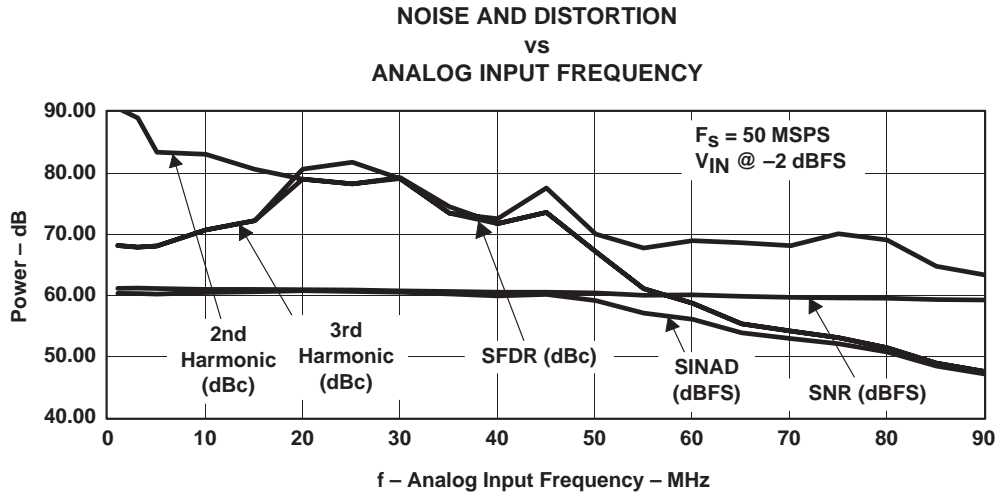


Figure 10

TWO-TONE OUTPUT POWER SPECTRUM  
 vs  
 FREQUENCY

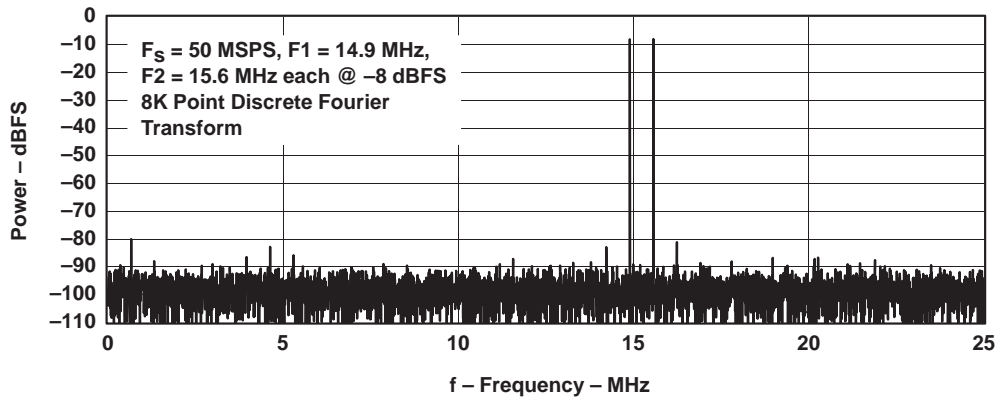


Figure 11

TYPICAL CHARACTERISTICS

NOISE AND DISTORTION  
 vs  
 ANALOG INPUT POWER LEVEL

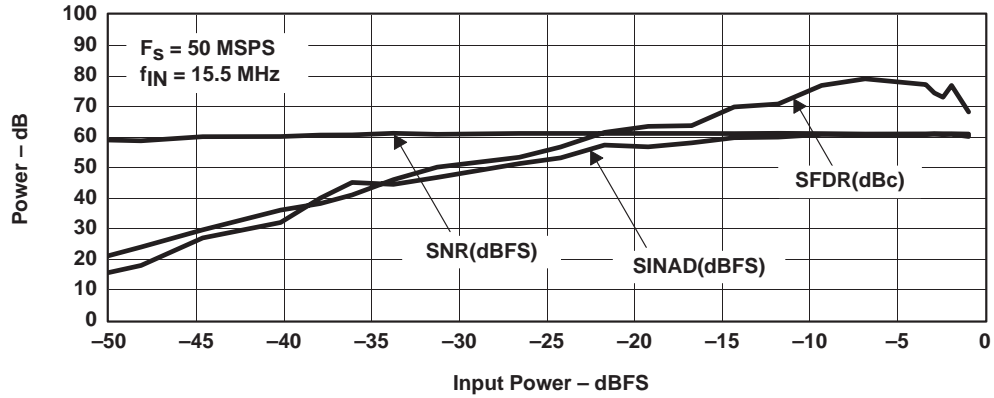


Figure 12

NOISE AND DISTORTION  
 vs  
 CLOCK FREQUENCY

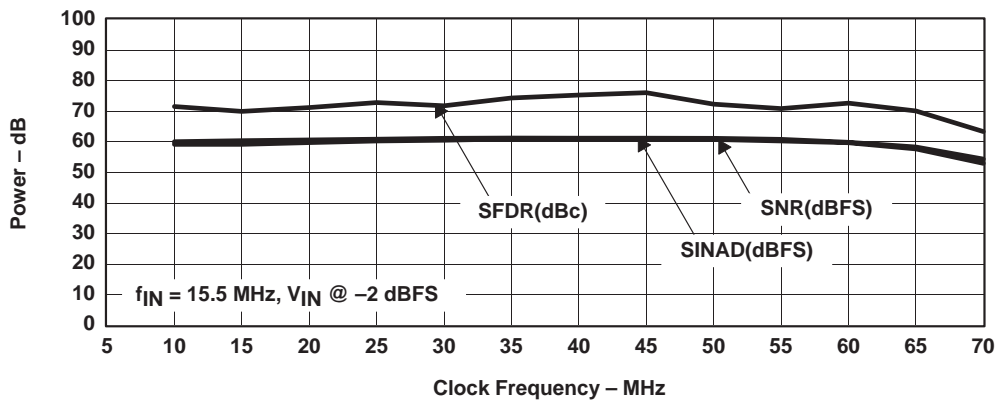


Figure 13

TYPICAL CHARACTERISTICS

NOISE AND DISTORTION  
 VS  
 DUTY CYCLE

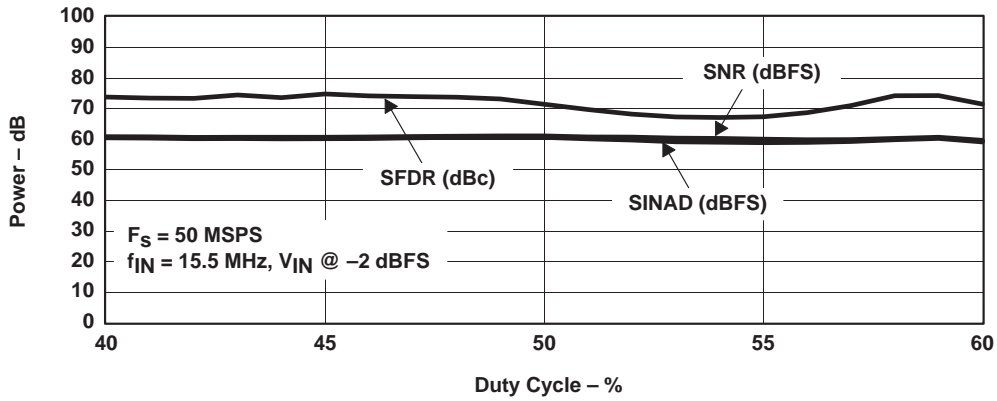


Figure 14

DIFFERENTIAL NONLINEARITY  
 VS  
 OUTPUT CODE

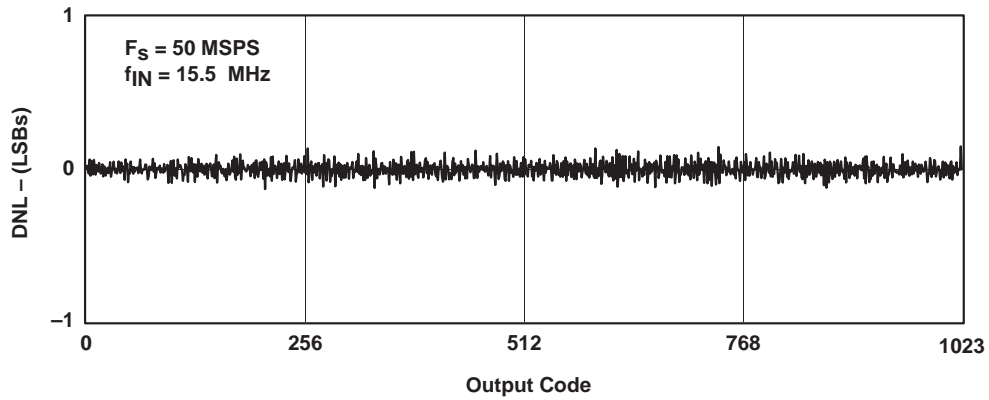


Figure 15

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY  
vs  
OUTPUT CODE

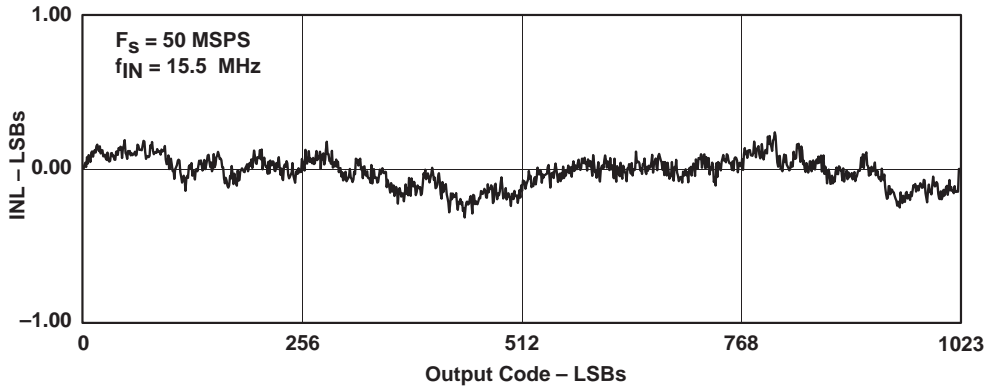


Figure 16

LARGE SIGNAL ANALOG INPUT BANDWIDTH

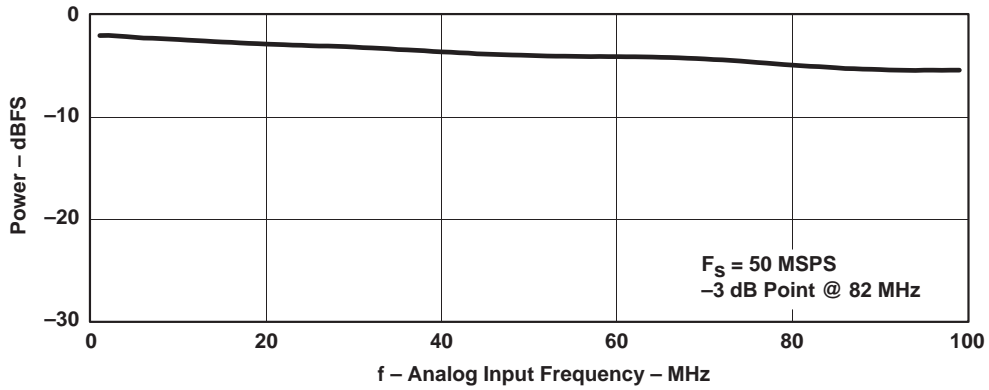


Figure 17

APPLICATION INFORMATION

using the THS1050 references

The option of internal or external reference is provided by allowing for an external connection of the internal reference to the reference inputs. This type of reference selection offers the lowest noise possible by not relying on any active switch to make the selection. Compensating each reference output with a 1- $\mu$ F and 0.01- $\mu$ F chip capacitor is required as shown in Figure 18. The differential analog input range is equal to  $2(V_{REFOUT+} - V_{REFOUT-})$ . When using external references, it is best to decouple the reference inputs with a 0.1- $\mu$ F and 0.01- $\mu$ F chip capacitor as shown in Figure 19.

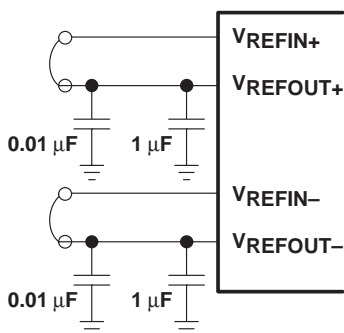


Figure 18. Internal Reference Usage

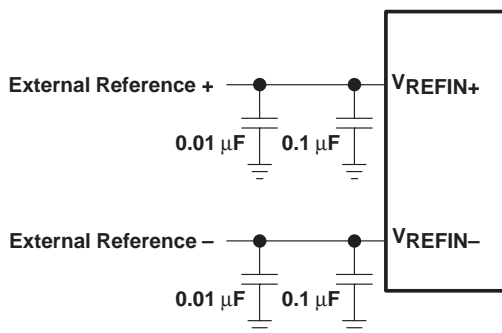


Figure 19. External Reference Usage

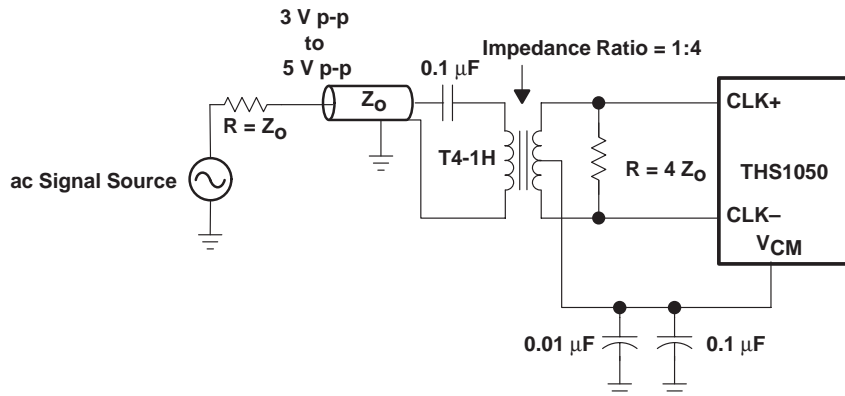
using the THS1050 clock input

The THS1050 is a high performance A/D converter. In order to obtain the best possible performance, care should be taken to ensure that the device is clocked appropriately. The optimal clock to the device is a low jitter square wave with sharp rise times (<2ns) at 50% duty cycle. The two clock inputs (CLK+ and CLK-), should be driven with complementary signals that have minimal skew, and nominally swing between 0 V and 5 V. The device will still operate with a peak-to-peak swing of 3 V on each clock channel (around the 2.5 V midpoint).

Use of a transformer coupled clock input ensures minimal skew between the CLK+ and CLK- signals. If the available clock signal swing is not adequate, a step-up transformer can be used in order to deliver the required levels to the converter's inputs, see Figure 20. For example if a 3.3 V standard CMOS logic is used for clock generation, a minicircuits T4-1H transformer can be used for 2x voltage step-up. This provides greater than 6-V differential swing at the secondary of the transformer, which provides greater than 3-V swings to both CLK+ and CLK- terminals of THS1050. The center tap of the transformer secondary is connected to the  $V_{CM}$  terminal of the THS1050 for proper dc biasing.

Both the transformer and the clock source should be placed close to THS1050 to avoid transmission line effects. 3.3 V TTL logic is not recommended with T4-1H transformer due to TTLs tendency to have lower output swings. If the input to the transformer is a square wave (such as one generated by a digital driver), care must be taken to ensure that the transformer's bandwidth does not limit the signal's rise time and effectively alter its shape and duty cycle characteristics. For a 50 MSPS rate, the transformer's bandwidth should be at least 300 MHz. A low phase noise sinewave can also be used to effectively drive the THS1050. In this case, the bandwidth of the transformer becomes less critical, as long as it can accommodate the frequency of interest (for example, 50 MHz). The turns ratio should be chosen to ensure appropriate levels at the device's input. If the clock signal is fed through a transmission line of characteristic impedance  $Z_0$ , then the secondary of the transformer should be terminated with a resistor of  $nZ_0$ , where n is the transformer's impedance ratio (1:n) as shown in Figure 20. Alternatively a series termination resistor having impedance equal to the characteristic impedance of the transmission line can be used at the clock source.

**APPLICATION INFORMATION**

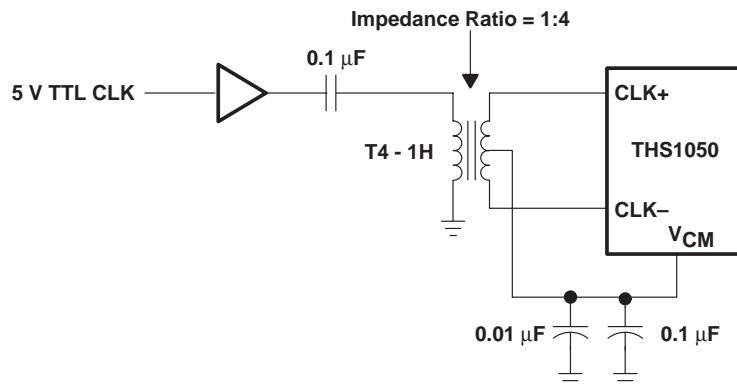


**Figure 20. Driving the Clock From an Impedance Matched Source**

The clock signals, CLK+ and CLK–, should be well matched and must both be driven.

A transformer ensures minimal skew between the two complementary channels. However, skew levels of up to 500 ps between CLK+ and CLK– can be tolerated with some performance degradation.

The clock input can also be driven differentially with a 5 V TTL signal by using an RF transformer to convert the TTL signal to a differential signal. The TTL signal is ac-coupled to the positive primary terminal with a high pass circuit. The negative terminal of the transformer is connected to ground (see Figure 21). The transformer secondary is connected to the CLK inputs.



**Figure 21. TTL Clock Input**

APPLICATION INFORMATION

using the analog input

The THS1050 obtains optimum performance when the analog signal inputs are driven differentially. The circuit below shows the optimum configuration, see Figure 22. The signal is fed to the primary of an RF transformer. Since the input signal must be biased around the common mode voltage of the internal circuitry, the common mode ( $V_{CM}$ ) reference from the THS1050 is connected to the center-tap of the secondary. To ensure a steady low noise  $V_{CM}$  reference, the best performance is obtained when the  $V_{CM}$  output is connected to ground with a 0.1- $\mu$ F and 0.01- $\mu$ F low inductance capacitor.

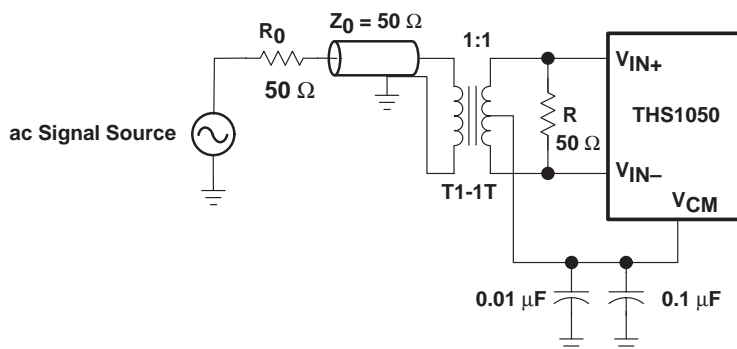


Figure 22. Driving the THS1050 Analog Input With Impedance Matched Transmission Line

When it is necessary to buffer or apply a gain to the incoming analog signal, it is also possible to combine a single-ended amplifier with an RF transformer as shown in Figure 23. For this application, a wide-band current mode feedback amplifier such as the THS3001 is best. The noninverting input to the op-amps is terminated with a resistor having an impedance equal to the characteristic impedance of the wave-guide or trace that sources the IF input signal. The single ended output allows the use of standard passive filters between the amplifier output and the primary. In this case, the SFDR of the op amp is not as critical as that of the A/D converter. While harmonics generated from within the A/D converter fold back into the first Nyquist zone, harmonics generated externally in the op amps can be filtered out with passive filters.

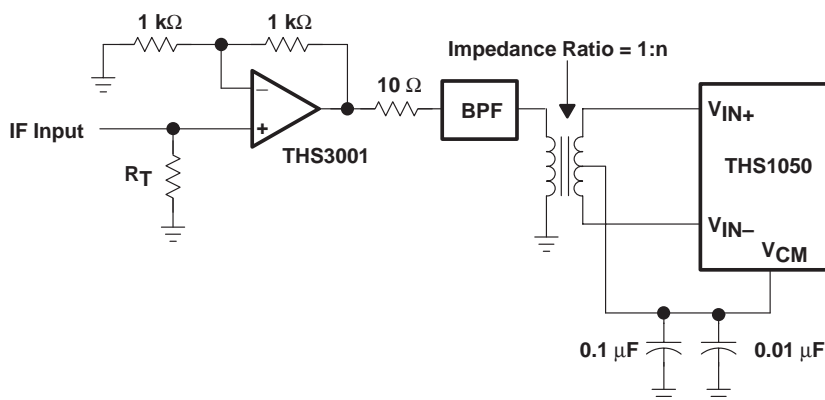


Figure 23. IF Input Buffered With THS3001 Op-Amp



## APPLICATION INFORMATION

### digital outputs

The digital outputs are in 2s complement format and can drive either TTL, 3-V CMOS, or 5-V CMOS logic. The digital output high voltage level is equal to  $DRV_{DD}$ . Table 1 shows the value of the digital output bits for full scale analog input voltage, midrange analog input voltage, and negative full scale input voltage. To reduce capacitive loading, each digital output of the THS1050 should drive only one digital input. The CMOS output drivers are capable of handling up to a 15 pF load. For better SNR performance, use 3.3 V for  $DRV_{DD}$ . Resistors of 200  $\Omega$  in series with the digital output can be used for optimizing SNR performance.

**Table 1. Digital Outputs**

ANALOG INPUT ( $V_{IN+}$ ) OR $-(V_{IN-})$	D9	D8	D7	D6	D5	D4	D	D2	D1	D0
$V_{ref+}$	0	1	1	1	1	1	1	1	1	1
$V_{CM}$	0	0	0	0	0	0	0	0	0	0
$V_{ref-}$	1	0	0	0	0	0	0	0	0	0

### power supplies

Best performance is obtained when  $AV_{DD}$  is kept separate from  $DV_{DD}$ . Regulated or linear supplies, as opposed to switched power supplies, must be used to minimize supply noise. It is also recommended to partition the analog and digital components on the board in such a way that the analog supply plane does not overlap with the digital supply plane in order to limit dielectric coupling between the different supplies.

### package

The THS1050 is packaged in a small 48-pin quad flat-pack PowerPAD™ package. The die of the THS1050 is bonded directly to copper alloy plate which is exposed on the bottom of the package. Although, the PowerPAD™ provides superior heat dissipation when soldered to ground land, it is not necessary to solder the bottom of the PowerPAD™ to anything in order to achieve minimum performance levels indicated in this specification over the full recommended operating temperature range.

If the device is to be used at ambient temperatures above the recommended operating temperatures, use of the PowerPAD™ is suggested.

The copper alloy plate or PowerPAD™ is exposed on the bottom of the device package for a direct solder attachment to a PCB land or conductive pad. The land dimensions should have minimum dimensions equal to the package dimensions minus 2 mm, see Figure 24.

For a multilayer circuit board, a second land having dimensions equal to or greater than the land to which the device is soldered should be placed on the back of the circuit board (see Figure 25). A total of 9 thermal vias or plated through-holes should be used to connect the two lands to a ground plane (buried or otherwise) having a minimum total area of 3 inches square in 1 oz. copper. For the THS1050 package, the thermal via centers should be spaced at a minimum of 1 mm. The ground plane need not be directly under or centered around the device footprint if a wide ground plane thermal run having a width on the order of the device is used to channel the heat from the vias to the larger portion of the ground plane. The THS1050 package has a standoff of 0.19 mm or 7.5 mils. In order to apply the proper amount of solder paste to the land, a solder paste stencil with a 6 mils thickness is recommended for this device. Too thin a stencil may lead to an inadequate connection to the land. Too thick a stencil may lead to beading of solder in the vicinity of the pins which may lead to shorts. For more information, refer to Texas Instruments literature number SLMA002 *PowerPAD™ Thermally Enhanced Package*.

PowerPAD is a trademark of Texas Instruments.



APPLICATION INFORMATION

package (continued)

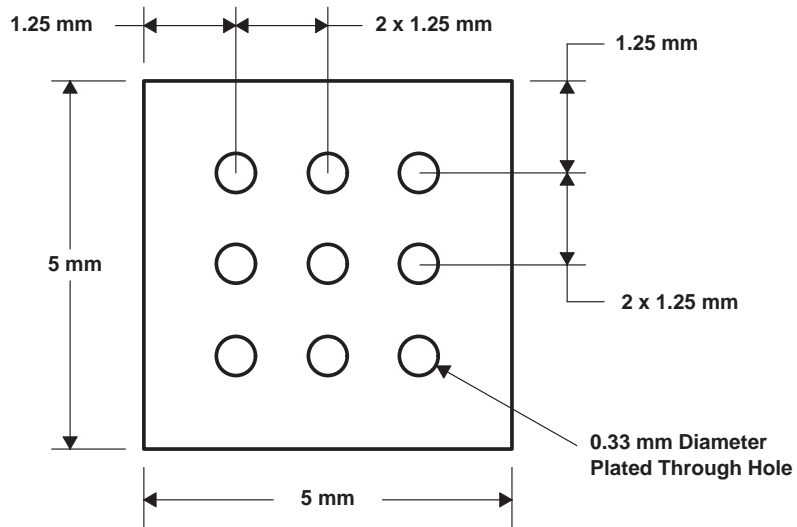


Figure 24. Thermal Land (top view)

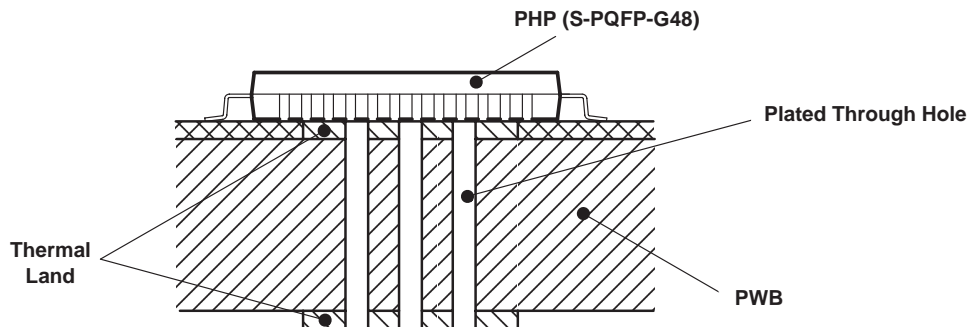


Figure 25. Top and Bottom Thermal Lands With Plated Through Holes (side view)

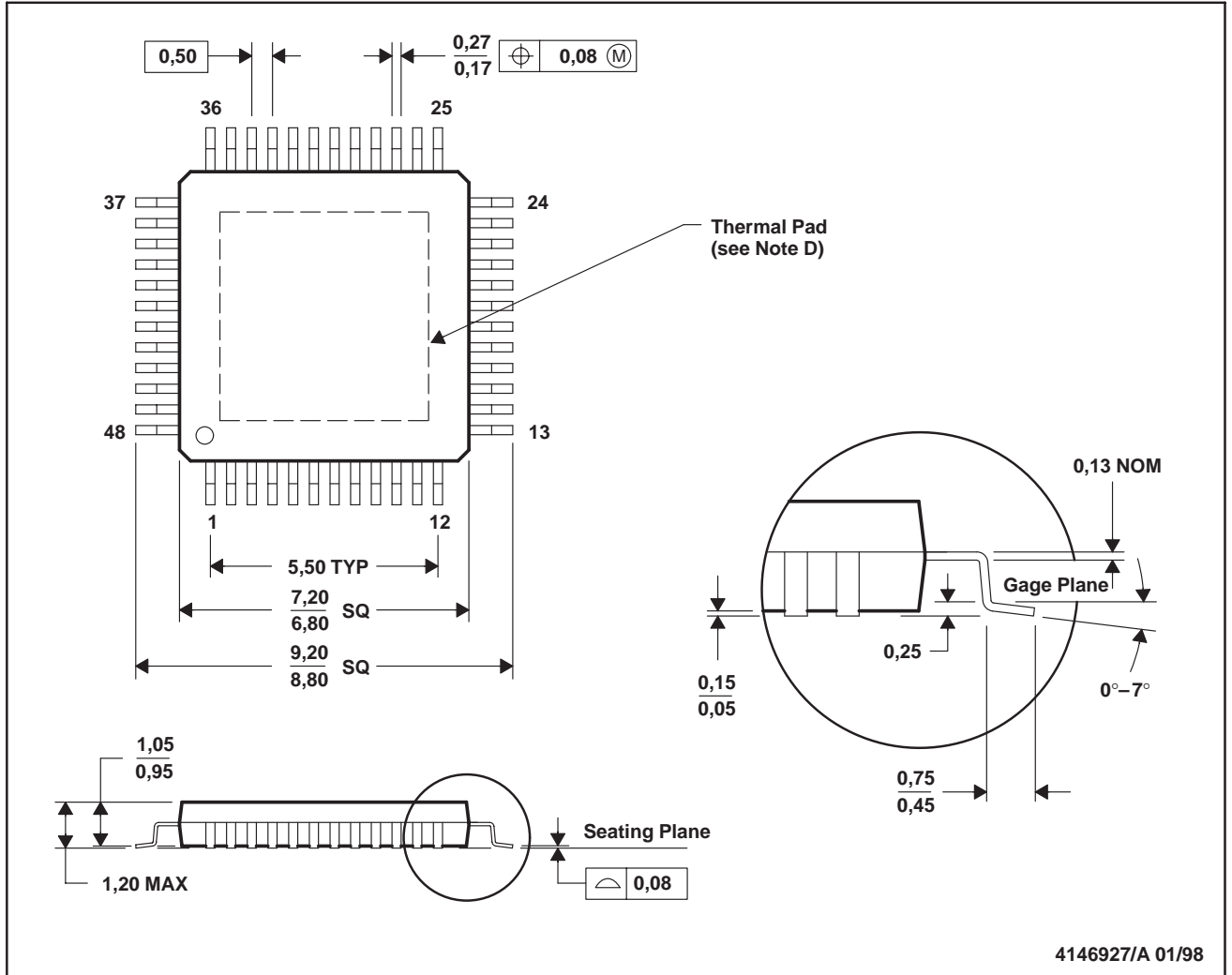
**THS1050**  
**10-BIT 50 MSPS IF SAMPLING COMMUNICATIONS**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS278 – APRIL 2000

**MECHANICAL DATA**

**PHP (S-PQFP-G48)**

**PowerPAD™ PLASTIC QUAD FLATPACK**



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusions.  
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.  
 E. Falls within JEDEC MO-153

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