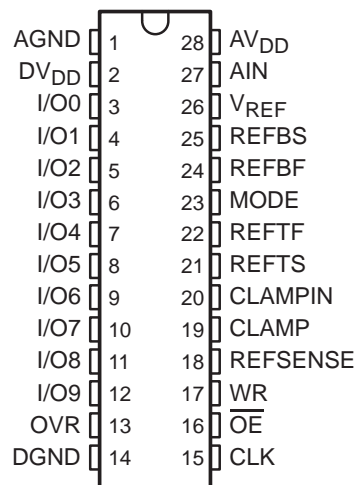


**THS1031**  
**2.7 V – 5.5 V, 10-BIT, 30 MSPS**  
**CMOS ANALOG-TO-DIGITAL CONVERTER**  
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- **10-Bit Resolution 30 MSPS Analog-to-Digital Converter:**
- **Configurable Input Functions:**
  - Single-Ended
  - Single-Ended With Analog Clamp
  - Single-Ended With Programmable Digital Clamp
  - Differential
- **Built-in Programmable Gain Amplifier (PGA)**
- **Differential Nonlinearity:  $\pm 0.3$  LSB**
- **Signal-to-Noise: 56 dB**
- **Spurious Free Dynamic Range: 60 dB**
- **Adjustable Internal Voltage Reference**
- **Straight Binary/2s Complement Output**
- **Out-of-Range Indicator**
- **Power-Down Mode**

**28-PIN TSSOP/SOIC PACKAGE  
(TOP VIEW)**



**description**

The THS1031 is a CMOS, low power, 10-bit, 30 MSPS analog-to-digital converter (ADC) that can operate with a supply range from 2.7 V to 3.3 V. The THS1031 has been designed to give circuit developers more flexibility. The analog input to the THS1031 can be either single-ended or differential. This device has a built-in clamp amplifier whose clamp input level can be selected from an external dc source or from an internal high-precision 10-bit digital clamp level programmable via an internal CLAMP register. A 3-bit PGA is included to maintain SNR for small signal. The THS1031 provides a wide selection of voltage reference to match the user's design requirements. For more design flexibility, the internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. The out-of-range output is used to monitor any out-of-range condition in THS1031's input range. The format of digital output can be coded in either straight binary or 2s complement.

The speed, resolution, and single-supply operation of the THS1031 are suited for applications in set-top-box (STB), video, multimedia, imaging, high-speed acquisition, and communications. The built-in clamp function allows dc restoration of video signal and is suitable for video application. The speed and resolution ideally suit charge-couple device (CCD) input systems such as color scanners, digital copiers, digital cameras, and camcorders. A wide input voltage range between REFBS and REFTS allows the THS1031 to be applied in both imaging and communications systems

The THS1031 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**AVAILABLE OPTIONS**

| T <sub>A</sub> | PACKAGED DEVICES |              |
|----------------|------------------|--------------|
|                | 28-TSSOP (PW)    | 28-SOIC (DW) |
| 0°C to 70°C    | THS1031CPW       | THS1031CDW   |
| -40°C to 85°C  | THS1031IPW       | THS1031IDW   |



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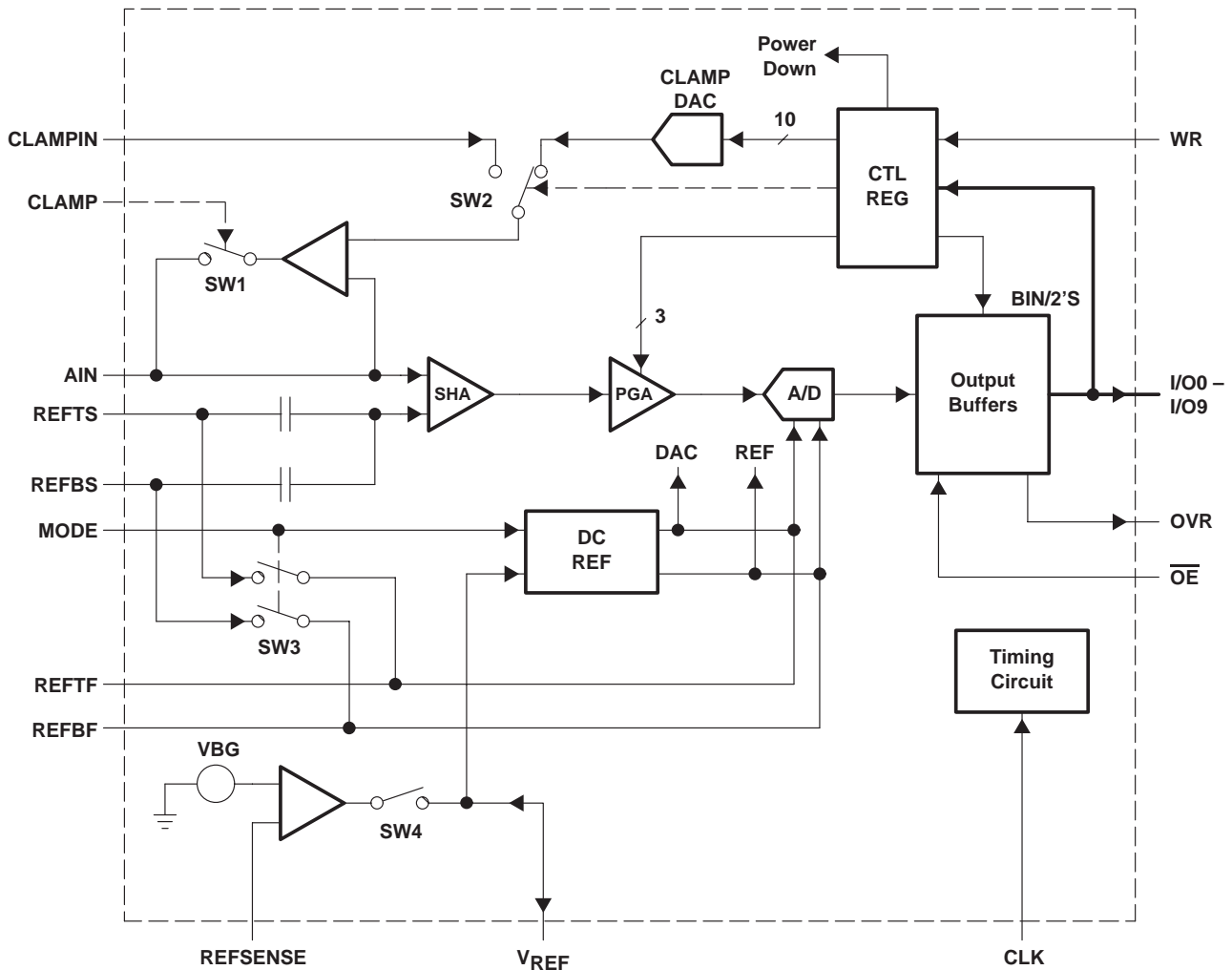


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**functional block diagram**



### Terminal Functions

| TERMINAL<br>NAME | NO. | I/O | DESCRIPTION   |
|------------------|-----|-----|---|
| AGND             | 1   | I   | Analog ground   |
| AIN              | 27  | I   | Analog input  |
| AVDD             | 28  | I   | Analog supply   |
| CLAMP            | 19  | I   | HI to enable CLAMP mode, LO to disable CLAMP mode                         |
| CLAMPIN          | 20  | I   | Connect to an external analog clamp reference input.                      |
| CLK              | 15  | I   | Clock input   |
| DGND             | 14  | I   | Digital ground  |
| DVDD             | 2   | I   | Digital driver supply   |
| I/O0             | 3   | I/O | Digital I/O bit 0 (LSB)   |
| I/O1             | 4   |     | Digital I/O bit 1   |
| I/O2             | 5   |     | Digital I/O bit 2   |
| I/O3             | 6   |     | Digital I/O bit 3   |
| I/O4             | 7   |     | Digital I/O bit 4   |
| I/O5             | 8   |     | Digital I/O bit 5   |
| I/O6             | 9   |     | Digital I/O bit 6   |
| I/O7             | 10  |     | Digital I/O bit 7   |
| I/O8             | 11  |     | Digital I/O bit 8   |
| I/O9             | 12  |     | Digital I/O bit 9 (MSB)   |
| MODE             | 23  | I   | Mode input  |
| $\overline{OE}$  | 16  | I   | HI to the 3-state data bus, LO to enable the data bus                     |
| OVR              | 13  | O   | Out-of-range indicator  |
| REFBS            | 25  | I   | Reference bottom sense  |
| REFBF            | 24  | I   | Reference bottom decoupling   |
| REFSENSE         | 18  | I   | Reference sense   |
| REFTF            | 22  | I   | Reference top decoupling  |
| REFTS            | 21  | I   | Reference top sense   |
| VREF             | 26  | I/O | Internal and external reference for ADC                                   |
| WR               | 17  | I   | Write strobe goes HI to write data value D0:D9 to the internal registers. |

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**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

|  |                                  |
|--|----------------------------------|
| Supply voltage: AV <sub>DD</sub> to AGND, DV <sub>DD</sub> to DGND | –0.3 to 6.5 V                    |
| AGND to DGND   | –0.3 to 0.3 V                    |
| AV <sub>DD</sub> to DV <sub>DD</sub>                               | –6.5 to 6.5 V                    |
| Mode input MODE to AGND  | –0.3 to AV <sub>DD</sub> + 0.3 V |
| Reference voltage input range REFTF, REFTB, REFTS, REFBS to AGND   | –0.3 to AV <sub>DD</sub> + 0.3 V |
| Analog input voltage range AIN to AGND                             | –0.3 to AV <sub>DD</sub> + 0.3 V |
| Reference input V <sub>REF</sub> to AGND                           | –0.3 to AV <sub>DD</sub> + 0.3 V |
| Reference output V <sub>REF</sub> to AGND                          | –0.3 to AV <sub>DD</sub> + 0.3 V |
| Clock input CLK to AGND  | –0.3 to AV <sub>DD</sub> + 0.3 V |
| Digital input to DGND  | –0.3 to DV <sub>DD</sub> + 0.3 V |
| Digital output to DGND   | –0.3 to DV <sub>DD</sub> + 0.3 V |
| Operating junction temperature range, T <sub>J</sub>               | 0°C to 150°C                     |
| Storage temperature range, T <sub>STG</sub>                        | –65°C to 150°C                   |
| Lead temperature 1,6 mm (1/16 in) from case for 10 seconds         | 300°C                            |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

**digital inputs**

|   | MIN | NOM | MAX                    | UNIT |
|---|-----|-----|------------------------|------|
| High-level input voltage, V <sub>IH</sub> | 2.4 |     |                        | V    |
| Low-level input voltage, V <sub>IL</sub>  |     |     | 0.2 x DV <sub>DD</sub> | V    |

**analog inputs**

|  | MIN   | NOM | MAX                 | UNIT |
|--|-------|-----|---------------------|------|
| Analog input voltage, V <sub>I(AIN)</sub>      | REFBS |     | REFTS               | V    |
| Reference input voltage, V <sub>I(VREF)</sub>  | 1     |     | 2                   | V    |
| Reference input voltage, V <sub>I(REFTS)</sub> | 1     |     | AV <sub>DD</sub>    | V    |
| Reference input voltage, V <sub>I(REFBS)</sub> | 0     |     | AV <sub>DD</sub> –1 | V    |
| Clamp input voltage, V <sub>I(CLAMPIN)</sub>   | REFBS |     | REFTS               | V    |

**power supply**

|                | MIN                             | NOM              | MAX | UNIT |     |   |
|----------------|---------------------------------|------------------|-----|------|-----|---|
| Supply voltage | Maximum sampling rate = 30 MSPS | AV <sub>DD</sub> | 2.7 | 3    | 5.5 | V |
|                |                                 | DV <sub>DD</sub> | 2.7 | 3    | 5.5 |   |

**REFTS, REFBS reference voltages (MODE = AV<sub>DD</sub>)**

|       | PARAMETER                           | MIN | TYP | MAX                 | UNIT |
|-------|-------------------------------------|-----|-----|---------------------|------|
| REFTS | Reference input voltage (top)       | 1   |     | AV <sub>DD</sub>    | V    |
| REFBS | Reference input voltage (bottom)    | 0   |     | AV <sub>DD</sub> –1 | V    |
|       | Differential input (REFTS – REFBS)  | 1   |     | 2                   | V    |
|       | Switched input capacitance on REFTS |     | 0.6 |                     | pF   |
|       | Switched input capacitance on REFBS |     | 0.6 |                     | pF   |

**sampling rate and resolution**

|                | PARAMETER | MIN | NOM | MAX | UNIT |
|----------------|-----------|-----|-----|-----|------|
| F <sub>s</sub> |           | 5   |     | 30  | MHz  |
| Resolution     |           |     | 10  |     | Bits |



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electrical characteristics,  $AV_{DD} = 3\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $F_s = 30\text{ MSPS}/50\%$  duty cycle,  $MODE = AV_{DD}$ , 2 V input span from 0.5 V to 2.5 V, external reference,  $PGA = 1X$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

#### analog inputs

| PARAMETER  |  | MIN   | TYP | MAX   | UNIT          |
|------------|--|-------|-----|-------|---------------|
| $V_I(AIN)$ | Analog input voltage                   | REFBS |     | REFTS | V             |
| $C_I$      | Switched input capacitance             |       | 1.2 |       | pF            |
| FPBW       | Full power BW (–3 dB)                  |       | 150 |       | MHz           |
|            | DC leakage current (input = $\pm FS$ ) |       | 100 |       | $\mu\text{A}$ |

#### REFTF, REFBF reference voltages

| PARAMETER                                |                        | TEST CONDITIONS        | MIN | TYP | MAX | UNIT     |
|--|------------------------|------------------------|-----|-----|-----|----------|
| Differential input (REFTF – REFBF)       |                        |                        | 1   |     | 2   | V        |
| Input common mode (REFTF + REFBF)/2      |                        | $AV_{DD} = 3\text{ V}$ | 1.3 | 1.5 | 1.7 | V        |
|  |                        | $AV_{DD} = 5\text{ V}$ | 2   | 2.5 | 3   |          |
| REFTF (MODE = $AV_{DD}$ )                | $V_{REF} = 1\text{ V}$ | $AV_{DD} = 3\text{ V}$ |     | 2   |     | V        |
|  |                        | $AV_{DD} = 5\text{ V}$ |     | 3   |     |          |
|  | $V_{REF} = 2\text{ V}$ | $AV_{DD} = 3\text{ V}$ |     | 2.5 |     | V        |
|  |                        | $AV_{DD} = 5\text{ V}$ |     | 3.5 |     |          |
| REFBF (MODE = $AV_{DD}$ )                | $V_{REF} = 1\text{ V}$ | $AV_{DD} = 3\text{ V}$ |     | 1   |     | V        |
|  |                        | $AV_{DD} = 5\text{ V}$ |     | 0.5 |     |          |
|  | $V_{REF} = 2\text{ V}$ | $AV_{DD} = 3\text{ V}$ |     | 2   |     | V        |
|  |                        | $AV_{DD} = 5\text{ V}$ |     | 1.5 |     |          |
| Input resistance between REFTF and REFBF |                        |                        |     | 600 |     | $\Omega$ |

#### $V_{REF}$ reference voltages

| PARAMETER                                      |  | MIN  | TYP | MAX  | UNIT             |
|--|--|------|-----|------|------------------|
| Internal 1 V reference (REFSENSE = $V_{REF}$ ) |  | 0.95 | 1   | 1.05 | V                |
| Internal 2 V reference (REFSENSE = $AV_{SS}$ ) |  | 1.90 | 2   | 2.10 | V                |
| External reference (REFSENSE = $AV_{DD}$ )     |  | 1    |     | 2    | V                |
| Reference input resistance                     |  |      | 18  |      | $\text{k}\Omega$ |

#### dc accuracy

| PARAMETER |                           | MIN                     | TYP       | MAX     | UNIT |
|-----------|---------------------------|-------------------------|-----------|---------|------|
| INL       | Integral nonlinearity     |                         | $\pm 1$   | $\pm 2$ | LSB  |
| DNL       | Differential nonlinearity |                         | $\pm 0.3$ | $\pm 1$ | LSB  |
|           | Offset error              |                         | 0.4       | 1.4     | %FSR |
|           | Gain error                |                         | 1.4       | 3.5     | %FSR |
|           | Missing code              | No missing code assured |           |         |      |



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electrical characteristics,  $AV_{DD} = 3\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $F_s = 30\text{ MSPS}/50\%$  duty cycle,  $MODE = AV_{DD}$ ,  $2\text{ V}$  input span from  $0.5\text{ V}$  to  $2.5\text{ V}$ , external reference,  $PGA = 1X$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted) (continued)

**dynamic performance (ADC and PGA)**

| PARAMETER |                                | TEST CONDITIONS                     | MIN   | TYP   | MAX | UNIT |
|-----------|--------------------------------|-------------------------------------|-------|-------|-----|------|
| ENOB      | Effective number of bits       | f = 3.5 MHz                         | 8.2   | 9     |     | Bits |
|           |                                | f = 3.5 MHz, $AV_{DD} = 5\text{ V}$ |       | 8.8   |     |      |
|           |                                | f = 15 MHz                          |       | 7.7   |     |      |
|           |                                | f = 15 MHz, $AV_{DD} = 5\text{ V}$  |       | 7.64  |     |      |
| SFDR      | Spurious free dynamic range    | f = 3.5 MHz                         | 55    | 60    |     | dB   |
|           |                                | f = 3.5 MHz, $AV_{DD} = 5\text{ V}$ |       | 63    |     |      |
|           |                                | f = 15 MHz                          |       | 48    |     |      |
|           |                                | f = 15 MHz, $AV_{DD} = 5\text{ V}$  |       | 52.4  |     |      |
| THD       | Total harmonic distortion      | f = 3.5 MHz                         | -58.2 | -54.7 |     | dB   |
|           |                                | f = 3.5 MHz, $AV_{DD} = 5\text{ V}$ |       | -68.7 |     |      |
|           |                                | f = 15 MHz                          |       | -47   |     |      |
|           |                                | f = 15 MHz, $AV_{DD} = 5\text{ V}$  |       | -51.9 |     |      |
| SNR       | Signal-to-noise                | f = 3.5 MHz                         | 51.2  | 56    |     | dB   |
|           |                                | f = 3.5 MHz, $AV_{DD} = 5\text{ V}$ |       | 55    |     |      |
|           |                                | f = 15 MHz                          |       | 53    |     |      |
|           |                                | f = 15 MHz, $AV_{DD} = 5\text{ V}$  |       | 49.3  |     |      |
| SINAD     | Signal-to-noise and distortion | f = 3.5 MHz                         | 51.1  | 56    |     | dB   |
|           |                                | f = 3.5 MHz, $AV_{DD} = 5\text{ V}$ |       | 55    |     |      |
|           |                                | f = 15 MHz                          |       | 48.1  |     |      |
|           |                                | f = 15 MHz, $AV_{DD} = 5\text{ V}$  |       | 47.7  |     |      |

**PGA**

| PARAMETER                     | MIN | TYP | MAX | UNIT |
|-------------------------------|-----|-----|-----|------|
| Gain range (linear scale)     | 0.5 |     | 4   | V/V  |
| Gain step size (linear scale) |     | 0.5 |     |      |
| Gain error from nominal       |     |     | 3%  |      |
| Number of control bits        |     | 3   |     | Bits |

**clamp DAC**

| PARAMETER                            | MIN   | TYP | MAX             | UNIT |
|--------------------------------------|-------|-----|-----------------|------|
| Resolution                           |       | 10  |                 | Bits |
| DAC output range                     | REFBF |     | RETF            |      |
| Clamping analog output voltage range | 0.1   |     | $AV_{DD} - 0.1$ | V    |
| Clamping analog output voltage error | -40   |     | +40             | mV   |



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**clock**

| PARAMETER  |                               | MIN | TYP  | MAX | UNIT   |
|------------|-------------------------------|-----|------|-----|--------|
| $t_{CK}$   | Clock period                  | 33  |      |     | ns     |
| $t_{CKH}$  | Pulse duration, clock high    | 15  | 16.5 |     | ns     |
| $t_{CKL}$  | Pulse duration, clock low     | 15  | 16.5 |     | ns     |
| $t_d$      | Clock to data valid           |     |      | 25  | ns     |
|            | Pipeline latency              |     | 3    |     | Cycles |
| $t_{(ap)}$ | Aperture delay                |     | 4    |     | ns     |
|            | Aperture uncertainty (jitter) |     | 2    |     | ps     |

**timing**

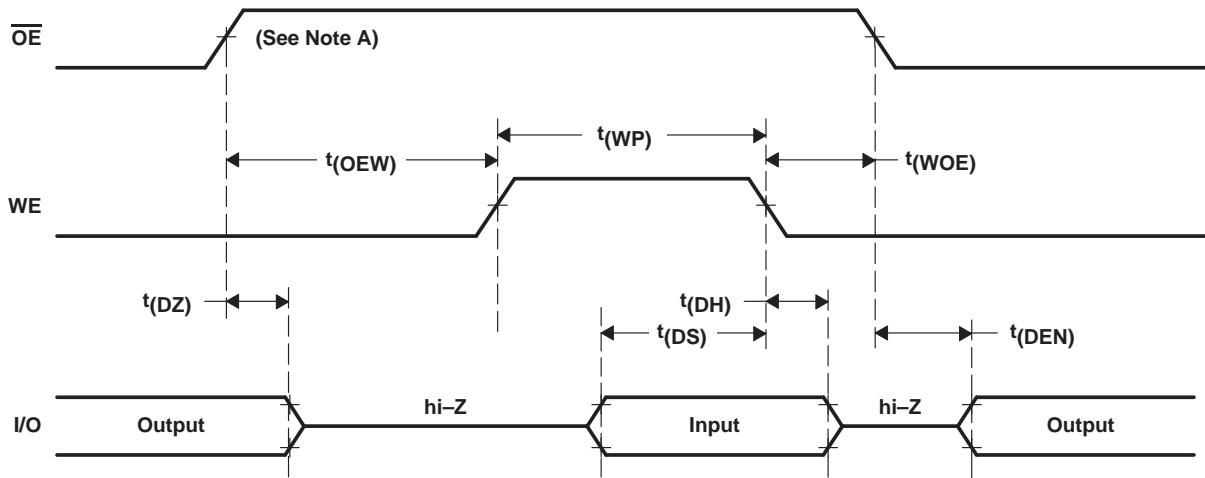
| PARAMETER   |                                 | MIN | TYP | MAX | UNIT |
|-------------|---------------------------------|-----|-----|-----|------|
| $t_{(PZ)}$  | Output disable to high-Z output | 0   |     | 20  | ns   |
| $t_{(DEN)}$ | Output enable to output valid   | 0   |     | 20  | ns   |
| $t_{(OEW)}$ | Output disable to write enable  | 12  |     |     | ns   |
| $t_{(WOE)}$ | Output enable to write enable   | 12  |     |     | ns   |
| $t_{(WP)}$  | Write pulse                     | 15  |     |     | ns   |
| $t_{(DS)}$  | Input data setup time           | 5   |     |     | ns   |
| $t_{(DH)}$  | Input data hold time            | 5   |     |     | ns   |

**power supply**

| PARAMETER          | TEST CONDITIONS          | MIN                              | TYP  | MAX | UNIT |
|--------------------|--------------------------|----------------------------------|------|-----|------|
| $I_{CC}$           | Operating supply current |                                  | 30.6 | 45  | mA   |
| $P_D$              | Power dissipation        | $AV_{DD} = DV_{DD} = 3\text{ V}$ |      | 94  | mW   |
|                    |                          | $AV_{DD} = DV_{DD} = 5\text{ V}$ |      | 160 |      |
| $P_D(\text{STBY})$ | Standby power            |                                  | 3    | 5   | mW   |

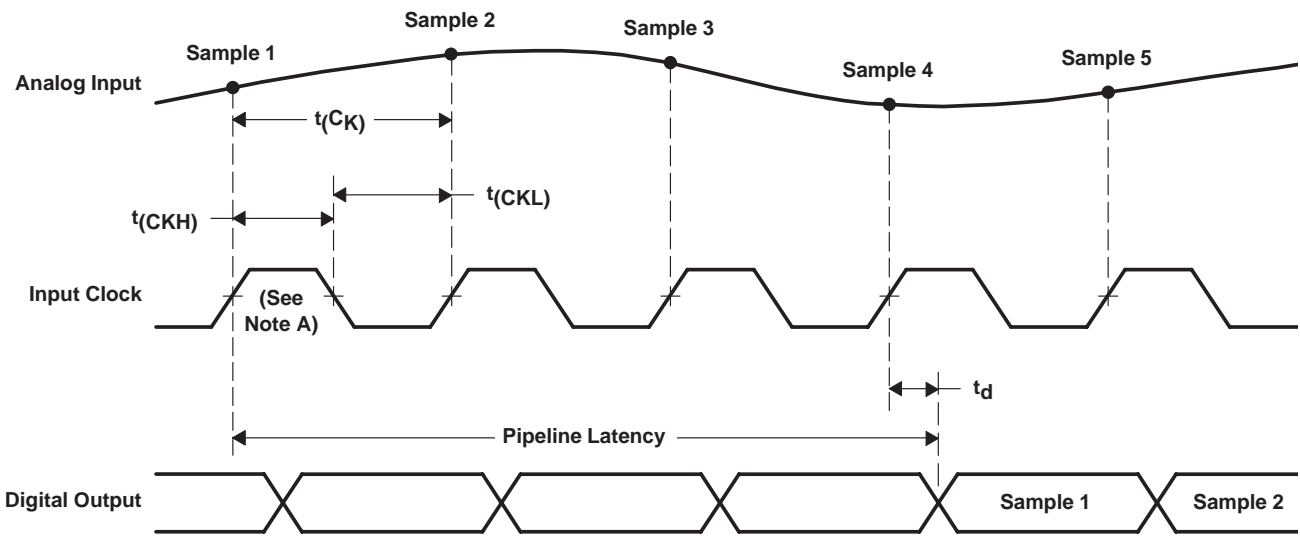


**PARAMETER MEASUREMENT INFORMATION**



NOTE A: All timing measurements are based on 50% of edge transition.

**Figure 1. Write Timing Diagram**



NOTE A: All timing measurements are based on 50% of edge transition.

**Figure 2. Digital Output Timing Diagram**



TYPICAL CHARACTERISTICS

POWER DISSIPATION  
vs  
SAMPLING FREQUENCY

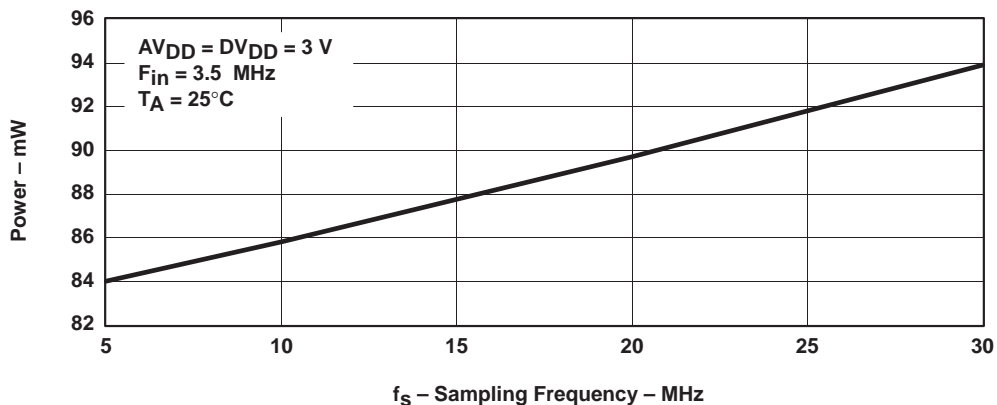


Figure 3

EFFECTIVE NUMBER OF BITS  
vs  
TEMPERATURE

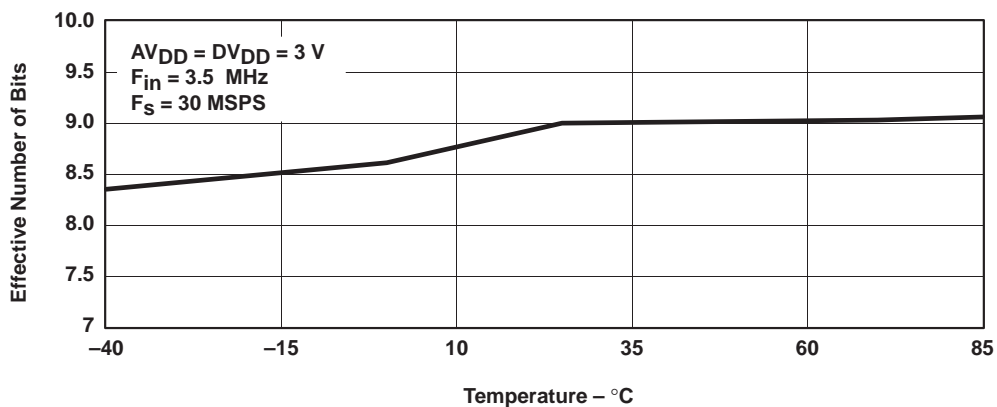
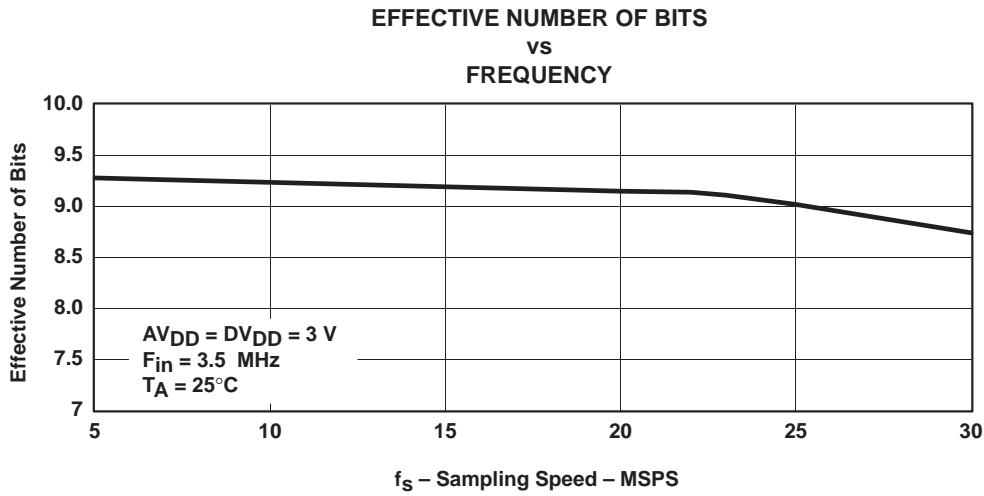
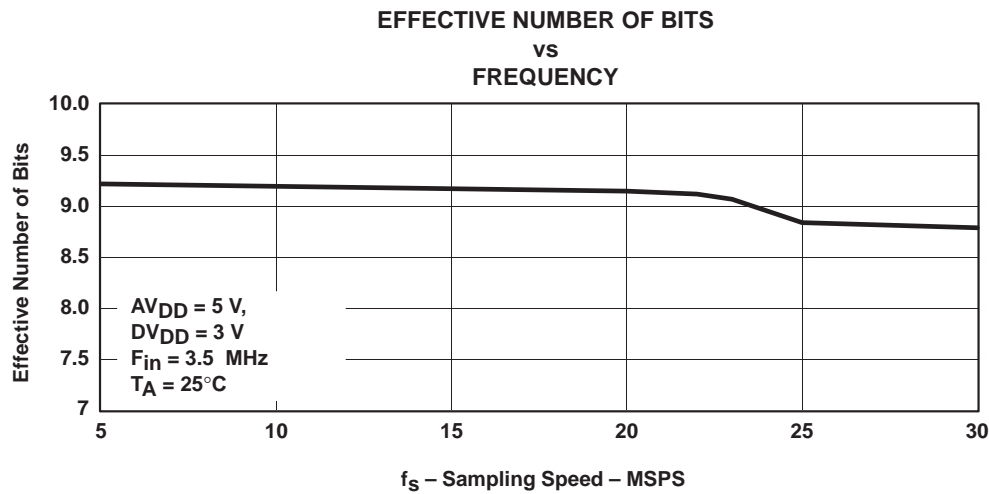


Figure 4

**TYPICAL CHARACTERISTICS**



**Figure 5**



**Figure 6**

TYPICAL CHARACTERISTICS

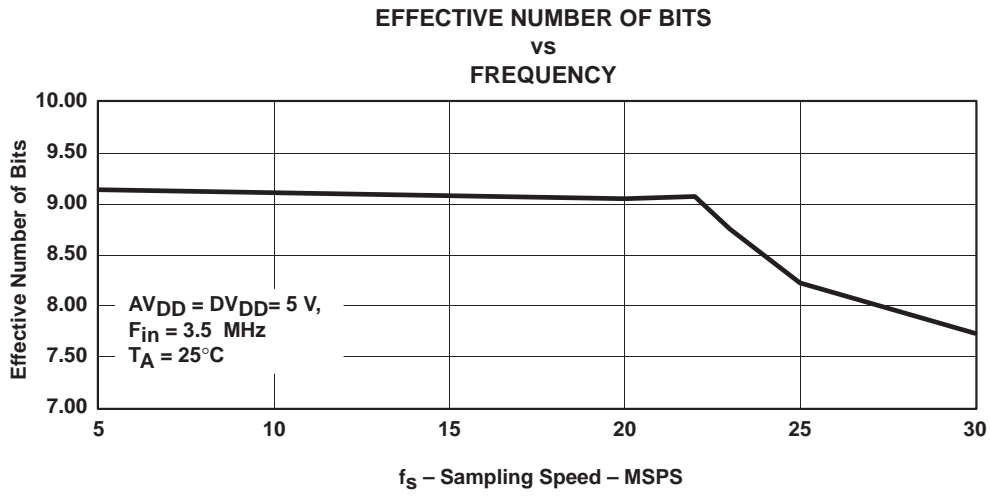


Figure 7

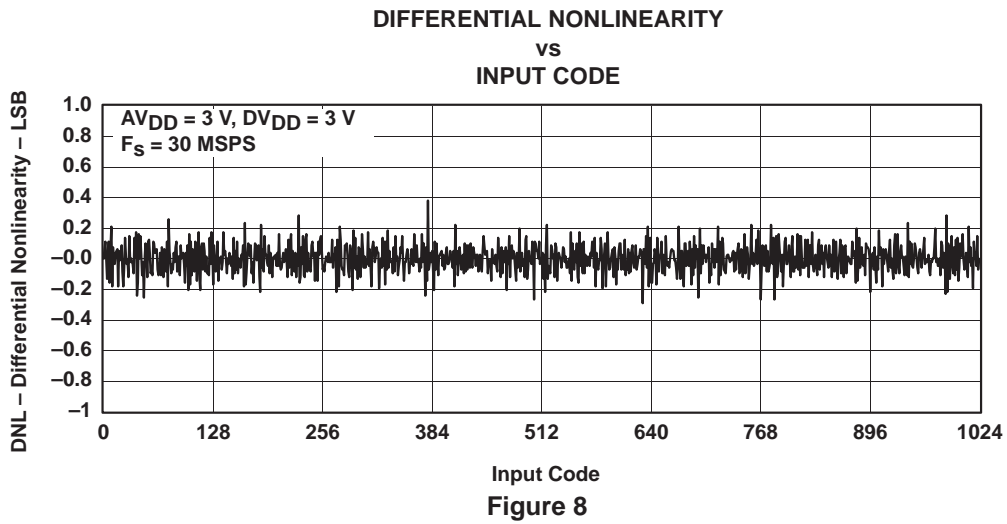


Figure 8

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY  
vs  
INPUT CODE

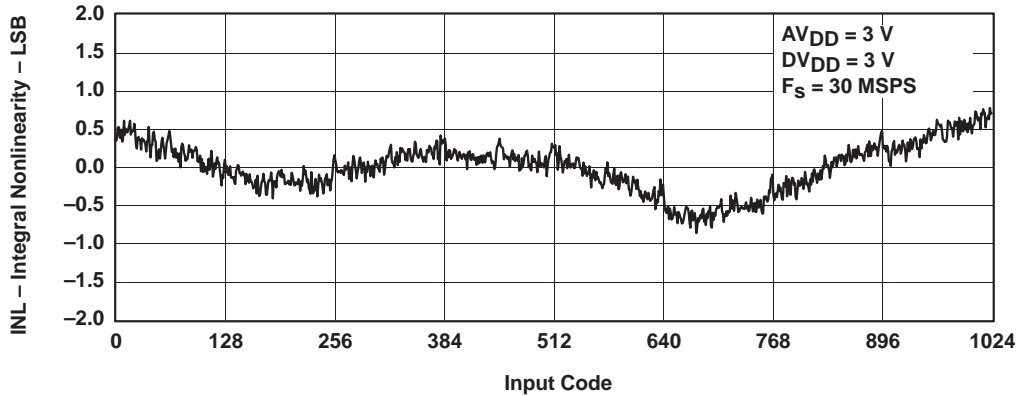


Figure 9

FFT  
vs  
FREQUENCY

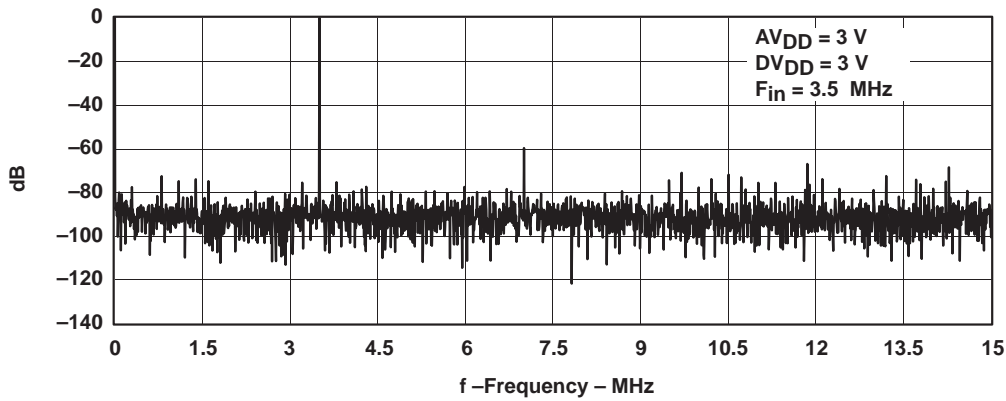


Figure 10

## PRINCIPLES OF OPERATION

**Table 1. Mode Selection**

| MODES              | ANALOG INPUT   | INPUT SPAN                       | MODE PIN            | REFSENSE PIN                        | VREF PIN                         | REFTS PIN                                    | REFBS PIN                                 | FIGURE     |
|--------------------|--|----------------------------------|---------------------|-------------------------------------|----------------------------------|--|---|------------|
| Top/bottom         | AIN  | 1 V                              | AV <sub>DD</sub>    | Short together                      |                                  |  | AGND                                      | 8, 15      |
|                    | AIN  | 2 V                              | AV <sub>DD</sub>    | AGND                                | Short together                   |  | AGND                                      | 9, 16      |
|                    | AIN  | 1+R <sub>a</sub> /R <sub>b</sub> | AV <sub>DD</sub>    | Mid R <sub>a</sub> & R <sub>b</sub> | Short together to R <sub>a</sub> |  | AGND                                      | 10, 15, 16 |
|                    | AIN  | External V <sub>REF</sub>        | AV <sub>DD</sub> /2 | AV <sub>DD</sub>                    | External                         | NC   | AGND                                      | 10, 15, 16 |
| Center span        | AIN  | 1 V                              | AV <sub>DD</sub> /2 | Short together                      |                                  |  | Short together to the common mode voltage | 8, 14      |
|                    | AIN  | 2 V                              | AV <sub>DD</sub> /2 | AGND                                | NC                               |  |   | 9, 14      |
|                    | AIN  | 1+R <sub>a</sub> /R <sub>b</sub> | AV <sub>DD</sub> /2 | Mid R <sub>a</sub> & R <sub>b</sub> | R <sub>a</sub>                   |  |   | 10, 14     |
|                    | AIN  | V <sub>REF</sub>                 | AV <sub>DD</sub> /2 | AV <sub>DD</sub>                    | External                         |  |   | 11, 14     |
| External reference | AIN  | 2 V max                          | AGND                | See Note 1                          | See Note 1                       | Voltage within supply (REFTS–REBS) = 2 V max |   | 12, 13     |
| Differential input | AIN is input 1<br>REFTS & REFBS are shorted together for input 2 | 1 V                              | AV <sub>DD</sub> /2 | Short together                      |                                  |  | Short together AV <sub>DD</sub> /2        | 17         |
|                    |  | 2 V                              | AV <sub>DD</sub> /2 | AGND                                | NC                               |  |   |            |
|                    |  | V <sub>REF</sub>                 | AV <sub>DD</sub> /2 | AV <sub>DD</sub>                    | External                         |  |   |            |

NOTE 1: In external reference mode, V<sub>REF</sub> can be available for external use with CENTER SPAN setup.

### reference operations

#### V<sub>REF</sub>-pin reference

The voltage reference sources on the V<sub>REF</sub> pin are controlled by the REFSENSE pin as shown in Table 2.

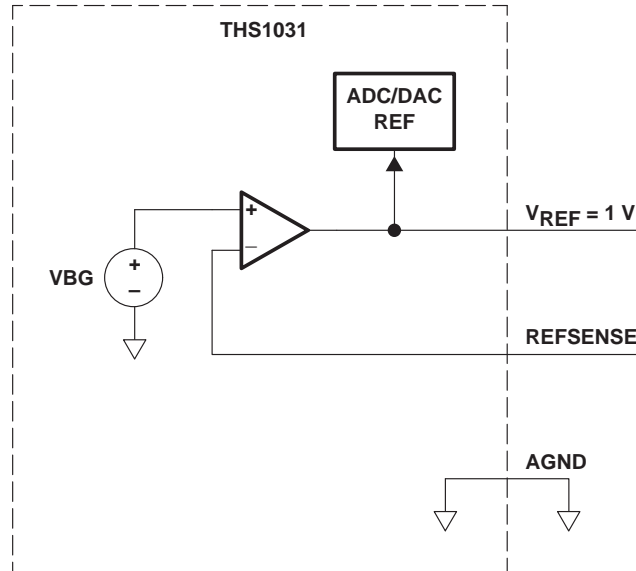
**Table 2. V<sub>REF</sub> Reference Selection**

| REFSENSE                                  | V <sub>REF</sub>   |
|---|--|
| AGND                                      | 2 V  |
| AV <sub>DD</sub>                          | The internal reference is disabled and an external reference should be connected to V <sub>REF</sub> pin if mode = AV <sub>DD</sub> /2 |
| Short to V <sub>REF</sub>                 | 1 V  |
| Connect to R <sub>a</sub> /R <sub>b</sub> | 1+R <sub>a</sub> /R <sub>b</sub>   |

**PRINCIPLES OF OPERATION**

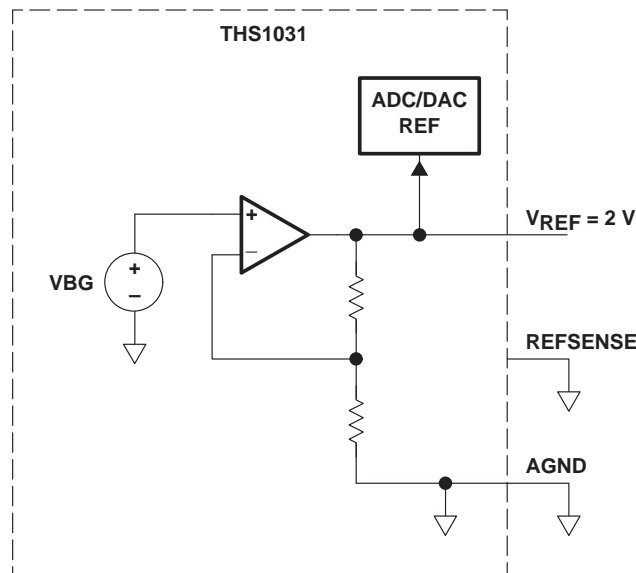
**reference operations (continued)**

- 1-V reference: The internal reference may be set to 1 V by connecting REFSENSE to  $V_{REF}$ .



**Figure 11.  $V_{REF}$  1-V Reference Mode**

- 2-V reference: The internal reference may be set to 2 V by connecting REFSENSE to AGND.

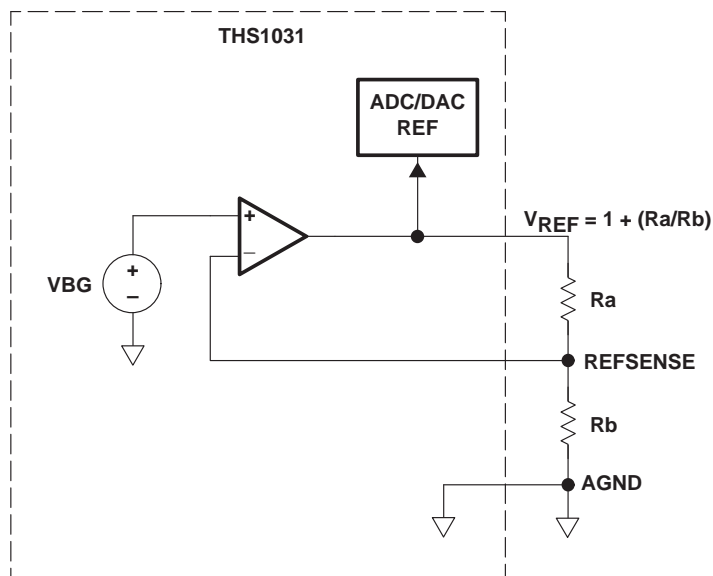


**Figure 12.  $V_{REF}$  2-V Reference Mode**

**PRINCIPLES OF OPERATION**

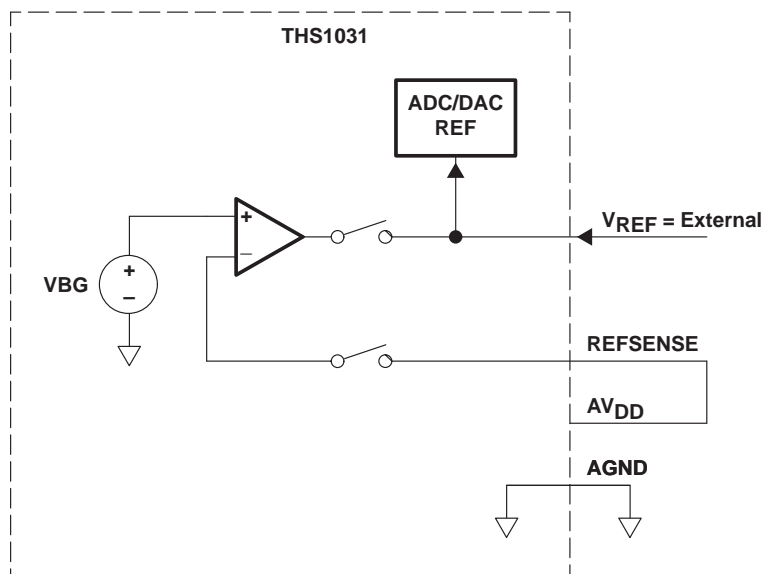
**reference operations (continued)**

- External divider: The internal reference can be set to a voltage between 1 V and 2 V by adding external resistors.



**Figure 13.  $V_{REF}$  External Divider Reference Mode**

- External reference: The internal reference may be overridden by using an external reference. This condition is met by connecting REFSENSE to  $AV_{DD}$  and an external reference circuit to the  $V_{REF}$  pin.



**Figure 14.  $V_{REF}$  External Reference Mode**

PRINCIPLES OF OPERATION

reference operations (continued)

ADC reference

The MODE pin is used to select the reference source for the ADC.

- **Internal ADC Reference:** Connect the MODE pin to  $AV_{DD}$  to use the reference source for ADC generated on the  $V_{REF}$  pin. (See  $V_{REF}$  REFERENCE described in Table 2) such that  $(REFTF-REFBF) = V_{REF}$  and  $(REFTF+REFBF)/2$  is set to a voltage for optimum operation of the ADC (near  $AV_{DD}/2$ ).
- **External ADC Reference:** To supply an external reference source to the ADC, connect the MODE pin to AGND. An external reference source should be connected to REFTF/REFTS and REFBF/REFBS. MODE = AGND closes internal switches to allow a Kelvin connection through REFBS/REFBS, and disables the on-chip amplifiers which drive on to the ADC references. Differential input is not supported

analog input mode

single-ended input

The single-ended input can be configured to work with either an external ADC reference or internal ADC reference.

- **External ADC Reference Mode:** A single-ended analog input is accepted at the AIN pin where the input signal is bounded by the voltages on the REFTS and REFBS pins. Figure 15 shows an example of applying external reference to REFTS and REFBS pins in which REFTS is connected to the low-impedance 2-V source and REFBS is connected to the low-impedance 2-V source. REFTS and REFBS may be driven to any voltage within the supply as long as the difference  $(REFTS - REFBS)$  is between 1 V and 2 V as specified in Table 2. Figure 16 shows an example of external-reference using a Kelvin connection to eliminate line voltage drop errors.

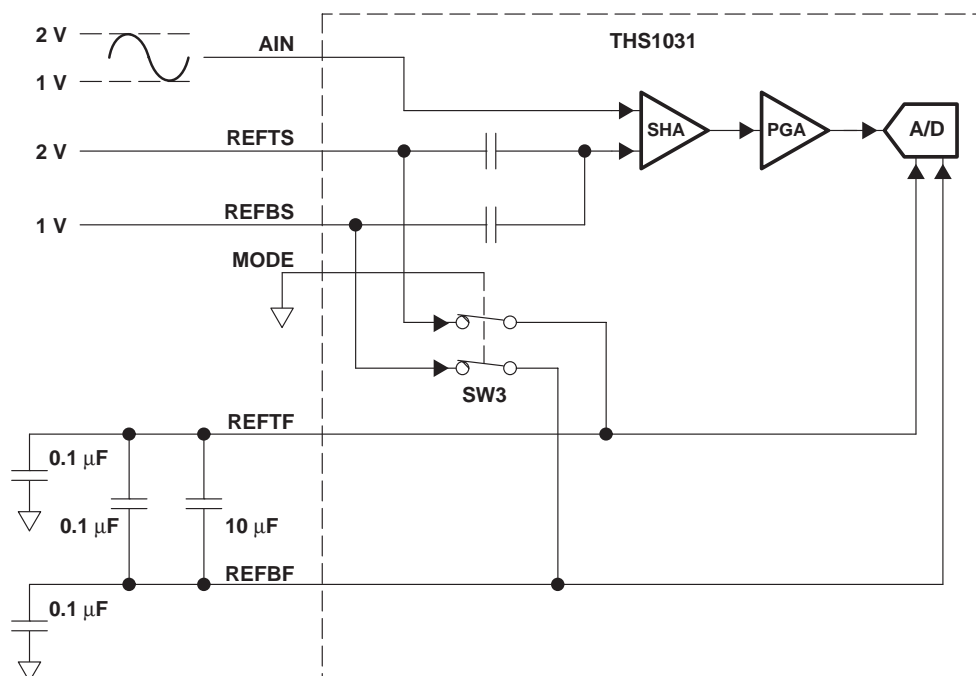


Figure 15. External ADC Reference Mode





PRINCIPLES OF OPERATION

analog input mode(continued)

- **Internal ADC Reference Mode With Common Mode Input  $V_{REF}/2$ :** The input common mode is set to  $V_{REF}/2$  by connecting REFTS to  $V_{REF}$  and REFBS to  $AV_{SS}$ . The input signal at AIN will swing between  $V_{REF}$  and  $AV_{SS}$ .

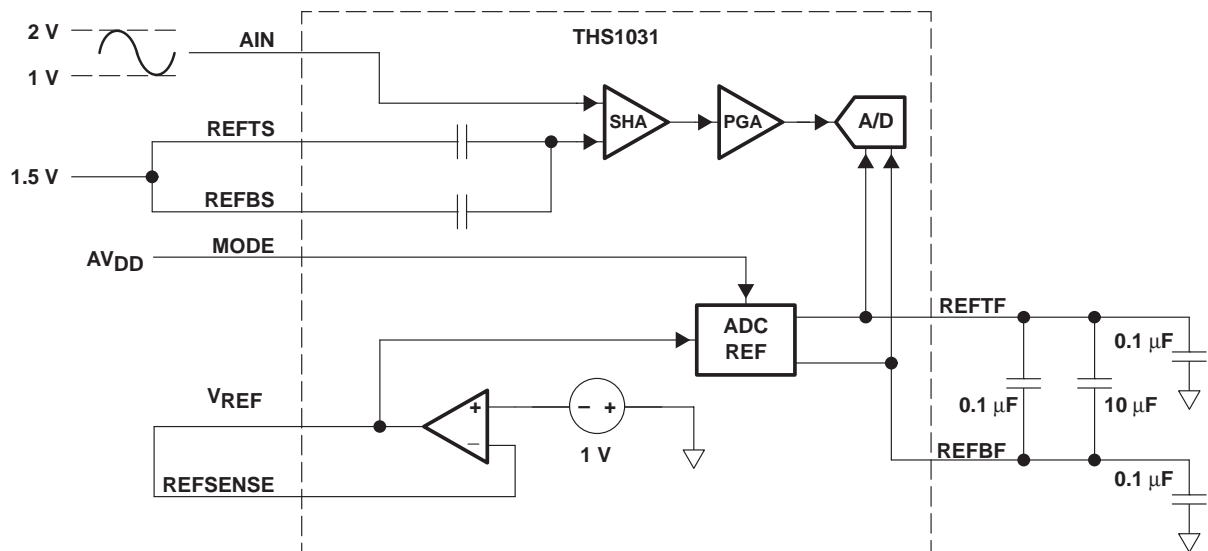


Figure 18. Common Mode Input  $V_{REF}/2$  With 1-V Internal Reference

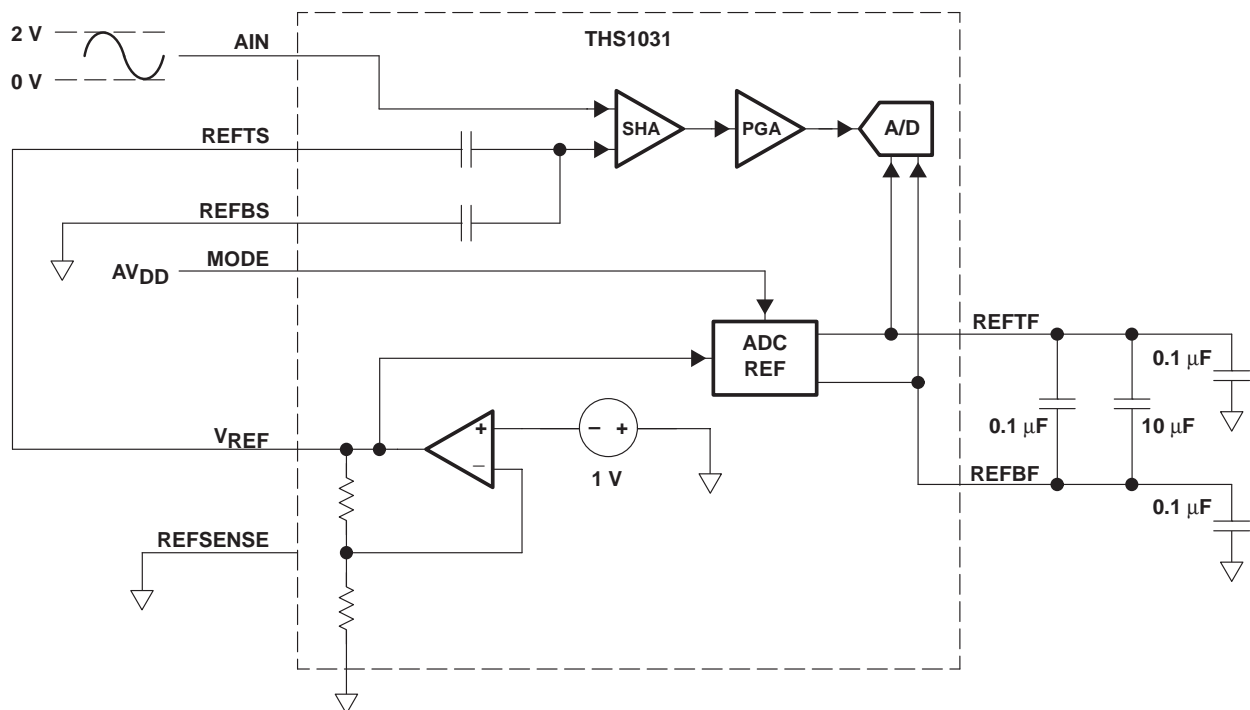


Figure 19. Common Mode Input  $V_{REF}/2$  With 2-V Internal Reference

## PRINCIPLES OF OPERATION

### analog input mode(continued)

#### differential input

In this mode, the first differential input is applied to the AIN pin and the second differential input is applied to the common point where REFTS and REFBS are tied together. The common mode of the input should be set to  $AV_{DD}/2$  as shown in Figure 20. The maximum magnitude of the differential input signal should be equal to  $V_{REF}$ .

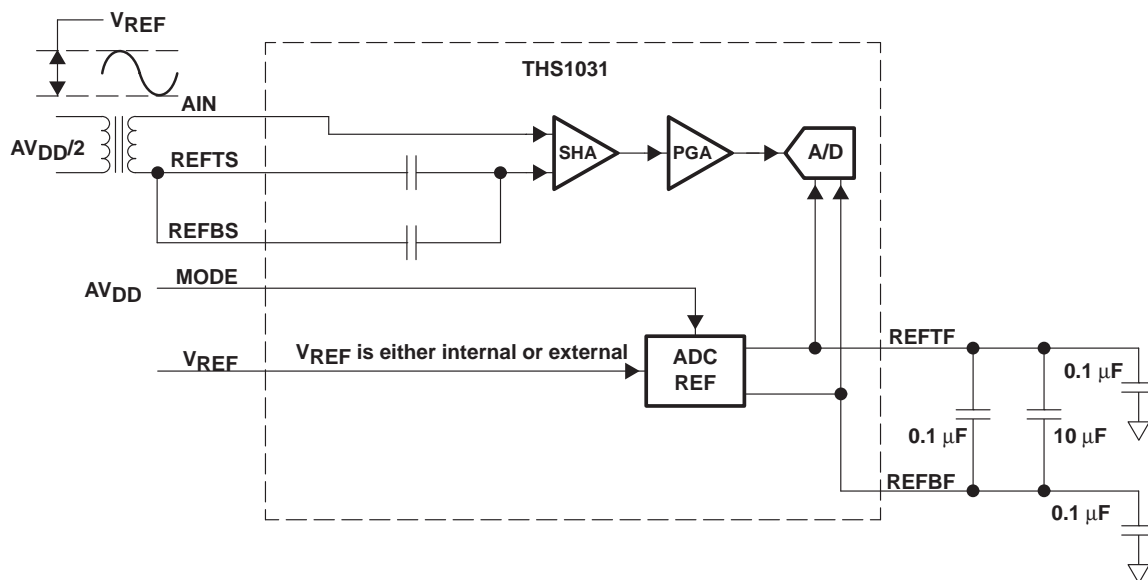


Figure 20. Differential Input

#### digital input mode

The THS1031 contains 4 registers: two CLAMP registers, a CONTROL register, and a TEST register. The TEST register is reserved for test purposes. Binary data can be written into the CLAMP and CONTROL registers via I/O0–I/O9 by inserting an active-low write strobe to the WR input pin and an active-low signal to the OE input pin. This will disable the ADC's output bus. The two MSBs of each register are address bits. For example, set bit 9 and bit 8 to 00 to select the clamp register 1. Set bit 9 and bit 8 to 01 to select the clamp register 2.

#### clamp registers

The internal digital clamp circuit uses a 10-bit DAC to convert the 10-bit digital value into the analog clamp level in which the clamp register 1 contains 8 LSBs of DAC(7:0). The clamp register 2 contains two MSBs of the DAC(9:8). **DAC(9:8)** (Default = 00): For clamping purpose, the entire range of voltage reference  $V_{REF}$  is divided into 4 quarters which can be selected by bit 0 (DAC8) and bit 1 (DAC9) in the clamp register 2. The user can clamp to any of 256-dc levels within each quarter determined by the 8-bit content of the clamp register 1. Figure 21 shows how the DACs 10-bit digital input map to the analog clamping range from 0 V to  $V_{REF}$ .

- **Clamp Register 1**

|   |   |      |      |      |      |      |      |      |      |
|---|---|------|------|------|------|------|------|------|------|
| 9 | 8 | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| 0 | 0 | DAC7 | DAC6 | DAC5 | DAC4 | DAC3 | DAC2 | DAC1 | DAC0 |

- **Clamp Register 2**

|   |   |   |   |   |   |   |   |      |      |
|---|---|---|---|---|---|---|---|------|------|
| 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
| 0 | 1 | X | X | X | X | X | X | DAC9 | DAC8 |

PRINCIPLES OF OPERATION

digital input mode (continued)

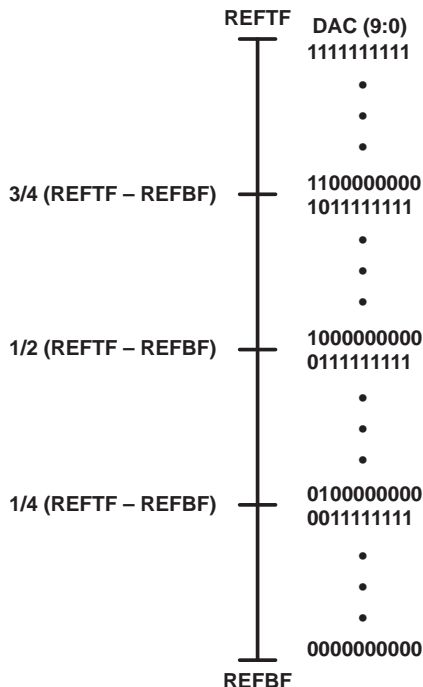


Figure 21. Digital Clamp Input Range

control register

|   |   |   |               |                |               |            |      |      |      |
|---|---|---|---------------|----------------|---------------|------------|------|------|------|
| 9 | 8 | 7 | 6             | 5              | 4             | 3          | 2    | 1    | 0    |
| 1 | 0 | X | Clamp Disable | Bin/2's Output | INT/EXT Clamp | Power Down | PGA2 | PGA1 | PGA0 |

- **Clamp Disable:** (Default = 0) Set bit 6 to 1 to disable the internal clamp amplifier for power savings.
- **BIN/2s Output:** (Default is straight binary) Set bit 5 to 0 to set the output data format to straight binary or set bit 5 to 1 to set the output data format to 2s complement.
- **INT/EXT Clamp:** (Default = 0) Set bit 4 of the CONTROL register to 0 to select the external analog clamp or set bit 4 to 1 to select the internal digital clamp whose clamp level is defined in the clamp register described above.
- **Power Down:** (Default = 0) Set bit 3 of the CONTROL register to 1 to power down the THS1031.

## PRINCIPLES OF OPERATION

### digital input mode (continued)

- **PGA(2–0):** (Default = 001) 3-bit gain for programmable gain amplifier can be set as indicated in the following table:

| PGA[2–0] | GAIN       |
|----------|------------|
| 000      | 0.5        |
| 001      | Unity gain |
| 010      | 1.5        |
| 011      | 2.0        |
| 100      | 2.5        |
| 101      | 3.0        |
| 110      | 3.5        |
| 111      | 4.0        |

### test register (reserved)

|   |   |   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|---|---|
| 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 1 | X | X | X | X | X | X | X | X |

### digital output mode

- **3-State Output:** The digital outputs can be set to high-impedance state by applying a Hi logic to the  $\overline{OE}$  pin.
- **Output Format:** Defined by bit 5 of the CONTROL register. The output format is straight binary if bit 5 set to 0. The output format is 2s complement if bit 5 is set to 1. *The default format is straight binary.*

### clamp operation

The THS1031 ADC features an internal clamp circuit for dc restoration of video or ac coupled signals. The clamp input level can come from either an external source or an internal digital clamp circuit containing a 10-bit DAC and clamp register.

- **External Clamp Input:** To enable the external clamp input source, use the default state on power up or write a 0 to bit 4 of the PGA/CONTROL register. This will connect the switch SW2 to the CLAMPIN pin. The clamp amplifier will then servo the voltage at the AIN pin to be equal to the clamp voltage applied at the CLAMPIN pin. After the desired clamp level is attained, the switch SW1 is opened by taking CLAMP back to logic low. Ignoring the droop caused by the input bias current, the input capacitor C<sub>IN</sub> will hold the DC voltage at AIN constant until the next clamp interval. The input resistor R<sub>IN</sub> has a minimum recommended value of 10 W, to maintain the closed-loop stability of the clamp amplifier.
- **Internal Programmable Digital Clamp Input:** The THS1031 ADC features a programmable digital clamp circuit to set more precise clamping level to 1-LSB accuracy for dc restoration of video or ac coupled signals. Figure 22 shows the internal clamp circuitry and the external control signals needed for the digital clamp operation. To enable the digital clamp input source, write a 1 to bit 4 of the CONTROL register which will connect the switch SW2 to the output of the 10-bit clamp DAC. In the CLAMP register, bit 0 to bit 7 are used to set the clamp level input to the 10-bit DAC and bit 6–7 are used to select one of 4 equal clamping voltage sub-ranges as described in the description of CLAMP REGISTER for digital input mode. The clamp amplifier will then servo the voltage at the AIN pin to be equal to the clamp voltage applied at the CLAMPIN pin. After the desired clamp level is attained, the switch SW1 is opened by taking CLAMP back to logic low. Ignoring the droop caused by the input bias current, the input capacitor C<sub>IN</sub> will hold the dc voltage at AIN constant until the next clamp interval. The input resistor R<sub>IN</sub> has a minimum recommended value of 10 W, to maintain the closed-loop stability of the clamp amplifier.

PRINCIPLES OF OPERATION

clamp operation (continued)

● Clamp and Droop Analysis

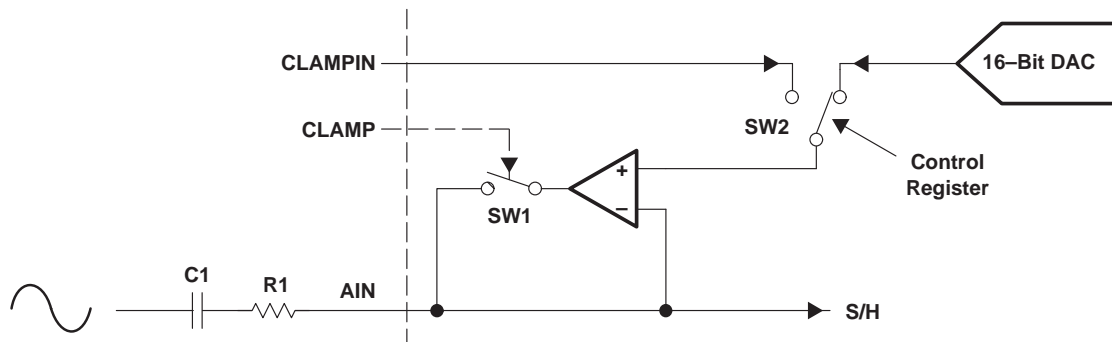


Figure 22. Clamp Operation

- **Clamp Acquisition Time:** Figure 22 shows the basic operation of the clamp circuit in which the ac input signal is passed through an RC coupler.

The acquisition time when the switch is closed will equal a:  $T(acq) = C_i \cdot R_i \ln(V_c/V_e)$  (Eq. 1)

In case of composite video, typical input  $R_i = 20 \Omega$ . In a video clamping application, the droop is a critical parameter and thus the input capacitor should be sized to allow sufficient acquisition time of clamp voltage at AIN within the CLAMP interval, but also to minimize droop between clamping intervals. Typically,  $C_i = 1 \mu F$

By applying equation 1 above, the following examples apply to an NTSC composite video signal:

- The acquisition time needed to clamp 1-V input level to black level (0.340 Vdc) is about 130  $\mu s$ .
- The acquisition time needed to clamp 2-V input level to the white level (1 Vdc) is about 140  $\mu s$ .
- The acquisition time needed to clamp 3-V input level to the sync level (0.288 Vdc) is about 160  $\mu s$ .

droop

The voltage droop is the voltage change across the input capacitor  $C_i$  by the bias current as follows:

$$dV = (I_{bias}/C_i)(t)$$

where  $t$  = elapsed time between clamping intervals

The bias current depends on the sampling rate. For a sampling rate of 30 MSPS and a typical input capacitance of 1 pF, the input resistance is

$$R_s = 1/(C_s \cdot F_s) = 1/(1 \text{ pF} \times 30 \text{ MHz}) = 33 \text{ k}\Omega$$

For 1-V input range and clamping period = 64  $\mu s$ , the max bias current will equal  $I_{bias} = 0.5 \text{ V}/33 \text{ k}\Omega = 15 \mu A$ :

$$dV = (15 \mu A/1 \mu F)(64 \mu s) = 0.96 \text{ mV}$$

For 1-V input range and clamping period = 64  $\mu s$ , the max bias current will equal  $I_{bias} = 0.5 \text{ V}/33 \text{ k}\Omega = 15 \mu A$ :

$$dV = (15 \mu A/1 \mu F)(64 \mu s) = 0.96 \text{ mV}$$

For 2-V input range and clamping period = 64  $\mu s$ , the max bias current will equal  $I_{bias} = 1.0 \text{ V}/33 \text{ k}\Omega = 30 \mu A$

$$dV = (30 \mu A/1 \mu F)(64 \mu s) = 1.9 \text{ mV}$$

## PRINCIPLES OF OPERATION

### clamp operation (continued)

#### requirements

For a single direct source of NTSC video,

- The initial clamp acquisition time needs to be between 130  $\mu$ s and 160  $\mu$ s to set the input dc level within 1 mV accuracy.
- The clamp pulse at CLAMP is recommended to be 2  $\mu$ s (typ).
- The droop voltage needs to be compensated within one clamping period of 64  $\mu$ s for 1 V and 2 V. Input ranges are 1 mV and 1.9 mV respectively which are less than 1 LSB.

#### power management

Upon power up, the THS1031 is put in the default mode. In the default mode, the PGA (PGA bypass) and the clamp DAC are powered down which adds to the device's flexibility. The users need not incur the penalty of having to provide power for a certain section if it is not necessary to their design.

When bit 3 of PGA/control register is set to 1, the entire device is powered down. The ADC will wake-up in 400 ns (typ) after the bit 3 is reset.

**THS1031**  
**2.7 V – 5.5 V, 10-BIT, 30 MSPS**  
**CMOS ANALOG-TO-DIGITAL CONVERTER**

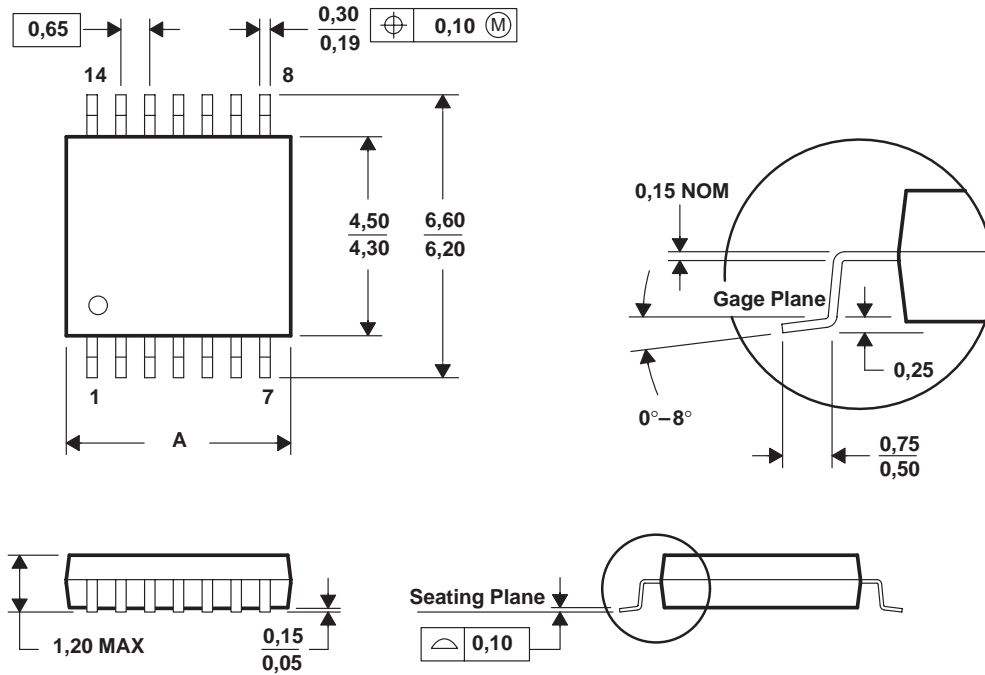
SLAS242A – NOVEMBER 1999 – REVISED JANUARY 2000

**MECHANICAL DATA**

**PW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

14 PINS SHOWN



| DIM \ PINS ** | PINS ** |      |      |      |      |      |
|---------------|---------|------|------|------|------|------|
|               | 8       | 14   | 16   | 20   | 24   | 28   |
| A MAX         | 3,10    | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN         | 2,90    | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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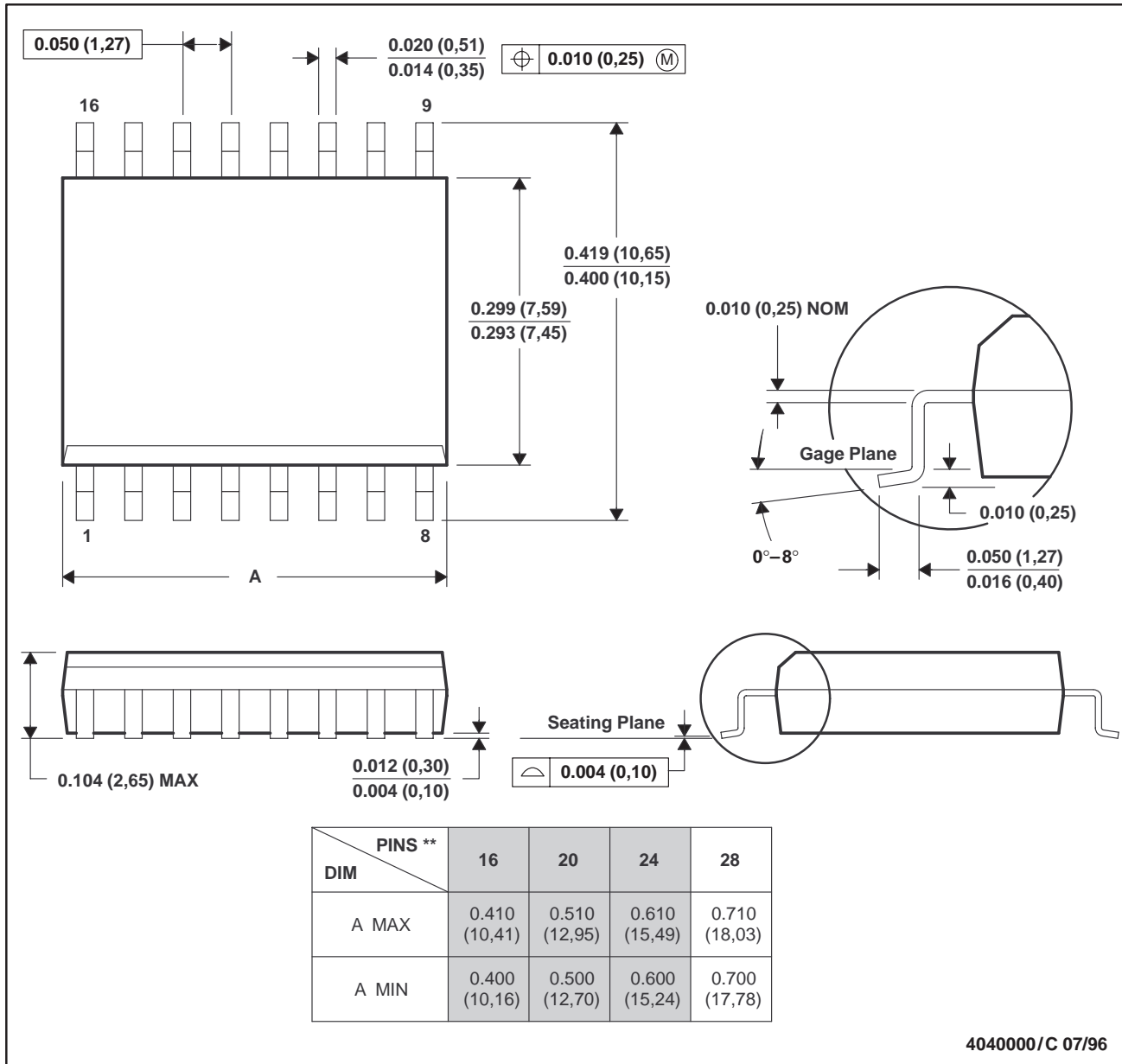


**MECHANICAL DATA**

**DW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

**16 PINS SHOWN**



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013

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