

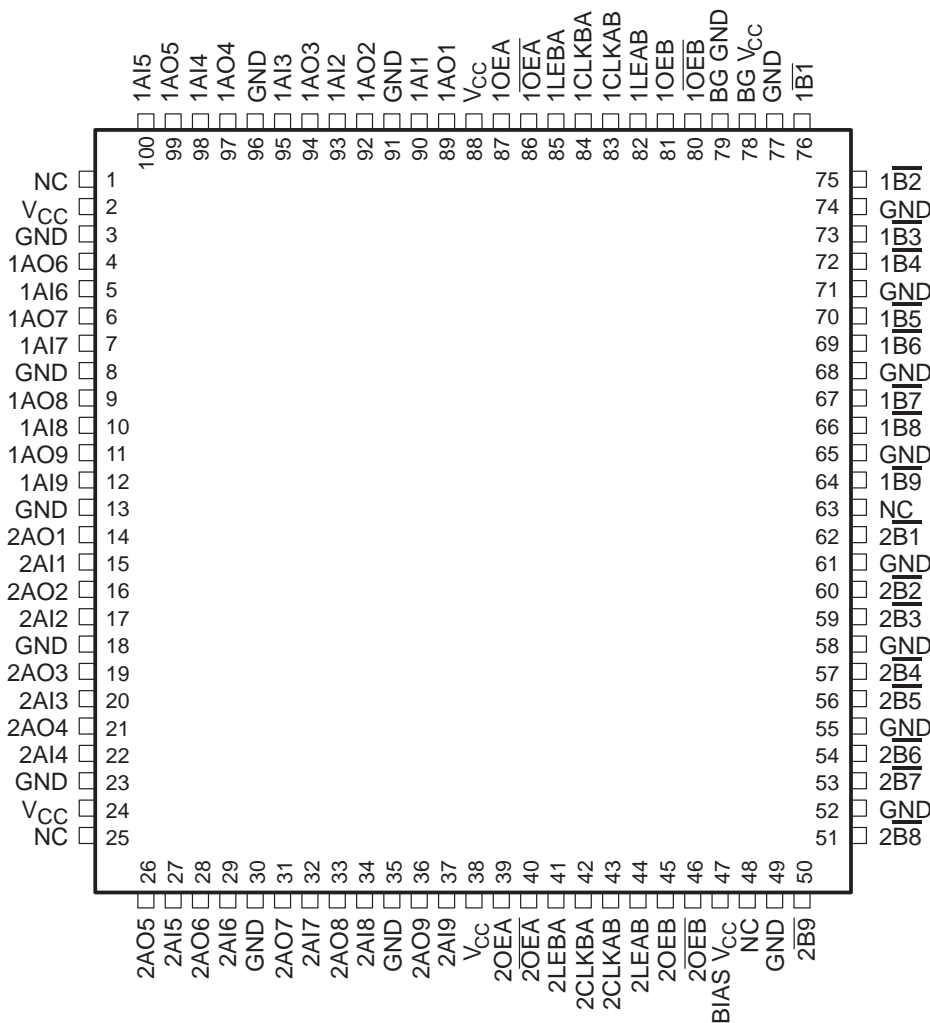
# SN74FB1650

## 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVER

SCBS178L – AUGUST 1992 – REVISED SEPTEMBER 1999

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL)  $\bar{B}$  Port**
- **Open-Collector  $\bar{B}$ -Port Outputs Sink 100 mA**
- **BIAS  $V_{CC}$  Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\bar{B}$ -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL Input Structures Incorporate Active Clamping to Aid in Line Termination**
- **Packaged in Plastic High-Power Low-Profile Quad Flatpack**

**PCA PACKAGE  
(TOP VIEW)**



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

# SN74FB1650

## 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVER

SCBS178L – AUGUST 1992 – REVISED SEPTEMBER 1999

### description

The SN74FB1650 device contains two 9-bit transceivers designed to translate signals between TTL and backplane transceiver-logic (BTL) environments. It is designed specifically to be compatible with IEEE Std 1194.1-1991.

The  $\bar{B}$  port operates at BTL-signal levels. The open-collector  $\bar{B}$  ports are specified to sink 100 mA. Two output enables (OEB and  $\overline{OEB}$ ) are provided for the  $\bar{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is less than 2.1 V, the  $\bar{B}$  port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the  $\bar{B}$  port when the A-port output enable (OEA) is high. When OEA is low or when  $V_{CC}$  is less than 2.1 V, the A outputs are in the high-impedance state.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

BG  $V_{CC}$  and BG GND are the supply inputs for the bias generator.

The SN74FB1650 is characterized for operation from 0°C to 70°C.

### Function Tables

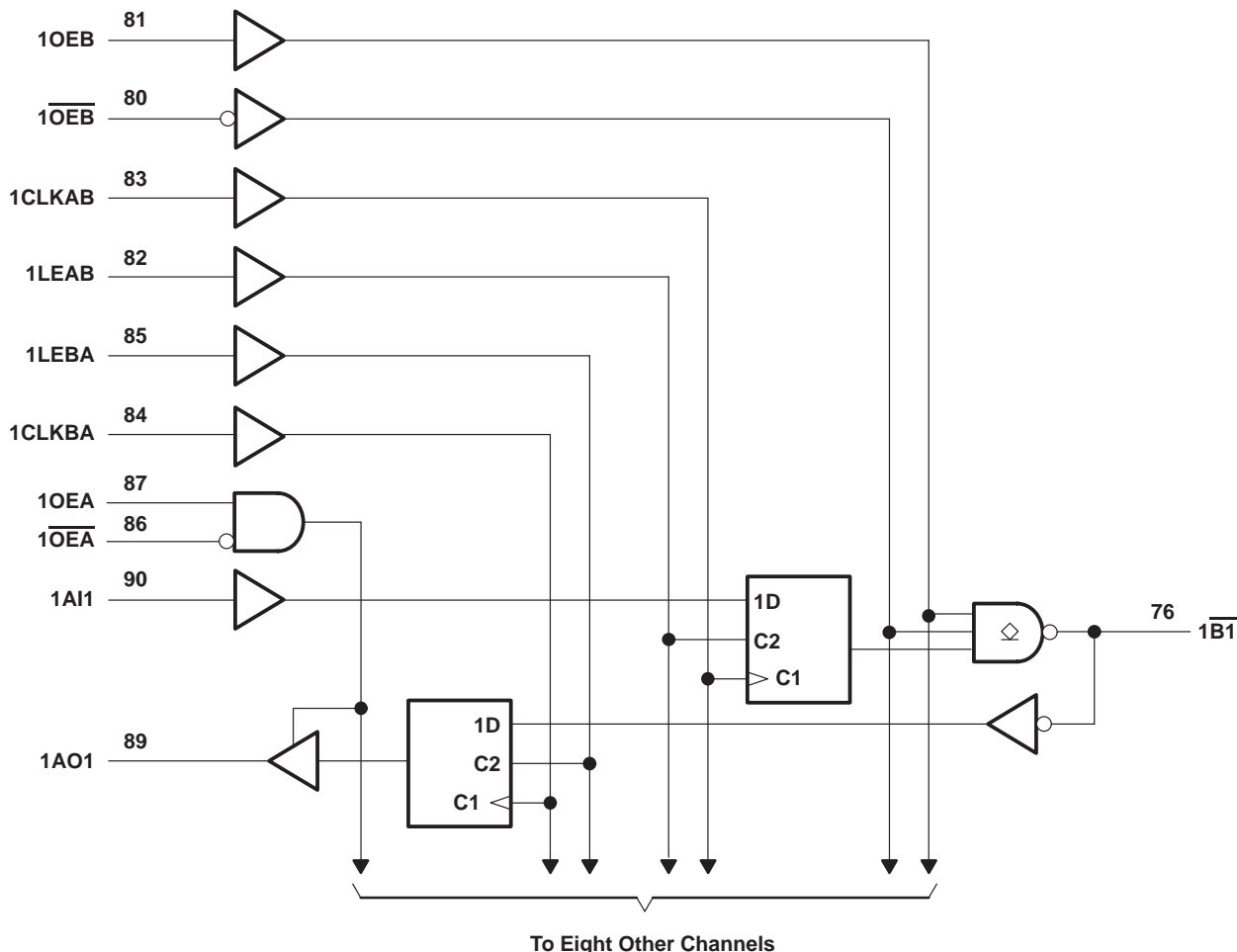
#### TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\bar{A}$ data to B bus
L	H	X	X	$\bar{B}$ data to A bus
L	H	H	L	$\bar{A}$ data to B bus, $\bar{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

#### STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

**functional block diagram**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ , BIAS $V_{CC}$ , BG $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ : Except $\bar{B}$ port .....	-1.2 V to 7 V
$\bar{B}$ port .....	-1.2 V to 3.5 V
Voltage range applied to any $\bar{B}$ output in the disabled or power-off state, $V_O$ .....	-0.5 V to 3.5 V
Voltage range applied to any output in the high state, $V_O$ .....	-0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ : Except $\bar{B}$ port .....	-40 mA
$\bar{B}$ port .....	-18 mA
Current applied to any single output in the low state, $I_O$ : A port .....	48 mA
$\bar{B}$ port .....	200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1) .....	22°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

# SN74FB1650

## 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVER

SCBS178L – AUGUST 1992 – REVISED SEPTEMBER 1999

### recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
$V_{CC}$ , BG $V_{CC}$ , BIAS $V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$\overline{B}$ port	1.62	2.3	V
		Except $\overline{B}$ port	2		
$V_{IL}$	Low-level input voltage	$\overline{B}$ port	0.75	1.47	V
		Except $\overline{B}$ port		0.8	
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-3	mA
$I_{OL}$	Low-level output current	A port		24	mA
		$\overline{B}$ port		100	
$T_A$	Operating free-air temperature	0		70	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$\overline{B}$ port	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2	V
	Except $\overline{B}$ port	$V_{CC} = 4.5$ V,	$I_I = -40$ mA			-0.5	
$V_{OH}$	AO port	$V_{CC} = 4.5$ V	$I_{OH} = -1$ mA				V
			$I_{OH} = -3$ mA	2.5	3.3		
$V_{OL}$	AO port	$V_{CC} = 4.5$ V,	$I_{OL} = 24$ mA		0.35	0.5	V
	$\overline{B}$ port	$V_{CC} = 4.5$ V	$I_{OL} = 80$ mA	0.75	1.1		
			$I_{OL} = 100$ mA			1.15	
$I_I$	Except $\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 5.5$ V			50	μA
$I_{IH}‡$	Except $\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			50	μA
$I_{IL}‡$	Except $\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V			-50	μA
	$\overline{B}$ port	$V_{CC} = 5.5$ V,	$V_I = 0.75$ V			-100	
$I_{OZH}$	AO port	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50	μA
$I_{OZL}$	AO port	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			-50	μA
$I_{OZPU}$	AO port	$V_{CC} = 0$ to 2.1 V,	$V_O = 0.5$ V to 2.7 V			50	μA
$I_{OZPD}$	AO port	$V_{CC} = 2.1$ V to 0,	$V_O = 0.5$ V to 2.7 V			-50	μA
$I_{OH}$	$\overline{B}$ port	$V_{CC} = 0$ to 5.5 V,	$V_O = 2.1$ V			100	μA
$I_{OS}§$	A port	$V_{CC} = 5.5$ V,	$V_O = 0$	-30		-150	mA
$I_{CC}$	A port to $\overline{B}$ port	$V_{CC} = 5.5$ V,	$I_O = 0$			100	mA
	$\overline{B}$ port to A port					120	
$C_i$	A1 port	$V_I = V_{CC}$ or GND			5.5		pF
	Control inputs				5.5		
$C_O$	AO ports	$V_O = V_{CC}$ or GND			5.5		pF
$C_{iO}$	$\overline{B}$ port per IEEE Std 1194.1-1991	$V_{CC} = 0$ to 5.5 V				5.5	pF

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN74FB1650

## 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVER

SCBS178L – AUGUST 1992 – REVISED SEPTEMBER 1999

### live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0$ to 4.5 V	$V_B = 0$ to 2 V,	$V_I$ (BIAS $V_{CC}$ ) = 4.5 V to 5.5 V	450		$\mu A$
	$V_{CC} = 4.5$ V to 5.5 V			10		
$V_O$	$\bar{B}$ port	$V_{CC} = 0$ ,	$V_I$ (BIAS $V_{CC}$ ) = 5 V	1.62	2.1	V
$I_O$	$\bar{B}$ port	$V_{CC} = 0$ ,	$V_B = 1$ V,	$V_I$ (BIAS $V_{CC}$ ) = 4.5 V to 5.5 V		-1
		$V_{CC} = 0$ to 5.5 V,	OEB = 0 to 0.8 V			100
		$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V			100

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5$ V, $T_A = 25^\circ C$		MIN	MAX	UNIT
			MIN	MAX			
$f_{clock}$	Clock frequency		150			150	MHz
$t_w$	Pulse duration	CLK or LE	3.3			3.3	ns
$t_{su}$	Setup time	Data before LE	4.8			4.8	ns
		Data before CLK $\uparrow$	4.9			4.9	
$t_h$	Hold time	Data after LE	1.8			1.8	ns
		Data after CLK $\uparrow$	1.1			1.1	



# SN74FB1650

## 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVER

SCBS178L – AUGUST 1992 – REVISED SEPTEMBER 1999

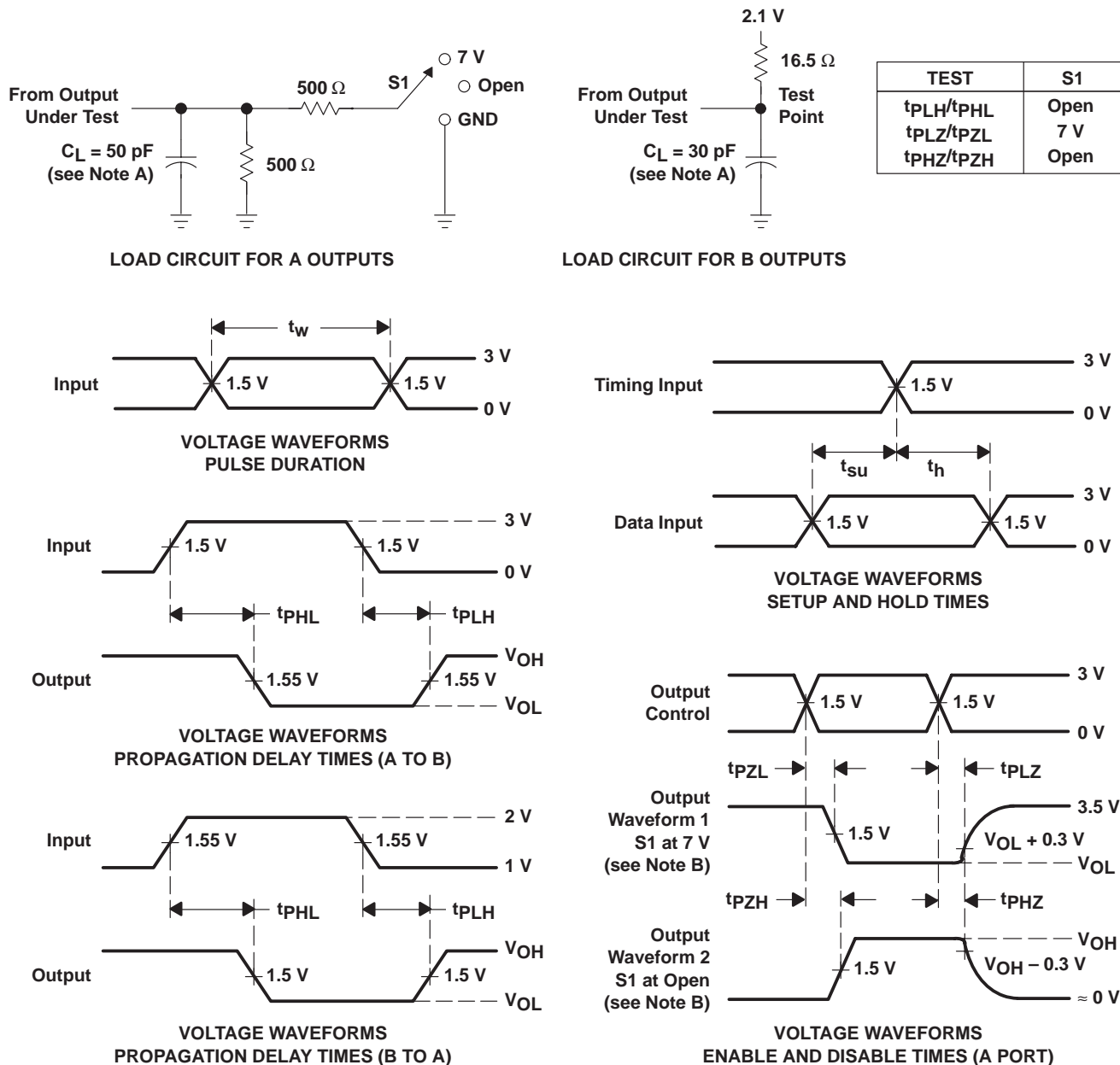
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			150			150		MHz
t <sub>PLH</sub>	AI	$\overline{B}$	1.8	3.7	5.3	1.8	6.2	ns
t <sub>PHL</sub>			2.9	4.4	6	2.9	7.2	
t <sub>PLH</sub>	LEAB	$\overline{B}$	2.7	4.2	5.8	2.7	6.4	ns
t <sub>PHL</sub>			3.5	5	6.5	3.5	7.3	
t <sub>PLH</sub>	CLKAB	$\overline{B}$	2.3	3.9	5.5	2.3	6	ns
t <sub>PHL</sub>			2.9	4.5	6.1	2.9	6.7	
t <sub>PLH</sub>	$\overline{B}$	AO	3.5	5.9	7.9	3.5	8.6	ns
t <sub>PHL</sub>			2.2	3.7	5.3	2.2	5.7	
t <sub>PLH</sub>	LEBA	AO	1.8	3.2	4.6	1.8	5.1	ns
t <sub>PHL</sub>			1.7	3	4.4	1.7	4.7	
t <sub>PLH</sub>	CLKBA	AO	1.8	3.1	4.6	1.8	5.1	ns
t <sub>PHL</sub>			1.7	3.1	4.6	1.7	4.9	
t <sub>PLH</sub>	OEB	$\overline{B}$	2.7	4.6	6.4	2.7	6.7	ns
t <sub>PHL</sub>			2.9	4.1	5.9	2.9	6.6	
t <sub>PLH</sub>	$\overline{OEB}$	$\overline{B}$	2.6	4.3	6.2	2.6	6.6	ns
t <sub>PHL</sub>			3.4	4.6	6.4	3.4	7	
t <sub>PZH</sub>	OEA	AO	1.4	2.9	4.4	1.4	4.9	ns
t <sub>PZL</sub>			1.4	2.6	4	1.4	4.6	
t <sub>PHZ</sub>	OEA	AO	1.7	3.4	5.1	1.7	5.8	ns
t <sub>PLZ</sub>			2.2	3.6	5	2.2	5.5	
t <sub>PZH</sub>	$\overline{OEA}$	AO	1.7	3.3	4.7	1.7	5.5	ns
t <sub>PZL</sub>			1.7	3.1	4.4	1.7	5.1	
t <sub>PHZ</sub>	$\overline{OEA}$	AO	1.5	2.9	4.5	1.5	5.1	ns
t <sub>PLZ</sub>			2	3.1	4.6	2	4.8	
t <sub>sk(p)</sub> <sup>†</sup>	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO		1					ns
t <sub>sk(o)</sub> <sup>†</sup>	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO		0.5					ns
t <sub>t</sub> Transition time	$\overline{B}$ outputs (1.3 V to 1.8 V)		0.9	1.7	3.1	0.5	4.6	ns
	AO outputs (10% to 90%)		0.5	2	3.6	0.4	4.2	
$\overline{B}$ -port input pulse rejection			1			1		ns

<sup>†</sup> Skew values are applicable for through mode only.



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ ; BTL inputs: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

**CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.**

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.