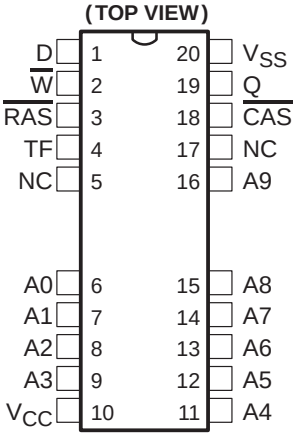
- **Organization . . . 1048576 × 1-Bit**
- **Processed to MIL-STD-883, Class B**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

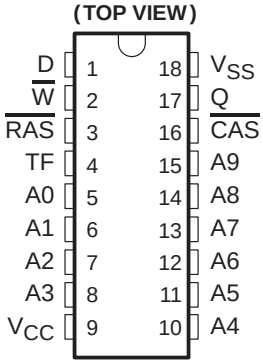
| | ACCESS TIME $t_{a(R)}$ ($t_{RAC}$) (MAX) | ACCESS TIME $t_{a(C)}$ ($t_{CAC}$) (MAX) | ACCESS TIME $t_{a(CA)}$ ($t_{AA}$) (MAX) | READ OR WRITE CYCLE (MIN) |
|---|---|---|---|---|
| '4C1024-80 | 80 ns | 20 ns | 40 ns | 150 ns |
| '4C1024-10 | 100 ns | 25 ns | 45 ns | 190 ns |
| '4C1024-12 | 120 ns | 30 ns | 55 ns | 220 ns |
| '4C1024-15 | 150 ns | 40 ns | 70 ns | 260 ns |

- **Enhanced Page-Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **One of TI's CMOS Megabit Dynamic Random-Access Memory (DRAM) Family Including SMJ44C256 — 256K × 4 Enhanced Page Mode**
- **$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR) Refresh**
- **Long Refresh Period**
  **512-Cycle Refresh in 8 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs/Outputs and Clocks Are TTL-Compatible**
- **Packaging Offered:**
  - **20/26-Pin J-Leaded Ceramic Surface Mount Package (HJ Suffix)**
  - **18-Pin 300-Mil Ceramic Dual-In-Line Package (JD Suffix)**
  - **20-Pin Ceramic Flatpack (HK Suffix)**
  - **20/26-Terminal Leadless Ceramic Surface Mount Package (FQ/HL Suffixes)**
  - **20-Pin Ceramic Zig-Zag In-Line Package (SV Suffix)**
- **Operating Temperature Range**
  **– 55°C to 125°C**

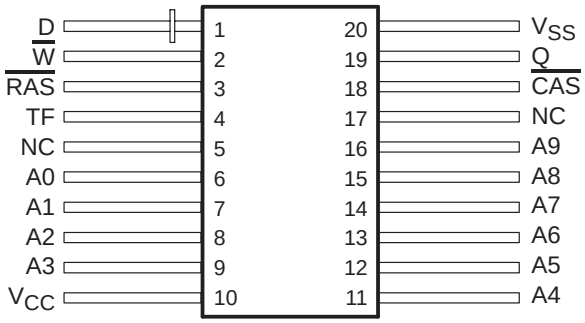
**HJ PACKAGE**
**(TOP VIEW)**



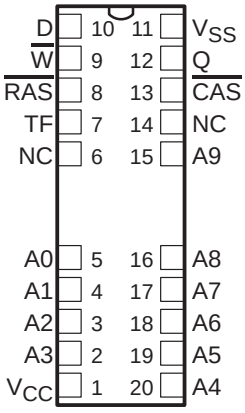

**JD PACKAGE**
**(TOP VIEW)**



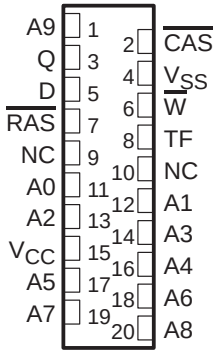

**HK PACKAGE**
**(TOP VIEW)**




**FQ/HL PACKAGES**
**(TOP VIEW)**




**SV PACKAGE**
**(SIDE VIEW)**

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| PIN NOMENCLATURE | |
|---|---|
| $\overline{A0}$–A9 | Address Inputs |
| $\overline{CAS}$ | Column Address Strobe |
| D | Data In |
| NC | No Internal Connection |
| Q | Data Out |
| $\overline{RAS}$ | Row Address Strobe |
| TF | Test Function |
| $V_{CC}$ | 5-V Supply |
| $V_{SS}$ | Ground |
| $\overline{W}$ | Write Enable |

## description

The SMJ4C1024 is a 1048576-bit DRAM organized as 1048576 words of one bit each. It employs technology for high performance, reliability, and low power at a low cost.

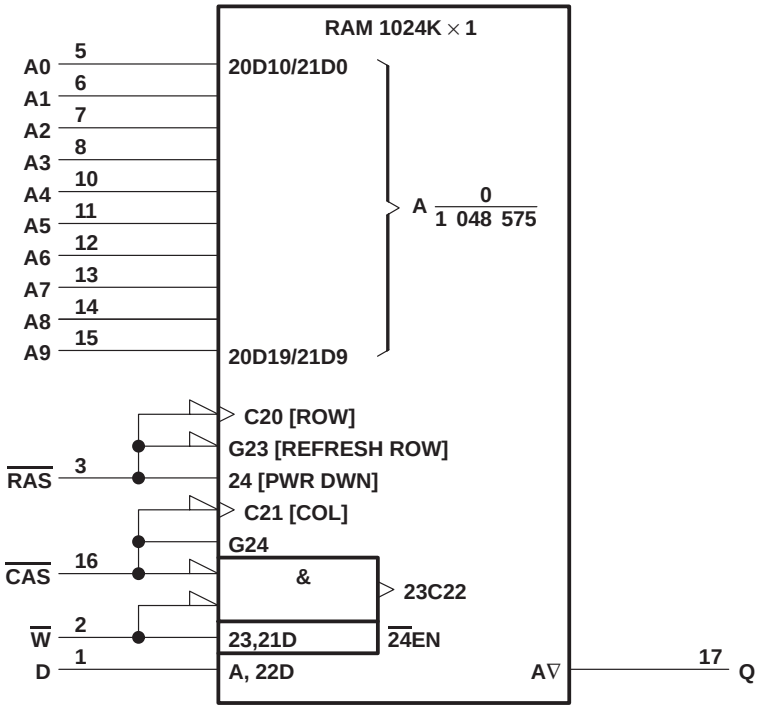
This device features maximum $\overline{RAS}$ access times of 80 ns, 100 ns, 120 ns, and 150 ns. Maximum power dissipation is as low as 305 mW operating and 16.5 mW standby on 150-ns devices.

$I_{DD}$ peaks are typIcally 140 mA and a –1 V input voltage undershoot can be tolerated, minimizing system noise.

All inputs and outputs, including clocks, are compatible with series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

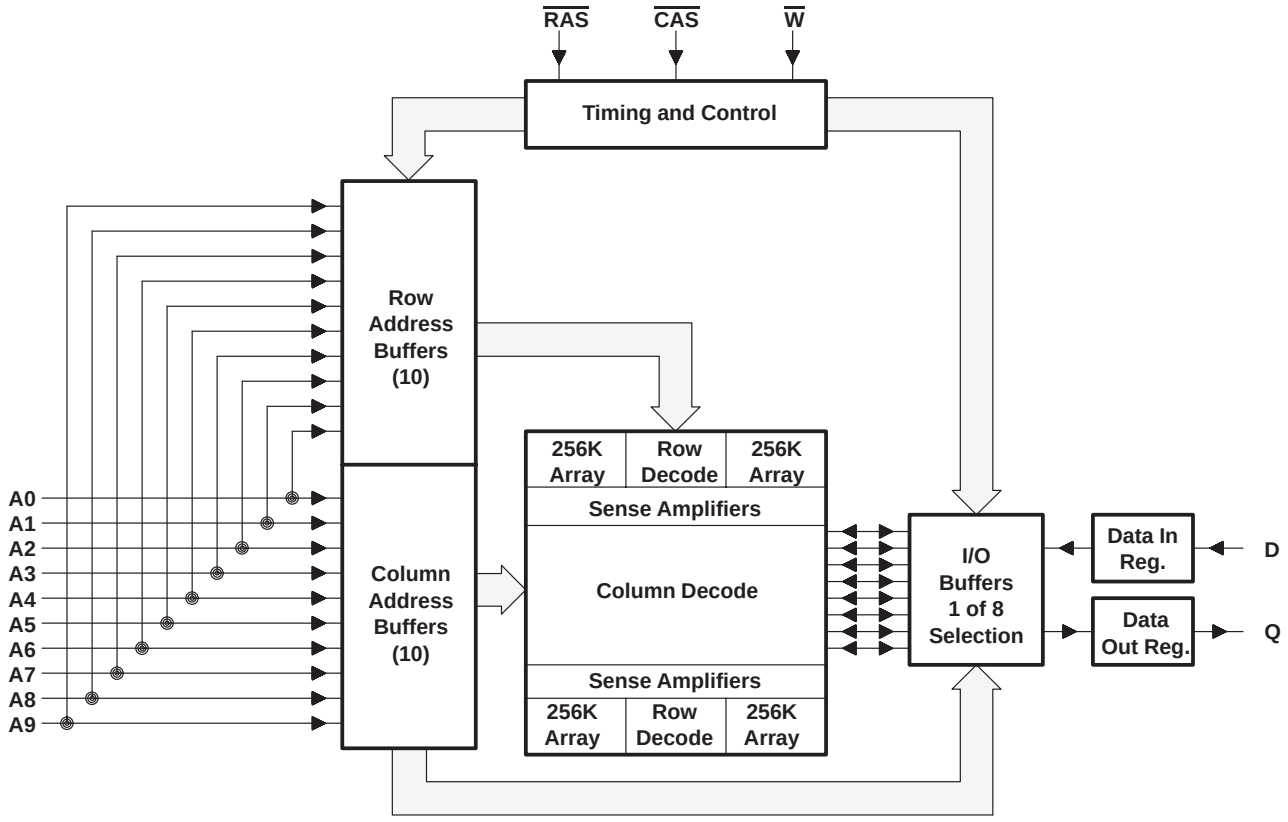
The SMJ4C1024 is offered in an 18-pin ceramic dual-in-line package (JD suffix), a 20/26-terminal leadless ceramic carrier package (FQ/HL suffixes), a 20/26-pin J-leaded carrier package (HJ suffix), a 20-pin flatpack (HK suffix), and a 20-pin ceramic zig-zag in-line package (SV suffix). They are characterized for operation from – 55°C to 125°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 18-pin JD package.

## functional block diagram




## operation

### enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and for address multiplexing is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page-cycle time used. With minimum $\overline{CAS}$ page-cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature lets the SMJ4C1024 operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ maximum (access time from $\overline{CAS}$ low) if $t_{a(CA)}$ maximum (access time from column address) has been satisfied. If the column addresses for the next page cycle are valid at the same time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(CA)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

### address (A0 – A9)

Twenty address bits are required to decode one of 1048576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by $\overline{RAS}$. The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges

**address (A0 – A9) (continued)**

of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select to activate the output buffer as well as to latch the address bits into the column-address buffer.

**write enable ($\overline{W}$)**

The read or write mode is selected through $\overline{W}$. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable pin can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting common input/output operation.

**data in (D)**

Data-in is written during a write or a read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or a read-modify-write cycle, $\overline{CAS}$ is already low, and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

**data out (Q)**

The 3-state output buffers provide direct TTL compatibility (no pullup resistor required) with a fanout of two series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid after the access time $t_{a(C)}$. The access time from $\overline{CAS}$ low ($t_{a(C)}$) begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; when $\overline{CAS}$ goes high, the output returns to a high-impedance state. In a delayed-write or read-modify-write cycle, the output follows the sequence for the read cycle.

**refresh**

A refresh operation must be performed at least once every 8 ms to retain data. This can be achieved by strobing each of the 512 rows (A0 – A8). A normal read or write cycle refreshes all bits in each selected row. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at $V_{IL}$ after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

**$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh**

CBR refresh is used by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter $t_{d(CLRL)R}$) and holding it low after $\overline{RAS}$ falls (parameter $t_{d(RLCH)R}$). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh cycles.

**power up**

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full $V_{CC}$ level is achieved.

**test function (TF) pin**

During normal device operation, TF must be disconnected or biased at a voltage ≤ $V_{CC}$.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage range on $V_{CC}$ . . . . . – 1 V to 7 V
Short-circuit output current, $I_{OS}$ . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, $T_A$ . . . . . – 55°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to $V_{SS}$.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.4 | | 6.5 | V |
| $V_{IL}$ | Low-level input voltage (see Note 2) | – 1 | | 0.8 | V |
| $T_A$ | Minimum operating free-air temperature | – 55 | | | °C |
| $T_C$ | Maximum operating case temperature | | | 125 | °C |

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | '4C1024-80 | | '4C1024-10 | | '4C1024-12 | | '4C1024-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = – 5 mA | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4.2 mA | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V |
| $I_I$ | Input current (leakage) | $V_{CC}$ = 5.5 V, $V_I$ = 0 V to 6.5 V, All other pins = 0 V to $V_{CC}$ | | ± 10 | | ± 10 | | ± 10 | | ± 10 | µA |
| $I_O$ | Output current (leakage) | $V_{CC}$ = 5.5 V, $V_O$ = 0 V to $V_{CC}$, $\overline{CAS}$ high | | ± 10 | | ± 10 | | ± 10 | | ± 10 | µA |
| $I_{CC1}$ | Read- or write-cycle current | $V_{CC}$ = 5.5 V, Minimum cycle | | 75 | | 70 | | 60 | | 55 | mA |
| $I_{CC2}$ | Standby current | After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH}$ = 2.4 V | | 3 | | 3 | | 3 | | 3 | mA |
| $I_{CC3}$ | Average refresh current ($\overline{RAS}$ only or CBR) | $V_{CC}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR) | | 70 | | 65 | | 55 | | 50 | mA |
| $I_{CC4}$ | Average page current | $V_{CC}$ = 5.5 V, $t_{PC}$ = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling | | 50 | | 45 | | 35 | | 30 | mA |

## capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

| PARAMETER | | HL / JD / FQ | | HJ | | HK | | SV | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $C_{i(A)}$ | Input capacitance, address inputs | | 6 | | 7 | | 8 | | 9 | pF |
| $C_{i(D)}$ | Input capacitance, data input | | 5 | | 5 | | 6 | | 7 | pF |
| $C_{i(RC)}$ | Input capacitance, strobe inputs | | 7 | | 7 | | 8 | | 8 | pF |
| $C_{i(W)}$ | Input capacitance, write-enable input | | 7 | | 7 | | 7 | | 7 | pF |
| $C_o$ | Output capacitance | | 7 | | 9 | | 10 | | 8 | pF |

NOTE 3: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

| PARAMETER | | ALT. SYMBOL | '4C1024-80 | | '4C1024-10 | | '4C1024-12 | | '4C1024-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{a(C)}$ | Access time from $\overline{CAS}$ low | $t_{CAC}$ | | 20 | | 25 | | 30 | | 40 | ns |
| $t_{a(CA)}$ | Access time from column address | $t_{AA}$ | | 40 | | 45 | | 55 | | 70 | ns |
| $t_{a(R)}$ | Access time from $\overline{RAS}$ low | $t_{RAC}$ | | 80 | | 100 | | 120 | | 150 | ns |
| $t_{a(CP)}$ | Access time from column precharge | $t_{CPA}$ | | 40 | | 40 | | 60 | | 75 | ns |
| $t_{dis(CH)}$ | Output disable time after $\overline{CAS}$ high (see Note 4) | $t_{OFF}$ | | 20 | | 25 | | 30 | | 35 | ns |

NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven. The output is disabled by bringing $\overline{CAS}$ high.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

| | | ALT. SYMBOL | '4C1024-80 | | '4C1024-10 | | '4C1024-12 | | '4C1024-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{c(rd)}$ | Cycle time, read (see Note 6) | $t_{RC}$ | 150 | | 190 | | 220 | | 260 | | ns |
| $t_{c(W)}$ | Cycle time, write | $t_{WC}$ | 150 | | 190 | | 220 | | 260 | | ns |
| $t_{c(rdW)}$ | Cycle time, read-write/read-modify-write | $t_{RWC}$ | 175 | | 220 | | 265 | | 315 | | ns |
| $t_{c(P)}$ | Cycle time, page-mode read or write (see Note 7) | $t_{PC}$ | 50 | | 55 | | 65 | | 80 | | ns |
| $t_{c(PM)}$ | Cycle time, page-mode read-modify-write | $t_{PRWC}$ | 75 | | 85 | | 110 | | 135 | | ns |
| $t_{w(CH)}$ | Pulse duration, $\overline{CAS}$ high | $t_{CP}$ | 10 | | 10 | | 15 | | 25 | | ns |
| $t_{w(CL)}$ | Pulse duration, $\overline{CAS}$ low (see Note 8) | $t_{CAS}$ | 20 | 10000 | 25 | 10000 | 30 | 10000 | 40 | 10000 | ns |
| $t_{w(RH)}$ | Pulse duration, $\overline{RAS}$ high (precharge) | $t_{RP}$ | 60 | | 80 | | 90 | | 100 | | ns |
| $t_{w(RL)}$ | Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 9) | $t_{RAS}$ | 80 | 10000 | 100 | 10000 | 120 | 10000 | 150 | 10000 | ns |
| $t_{w(RL)P}$ | Pulse duration, page mode, $\overline{RAS}$ low (see Note 9) | $t_{RASP}$ | 80 | 100000 | 100 | 100000 | 120 | 100000 | 150 | 100000 | ns |
| $t_{w(WL)}$ | Pulse duration, write | $t_{WP}$ | 15 | | 15 | | 20 | | 25 | | ns |
| $t_{su(CA)}$ | Setup time, column address before $\overline{CAS}$ low | $t_{ASC}$ | 0 | | 3 | | 3 | | 3 | | ns |
| $t_{su(RA)}$ | Setup time, row address before $\overline{RAS}$ low | $t_{ASR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{su(D)}$ | Setup time, data (see Note 10) | $t_{DS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{su(rd)}$ | Setup time, read before $\overline{CAS}$ low | $t_{RCS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{su(WCL)}$ | Setup time, $\overline{W}$ low before $\overline{CAS}$ low (see Note 11) | $t_{WCS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{su(WCH)}$ | Setup time, $\overline{W}$ low before $\overline{CAS}$ high | $t_{CWL}$ | 20 | | 25 | | 30 | | 40 | | ns |
| $t_{su(WRH)}$ | Setup time, $\overline{W}$ low before $\overline{RAS}$ high | $t_{RWL}$ | 20 | | 25 | | 30 | | 40 | | ns |
| $t_{h(CA)}$ | Hold time, column address after $\overline{CAS}$ low | $t_{CAH}$ | 15 | | 20 | | 20 | | 25 | | ns |
| $t_{h(RA)}$ | Hold time, row address after $\overline{RAS}$ low | $t_{RAH}$ | 12 | | 15 | | 15 | | 20 | | ns |

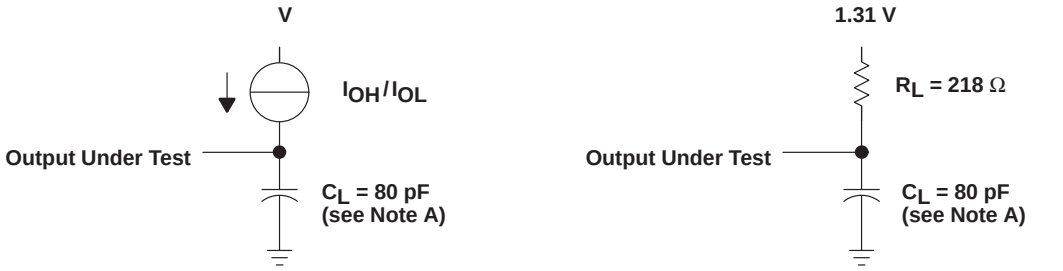
NOTES: 5. Timing measurements in this table are referenced to $V_{IL}$ max and $V_{IH}$ min.
6. All cycle times assume $t_t$ = 5 ns.
7. To assure $t_{c(P)}$ min, $t_{su(CA)}$ should be ≥ $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Early write operation only

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5) (continued)**

| | | ALT. SYMBOL | '4C1024-80 | | '4C1024-10 | | '4C1024-12 | | '4C1024-15 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{h(RLCA)}$ | Hold time, column address after $\overline{RAS}$ low (see Note 12) | $t_{AR}$ | 60 | | 70 | | 80 | | 100 | | ns |
| $t_{h(D)}$ | Hold time, data (see Note 10) | $t_{DH}$ | 15 | | 20 | | 25 | | 30 | | ns |
| $t_{h(RLD)}$ | Hold time, data after $\overline{RAS}$ low (see Note 12) | $t_{DHR}$ | 60 | | 70 | | 85 | | 110 | | ns |
| $t_{h(CHrd)}$ | Hold time, read after $\overline{CAS}$ high (see Note 13) | $t_{RCH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{h(RHrd)}$ | Hold time, read after $\overline{RAS}$ high (see Note 13) | $t_{RRH}$ | 10 | | 10 | | 10 | | 10 | | ns |
| $t_{h(CLW)}$ | Hold time, write after $\overline{CAS}$ low (see Note 11) | $t_{WCH}$ | 15 | | 20 | | 25 | | 30 | | ns |
| $t_{h(RLW)}$ | Hold time, write after $\overline{RAS}$ low (see Note 12) | $t_{WCR}$ | 60 | | 70 | | 85 | | 100 | | ns |
| $t_{d(RLCH)}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high | $t_{CSH}$ | 80 | | 100 | | 120 | | 150 | | ns |
| $t_{d(CHRL)}$ | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | $t_{CRP}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{d(CLRH)}$ | Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high | $t_{RSH}$ | 20 | | 25 | | 30 | | 40 | | ns |
| $t_{d(CLWL)}$ | Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14) | $t_{CWD}$ | 20 | | 25 | | 40 | | 50 | | ns |
| $t_{d(RLCL)}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15) | $t_{RCD}$ | 22 | 60 | 28 | 75 | 28 | 90 | 33 | 110 | ns |
| $t_{d(RLCA)}$ | Delay time, $\overline{RAS}$ low to column address (see Note 15) | $t_{RAD}$ | 17 | 40 | 20 | 55 | 20 | 65 | 25 | 80 | ns |
| $t_{d(CARH)}$ | Delay time, column address to $\overline{RAS}$ high | $t_{RAL}$ | 40 | | 45 | | 55 | | 70 | | ns |
| $t_{d(CACH)}$ | Delay time, column address to $\overline{CAS}$ high | $t_{CAL}$ | 40 | | 45 | | 55 | | 70 | | ns |
| $t_{d(RLWL)}$ | Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14) | $t_{RWD}$ | 80 | | 100 | | 130 | | 160 | | ns |
| $t_{d(CAWL)}$ | Delay time, column address to $\overline{W}$ low (see Note 14) | $t_{AWD}$ | 40 | | 45 | | 65 | | 80 | | ns |
| $t_{d(RLCH)R}$ | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16) | $t_{CHR}$ | 20 | | 25 | | 25 | | 30 | | ns |
| $t_{d(CLRL)R}$ | Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16) | $t_{CSR}$ | 10 | | 10 | | 10 | | 15 | | ns |
| $t_{d(RHCL)R}$ | Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low | $t_{RPC}$ | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{rf}$ | Refresh time interval | $t_{REF}$ | | 8 | | 8 | | 8 | | 8 | ms |
| $t_t$ | Transition time (see Note 17) | — | — | | — | | — | | — | | ns |

NOTES: 5. Timing measurements in this table are referenced to $V_{IL}$ max and $V_{IH}$ min.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early-write operation only
12. The minimum value is measured when $t_{d(RLCL)}$ is set $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Read-modify-write operation only
15. Maximum value specified only to assure access time.
16. CBR refresh only
17. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and a maximum of 50 ns.

## PARAMETER MEASUREMENT INFORMATION

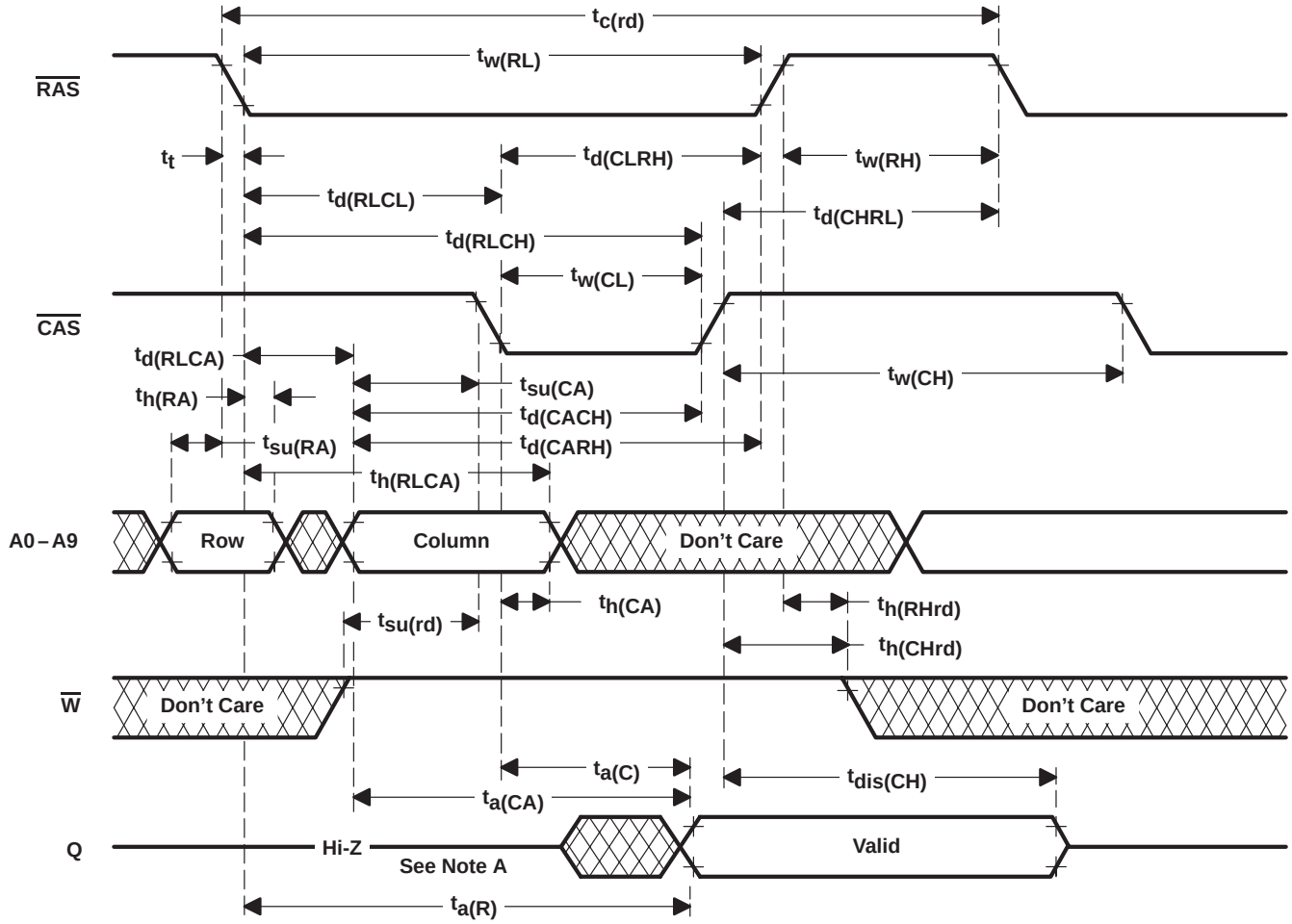



**(a) LOAD CIRCUIT** **(b) ALTERNATE LOAD CIRCUIT**

NOTE A: $C_L$ includes probe and fixture capacitance.

**Figure 1. Load Circuits for Timing Parameters**

## PARAMETER MEASUREMENT INFORMATION




NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

**Figure 2. Read-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

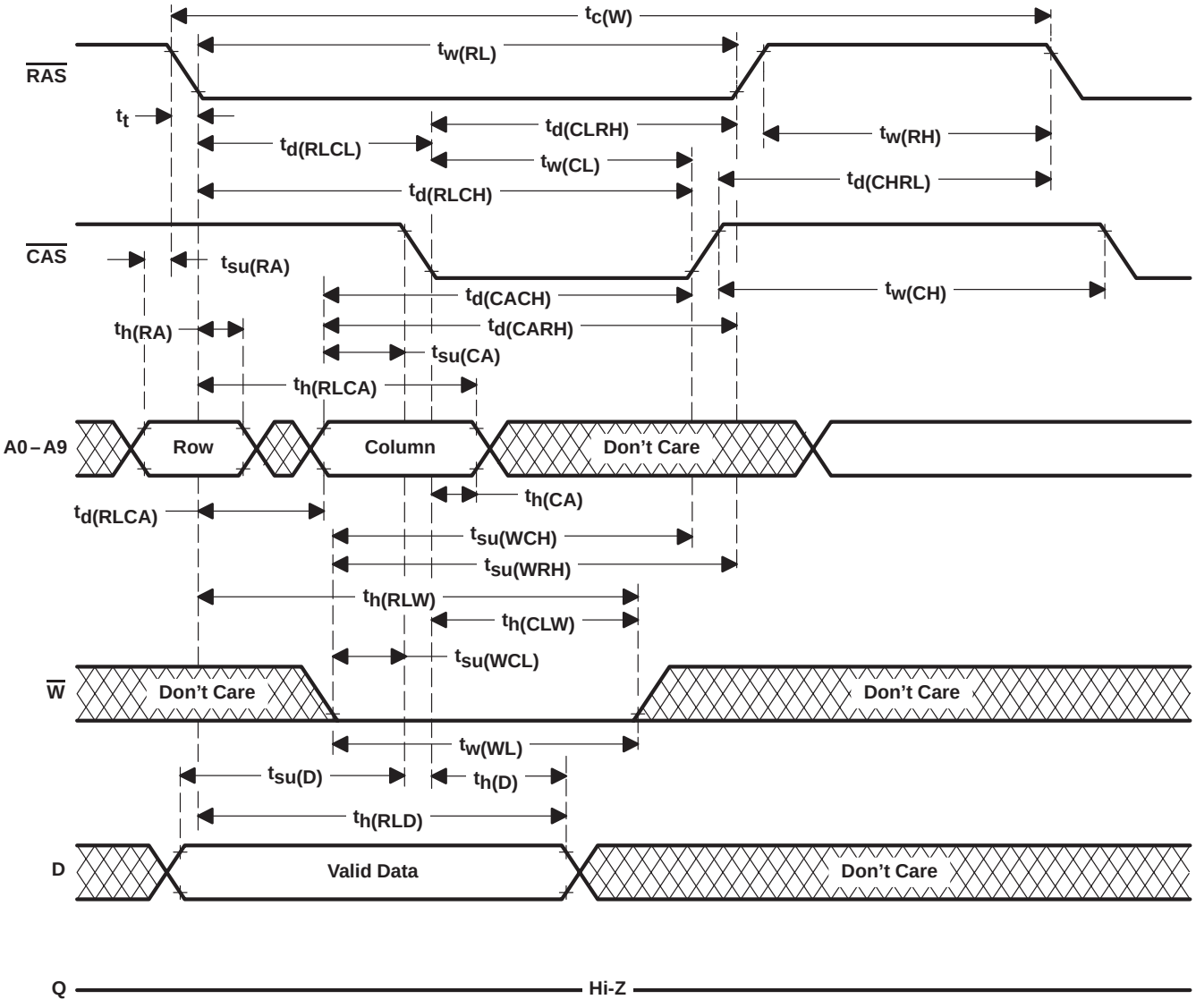



**Figure 3. Early-Write-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

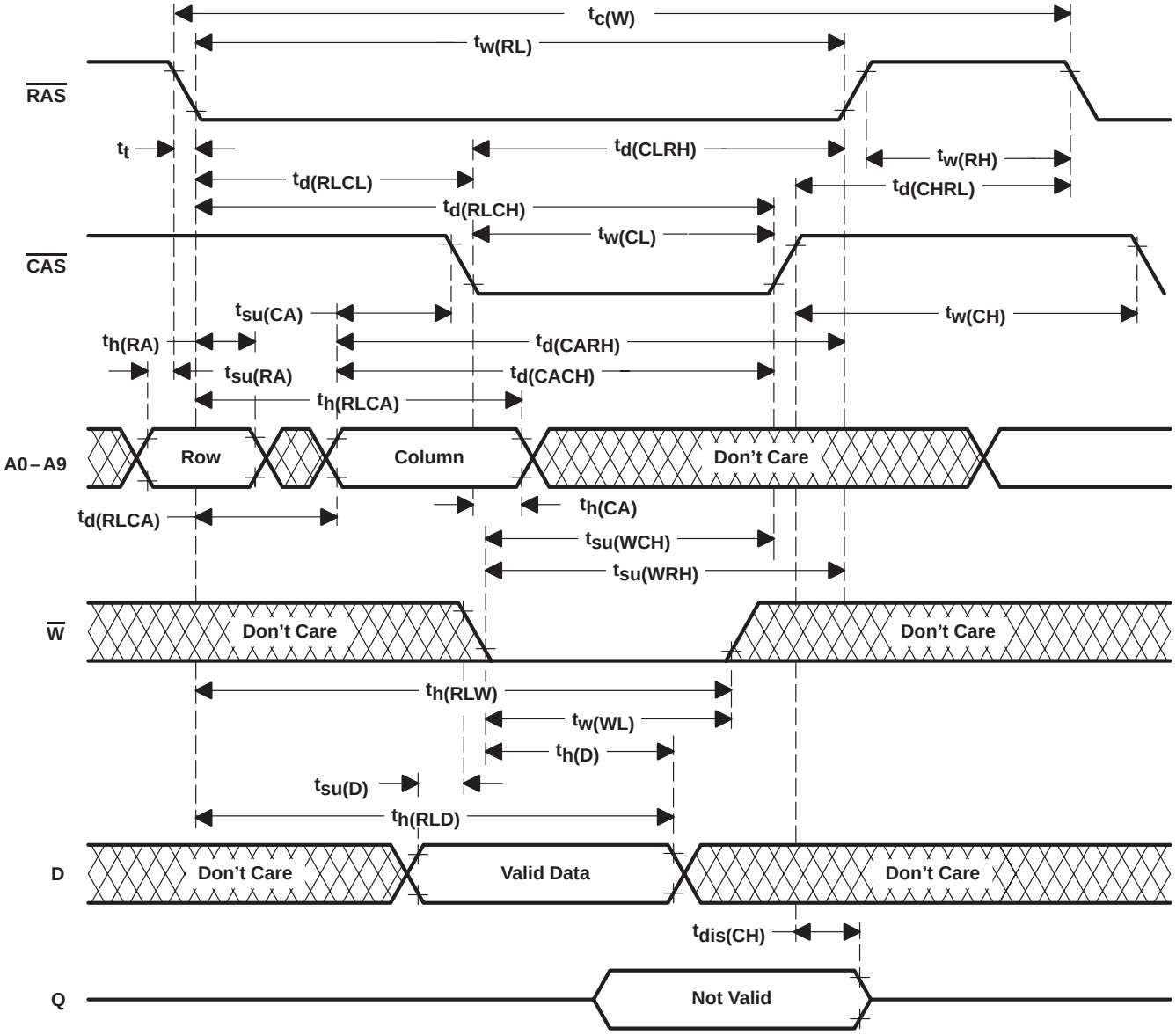
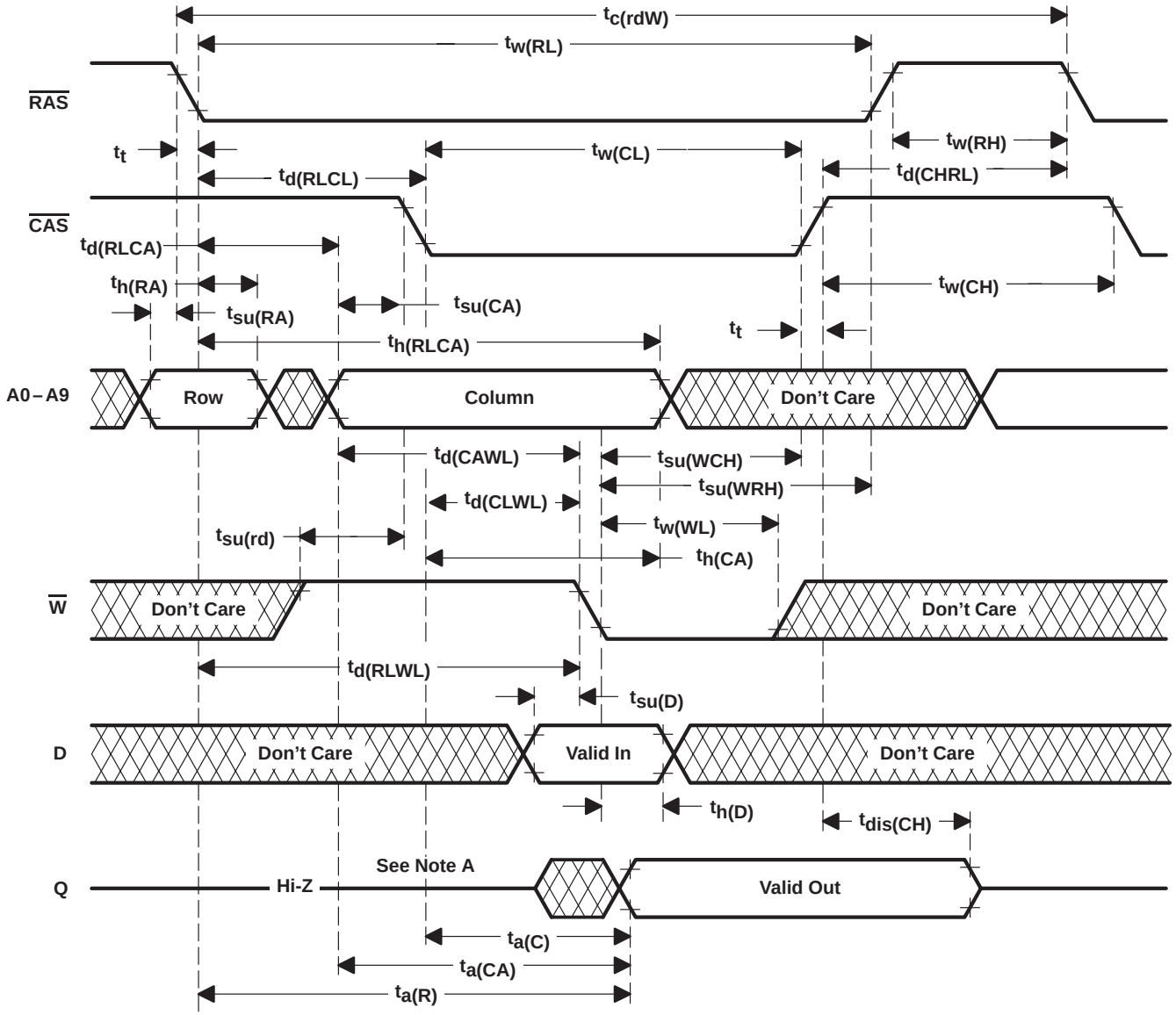



**Figure 4. Write-Cycle Timing**

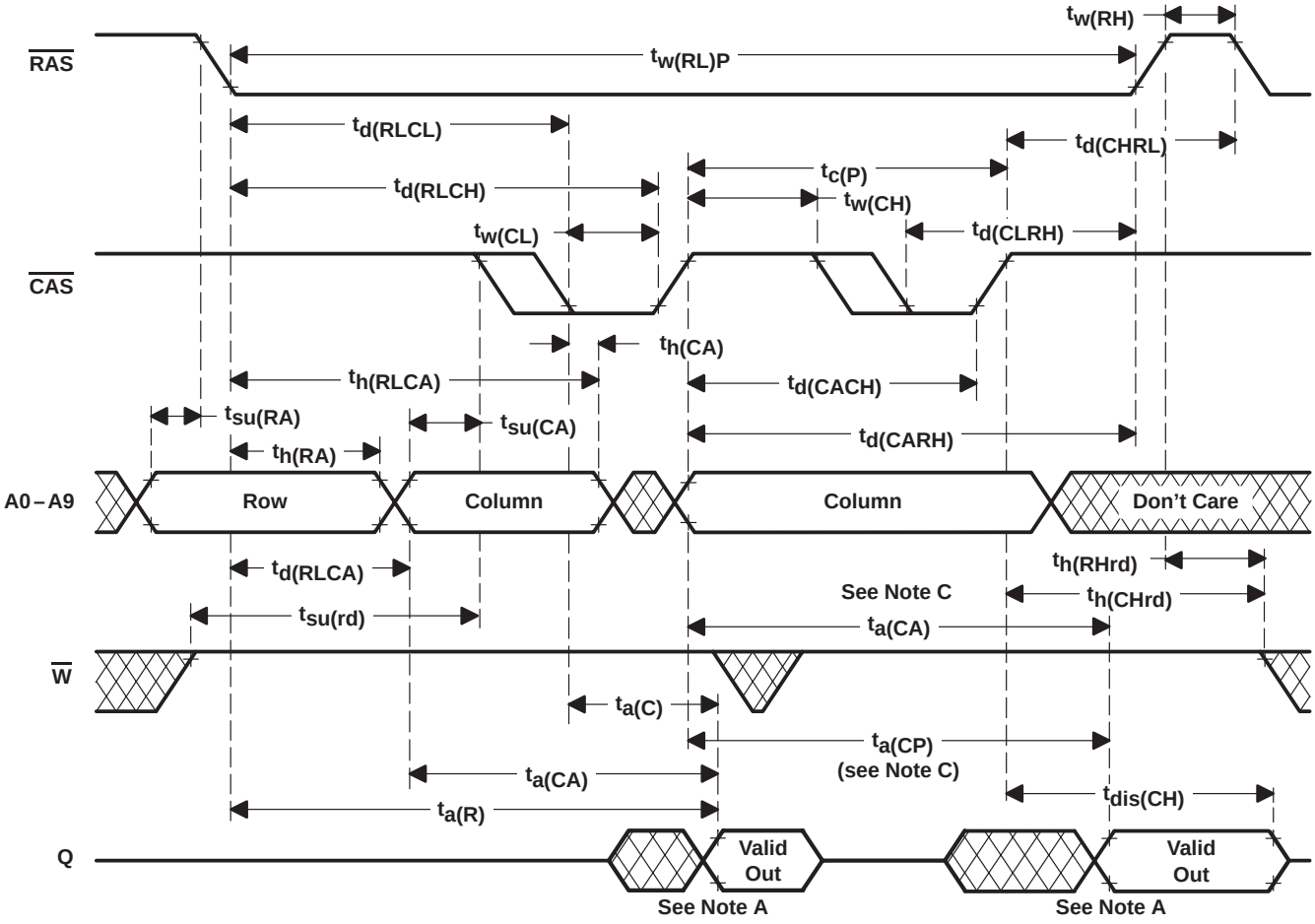
## PARAMETER MEASUREMENT INFORMATION




NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

**Figure 5. Read-Write-/Read-Modify-Write-Cycle Timing**

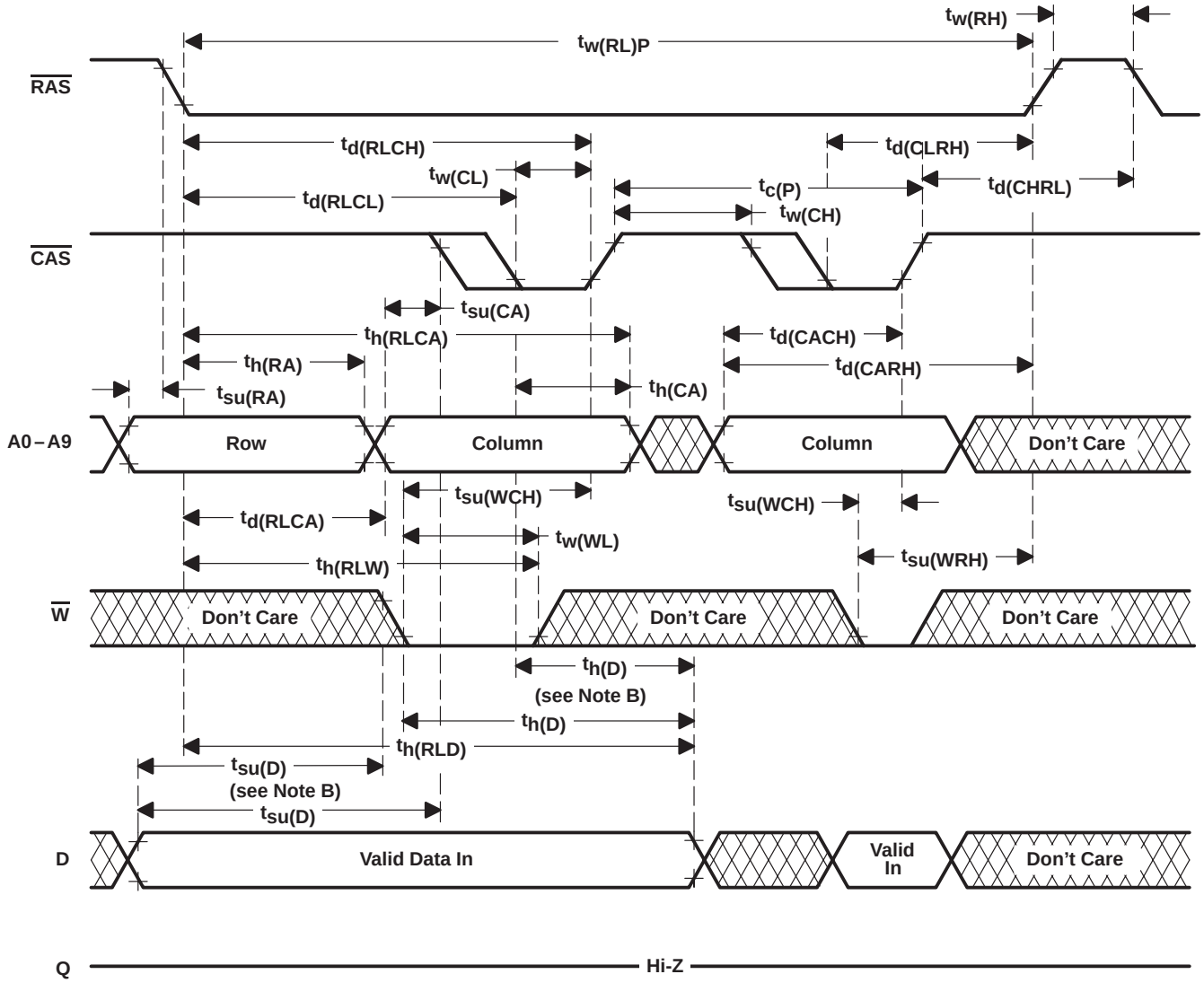
## PARAMETER MEASUREMENT INFORMATION




NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A write cycle or a read-modify cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

**Figure 6. Enhanced-Page-Mode Read-Cycle Timing**

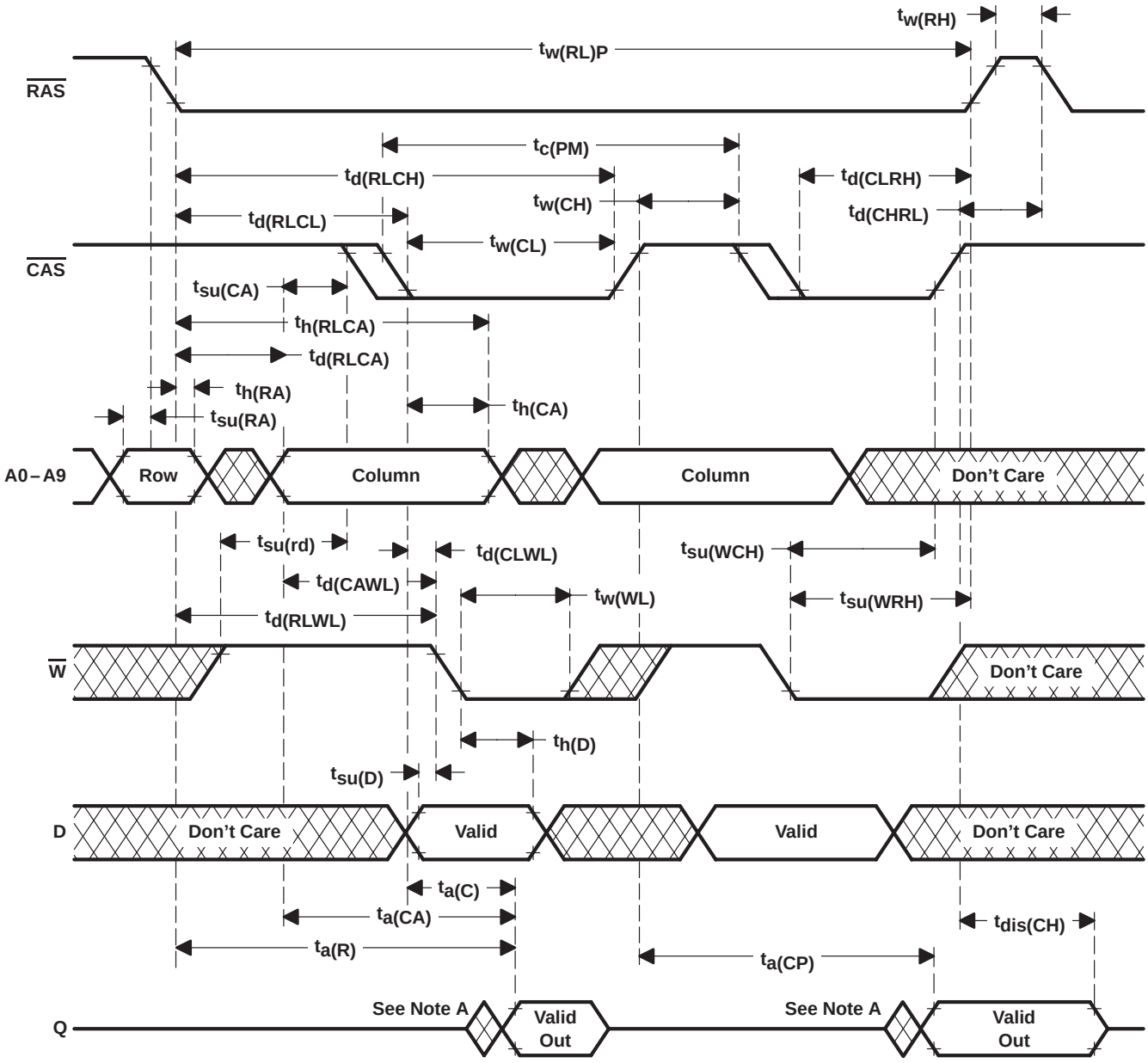
## PARAMETER MEASUREMENT INFORMATION




NOTES: A. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.
B. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

**Figure 7. Enhanced-Page-Mode Write-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. Output can go from high-impedance state to an invalid-data state prior to the specified access time.
B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

**Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

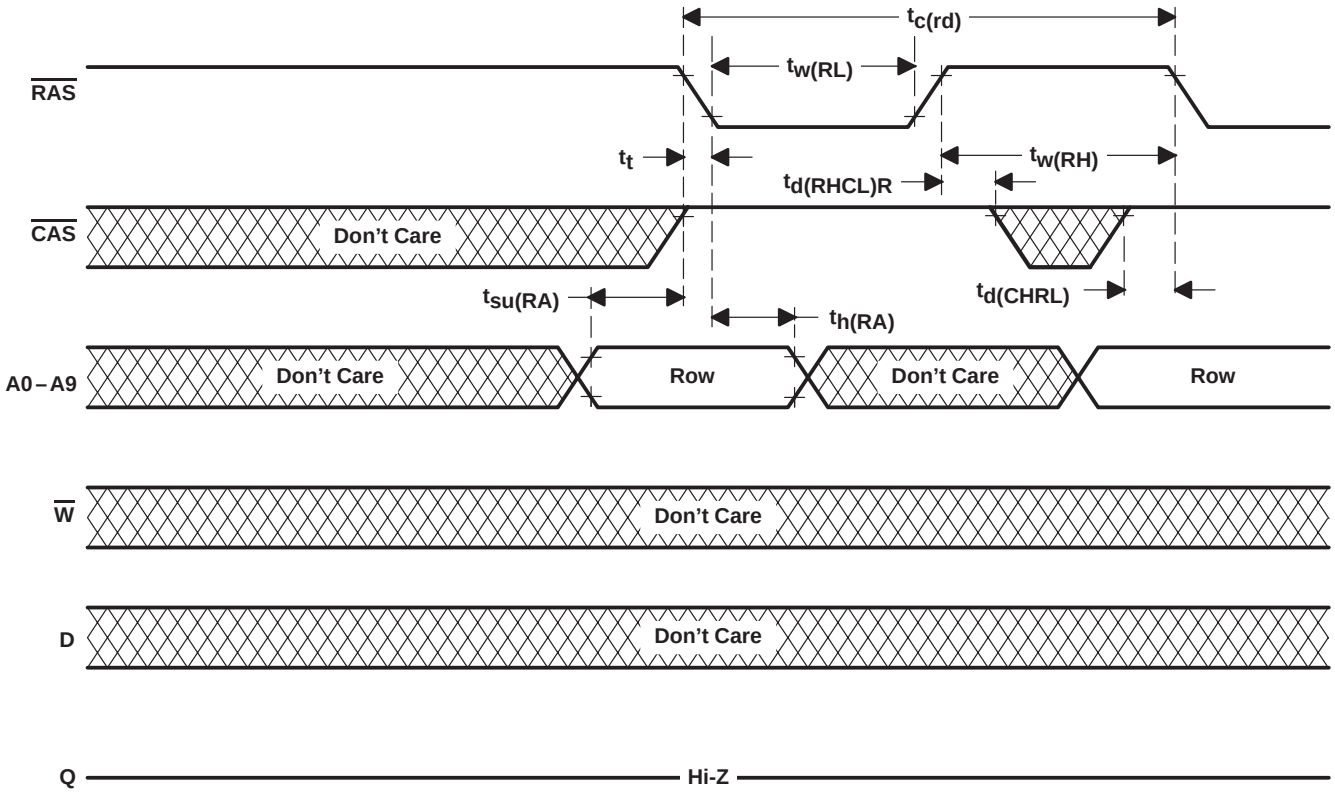



**Figure 9. $\overline{RAS}$-Only Refresh-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

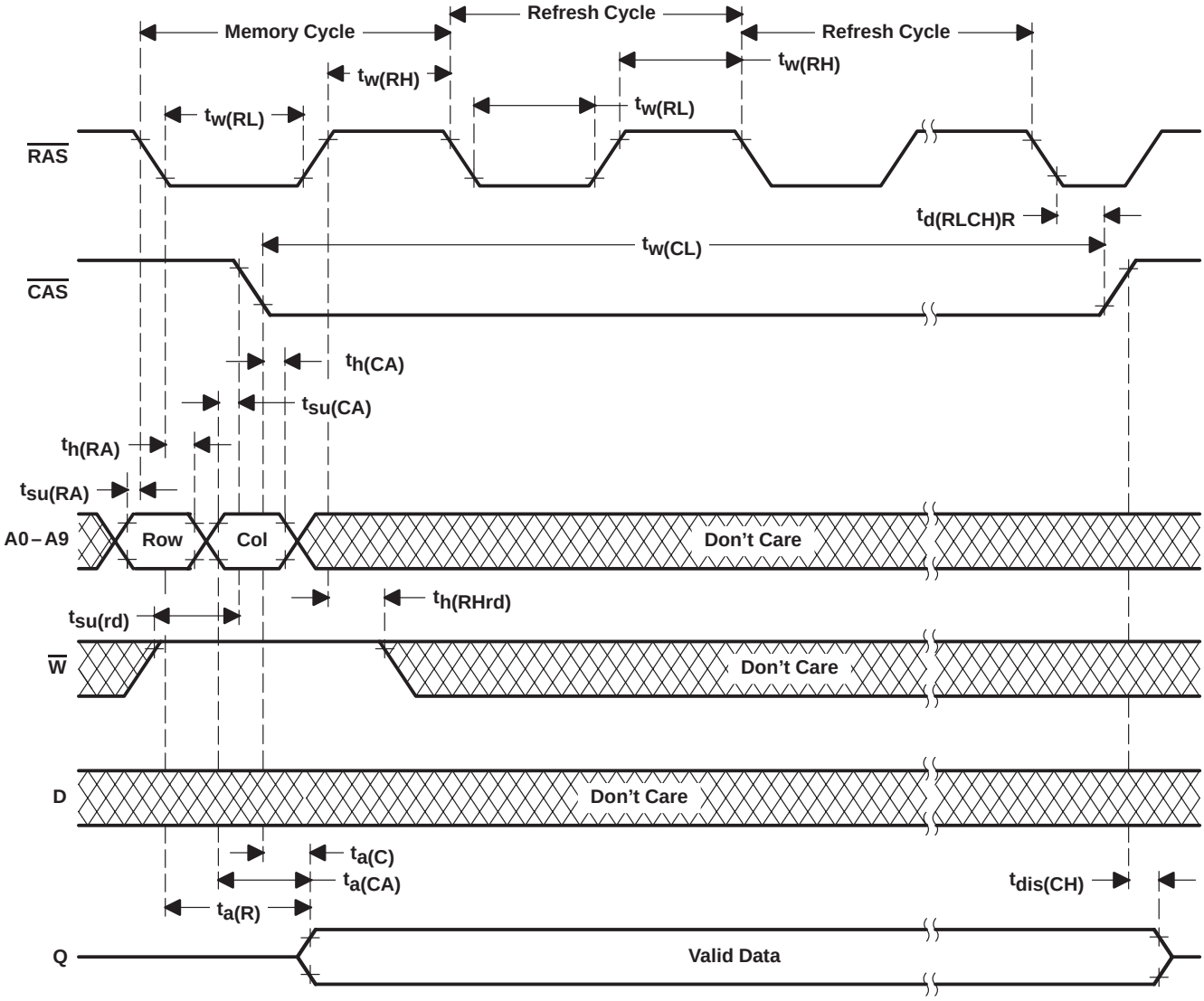



**Figure 10. Hidden-Refresh-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

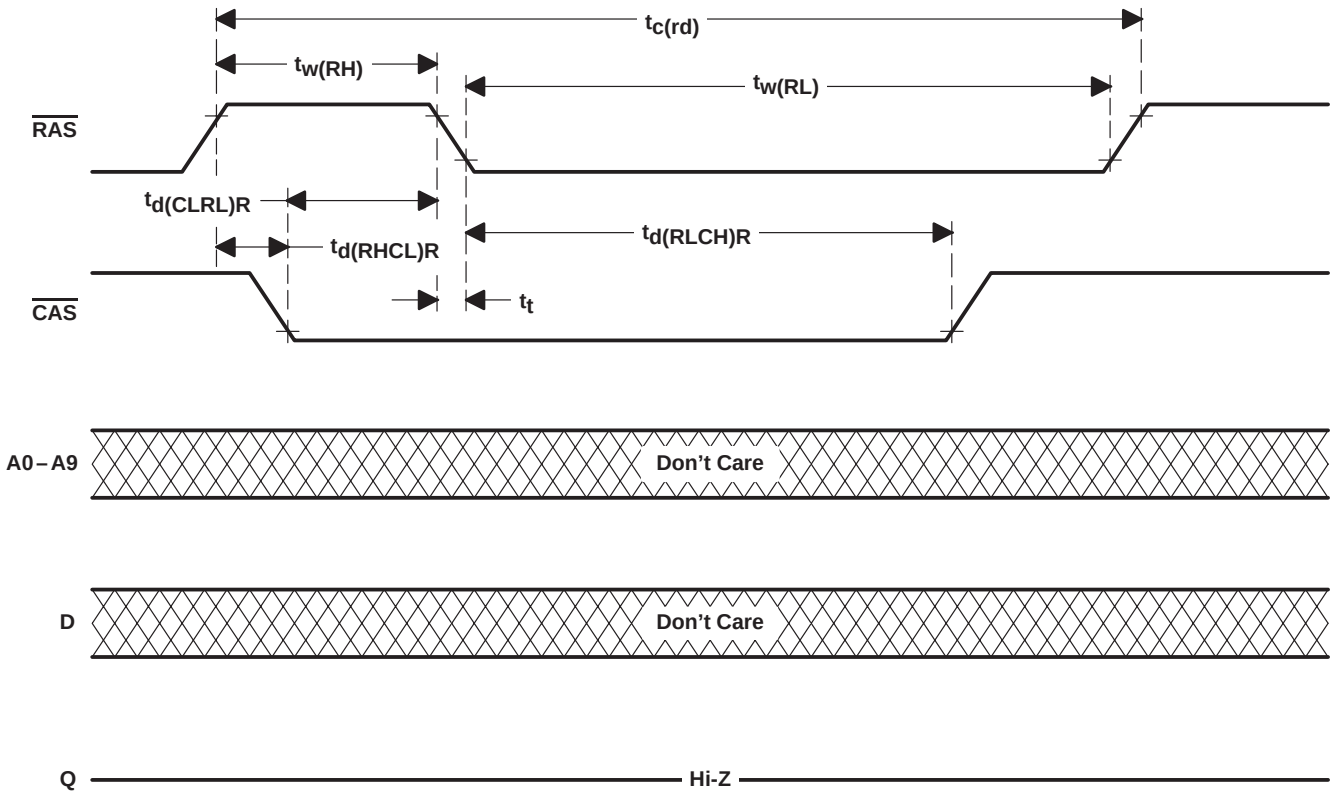
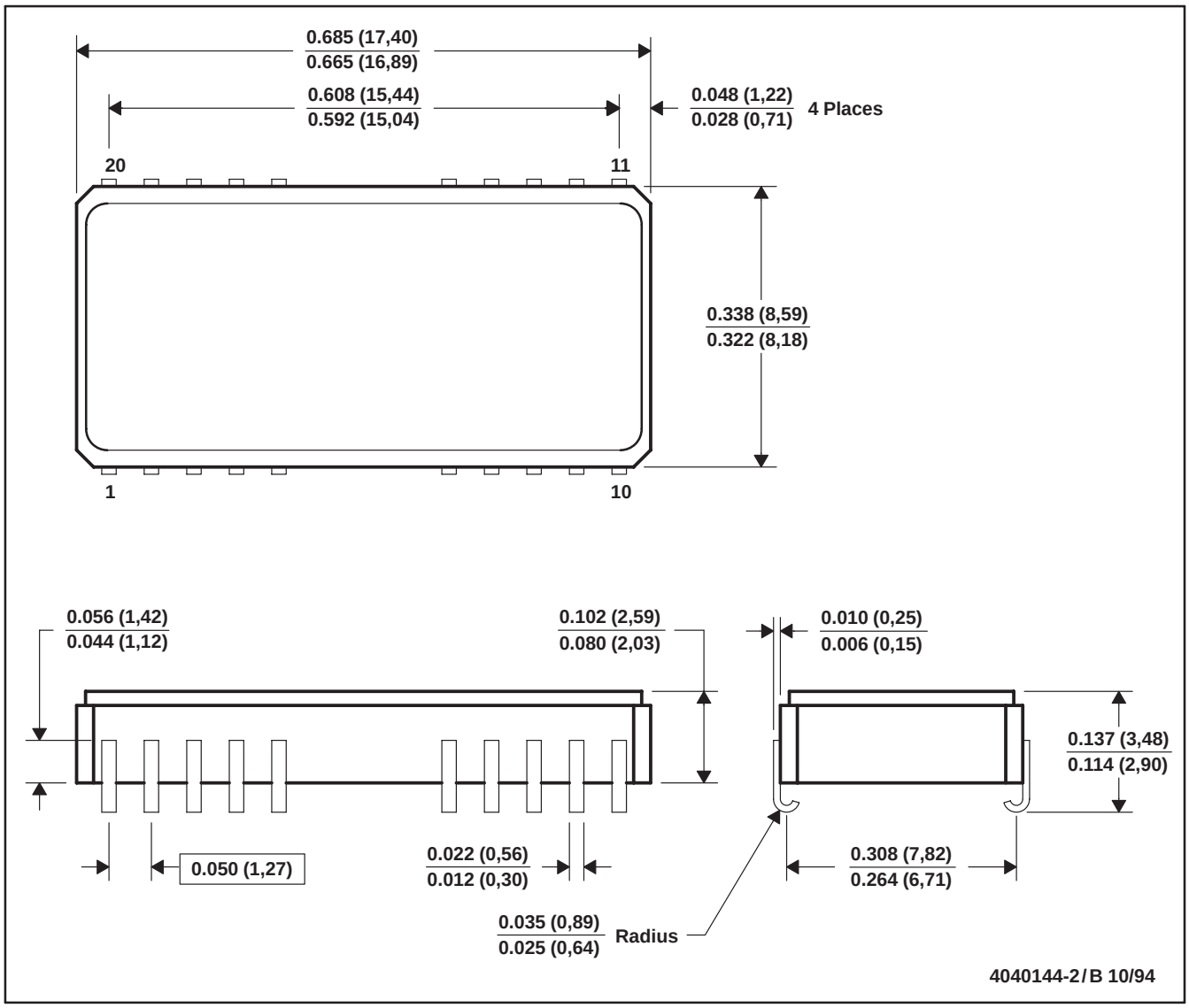



**Figure 11. Automatic-CBR-Refresh-Cycle Timing**

## MECHANICAL DATA

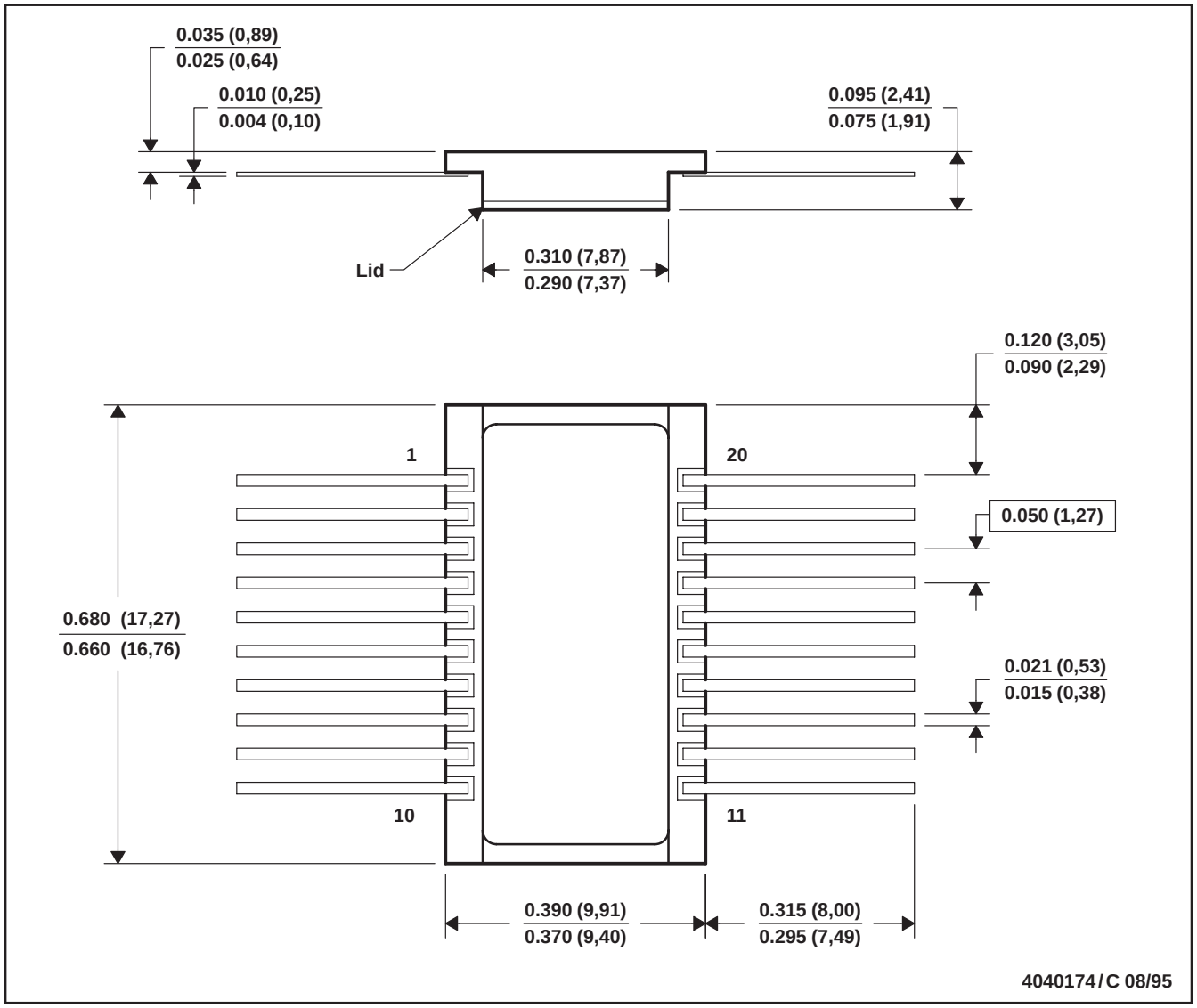
**HJ (R-CDCC-J20)** **J-LEADED CERAMIC CHIP CARRIER**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

## MECHANICAL DATA

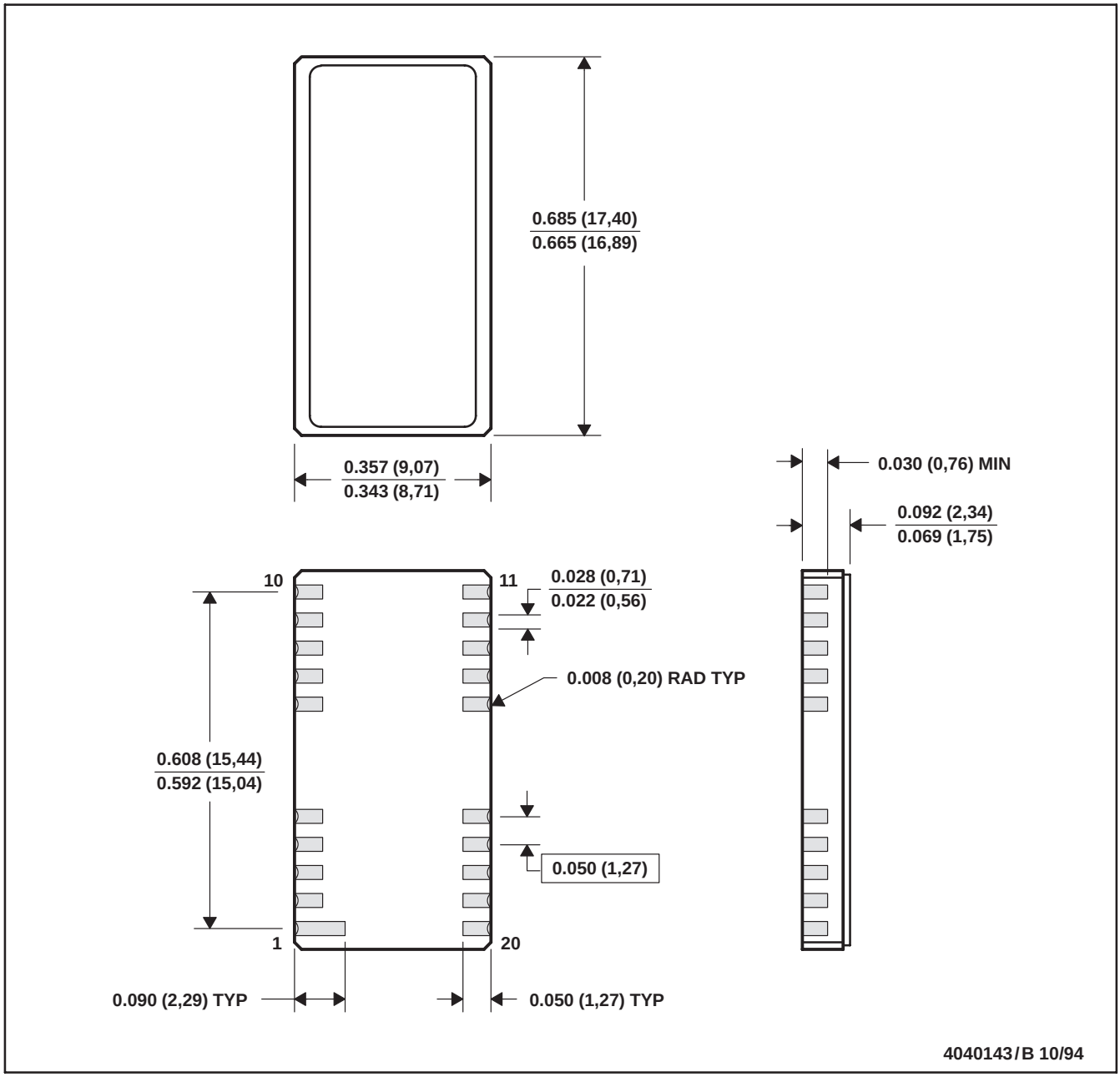
**HK (R-CDFP-F20)** **CERAMIC DUAL FLATPACK**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

## MECHANICAL DATA

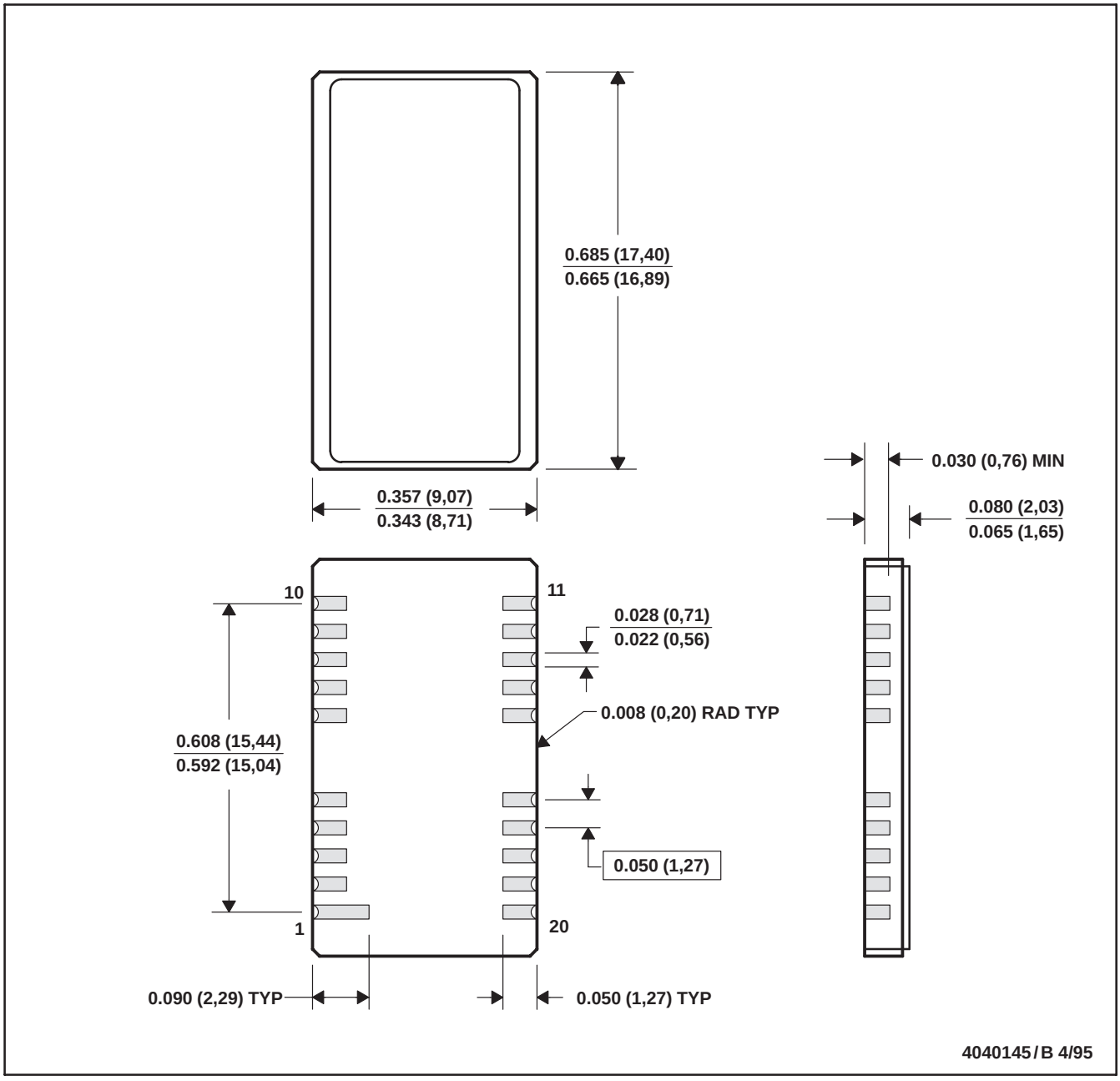
**FQ (R-CDCC-N20)** **LEADLESS CERAMIC CHIP CARRIER**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

## MECHANICAL DATA

**HL (R-CDCC-N20/26)** **LEADLESS CERAMIC CHIP CARRIER**

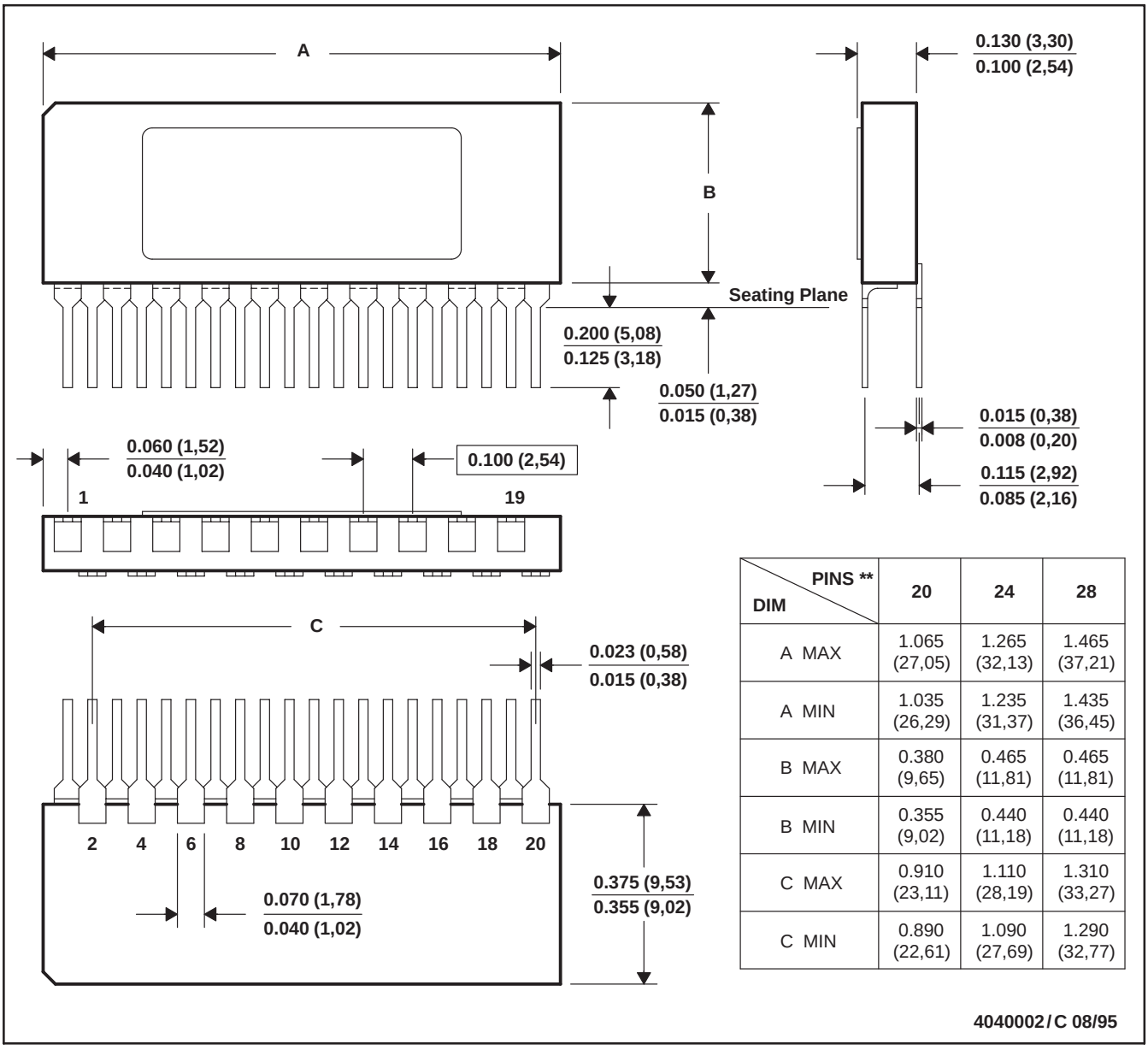



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

## MECHANICAL DATA

**SV (R-CZIP-T**)** **CERAMIC ZIG-ZAG PACKAGE**

**20 PIN SHOWN**




| DIM \ PINS ** | 20 | 24 | 28 |
|---|---|---|---|
| A MAX | 1.065 (27,05) | 1.265 (32,13) | 1.465 (37,21) |
| A MIN | 1.035 (26,29) | 1.235 (31,37) | 1.435 (36,45) |
| B MAX | 0.380 (9,65) | 0.465 (11,81) | 0.465 (11,81) |
| B MIN | 0.355 (9,02) | 0.440 (11,18) | 0.440 (11,18) |
| C MAX | 0.910 (23,11) | 1.110 (28,19) | 1.310 (33,27) |
| C MIN | 0.890 (22,61) | 1.090 (27,69) | 1.290 (32,77) |

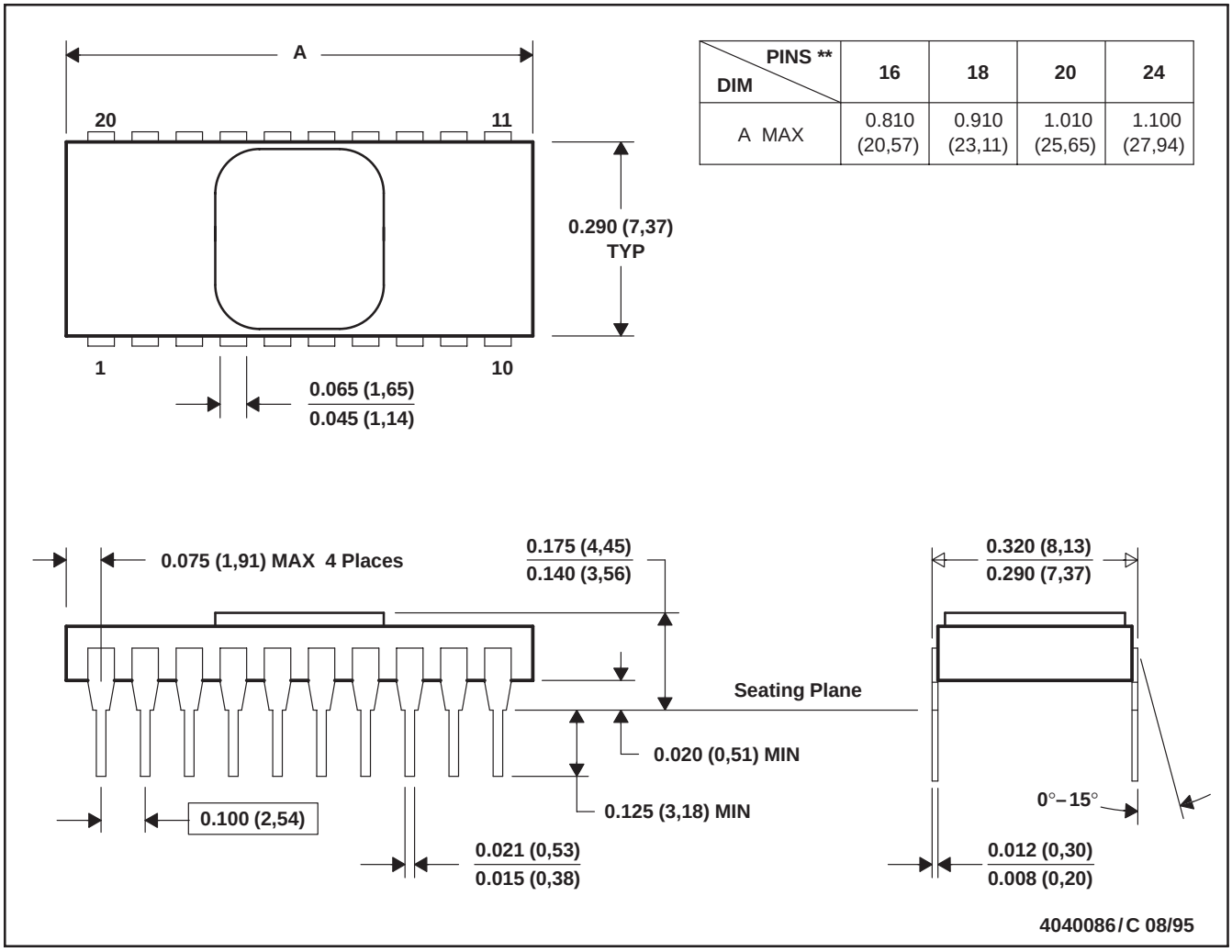
**4040002 / C 08/95**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

## MECHANICAL DATA

**JD (R-CDIP-T**)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE**

**20 PIN SHOWN**




| DIM \ PINS ** | 16 | 18 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 0.810 (20,57) | 0.910 (23,11) | 1.010 (25,65) | 1.100 (27,94) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

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