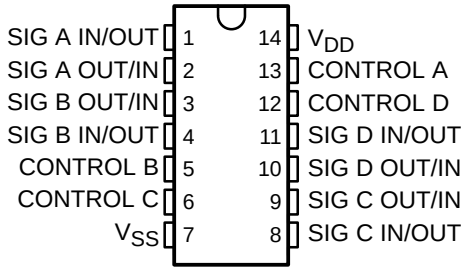
- **15-V Digital or ±7.5-V Peak-to-Peak Switching**
- **125-Ω Typical On-State Resistance for 15-V Operation**
- **Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range**
- **On-State Resistance Flat Over Full Peak-to-Peak Signal Range**
- **High On/Off Output-Voltage Ratio: 80 dB Typical at f_{is} = 10 kHz, R_L = 1 kΩ**
- **High Degree of Linearity: <0.5% Distortion Typical at f_{is} = 1 kHz, V_{is} = 5 V p-p, $V_{DD} - V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical**
- **Low Crosstalk Between Switches: –50 dB Typical at f_{is} = 8 MHz, R_L = 1 kΩ**
- **Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients**
- **Frequency Response, Switch On = 40 MHz Typical**
- **100% Tested for Quiescent Current at 20 V**
- **5-V, 10-V, and 15-V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, Standard Specifications for Description of B-Series CMOS Devices**
- **Applications:**
  - **Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch**
  - **Digital Signal Switching/Multiplexing**
  - **Transmission-Gate Logic Implementation**
  - **Analog-to-Digital and Digital-to-Analog Conversion**
  - **Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain**

E, F, M, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – F	Tube	CD4066BF3A	CD4066BF3A
	PDIP – E	Tube	CD4066BE	CD4066BE
	SOIC – M	Tube	CD4066BM	CD4066BM
		Tape and reel	CD4066BM96	
	SOP – NS	Tape and reel	CD4066BNSR	CD4066B
	TSSOP – PW	Tube	CD4066BPW	CM066B
		Tape and reel	CD4066BPWR	

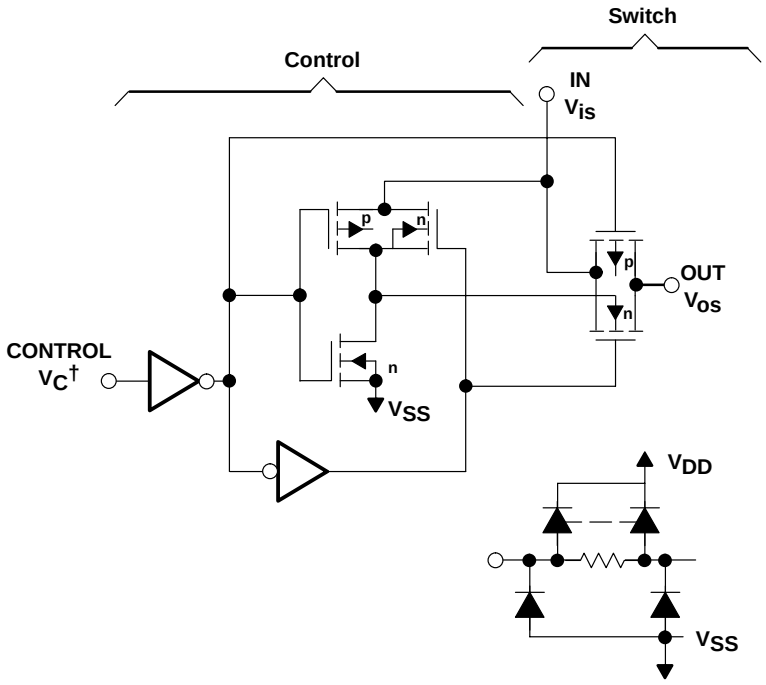
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input, when the switch is on, or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.



† All control inputs are protected by CMOS protection network.

NOTES: A. All p substrates are connected to V_{DD}.
B. Normal operation control-line biasing: Switch on (logic 1), $V_C = V_{DD}$; Switch off (logic 0), $V_C = V_{SS}$
C. Signal-level range: $VSS \le V_{is} \le V_{DD}$

92CS - 29113

Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

DC supply-voltage range, (V_{DD}) (voltages referenced to V_{SS} terminal) . . . . . –0.5 V to 20 V
Input voltage range, V_{IS}, all inputs . . . . . –0.5 V to V_{DD} + 0.5 V
DC input current, I_{IN}, any one input . . . . . ±10 mA
Package thermal impedance, θ_{JA} (see Note 1): E package . . . . . 80°C/W
M package . . . . . 86°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 265°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating free-air temperature	–55	125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES						UNIT
					–55°C	–40°C	85°C	125°C	25°C		
									TYP	MAX	
I_{DD}	Quiescent device current		0, 5	5	0.25	0.25	7.5	7.5	0.01	0.25	µA
			0, 10	10	0.5	0.5	15	15	0.01	0.5	
			0, 15	15	1	1	30	30	0.01	1	
			0, 20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Output (V_{OS})											
r_{on}	On-state resistance (max)	$V_C = V_{DD}$ R_L = 10 kΩ returned to $\frac{V_{DD} - V_{SS}}{2}$ $V_{is} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
				10	310	330	500	550	180	400	
				15	200	210	300	320	125	240	
Δr_{on}	On-state resistance difference between any two switches	R_L = 10 kΩ, $V_C = V_{DD}$		5					15		Ω
				10					10		
				15					5		
THD	Total harmonic distortion	$V_C = V_{DD}$ = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 10 kΩ, f_{is} = 1-kHz sine wave							0.4		%
	–3-dB cutoff frequency (switch on)	$V_C = V_{DD}$ = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ							40		MHz
	–50-dB feed-through frequency (switch off)	$V_C = V_{SS}$ = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ							1		MHz
I_{is}	Input/output leakage current (switch off) (max)	V_C = 0 V, V_{is} = 18 V, V_{os} = 0 V; and V_C = 0 V, V_{is} = 0 V, V_{os} = 18 V		18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	µA
	–50-dB crosstalk frequency	$V_C(A) = V_{DD}$ = 5 V, $V_C(B) = V_{SS}$ = –5 V, $V_{is}(A)$ = 5 V_{p-p}, 50-Ω source, R_L = 1 kΩ							8		MHz
t_{pd}	Propagation delay (signal input to signal output)	R_L = 200 kΩ, $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF, V_{is} = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns		5					20	40	ns
				10					10	20	
				15					7	15	
C_{is}	Input capacitance	V_{DD} = 5 V $V_C = V_{SS}$ = –5 V							8		pF
C_{os}	Output								8		
C_{ios}	Feed through								0.5		

electrical characteristics (continued)

CHARACTERISTIC		TEST CONDITIONS	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES						UNIT
				–55°C	–40°C	85°C	125°C	25°C TYP	25°C MAX	
Control (V_C)										
V_{ILC}	Control input, low voltage (max)	$\|I_{is}\| < 10\ \mu A$, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$	5	1	1	1	1		1	V
			10	2	2	2	2		2	
			15	2	2	2	2		2	
V_{IHC}	Control input, high voltage	See Figure 6	5	3.5 (MIN)						V
			10	7 (MIN)						
			15	11 (MIN)						
I_{IN}	Input current (MAX)	$V_{is} \le V_{DD}$, $V_{DD} - V_{SS} = 18$ V, $V_{CC} \le V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	μA
	Crosstalk (control input to signal output)	$V_C = 10$ V (square wave), t_r, $t_f = 20$ ns, $R_L = 10\ k\Omega$	10					50		mV
	Turn-on and turn-off propagation delay	$V_{IN} = V_{DD}$, t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 1\ k\Omega$	5					35	70	ns
			10					20	40	
			15					15	30	
	Maximum control input repetition rate	$V_{is} = V_{DD}$, V_{SS} = GND, $R_L = 1\ k\Omega$ to GND, $C_L = 50$ pF, $V_C = 10$ V (square wave centered on 5 V), t_r, $t_f = 20$ ns, $V_{OS} = 1/2\ V_{OS}$ at 1 kHz	5					6		MHz
			10					9		
			15					9.5		
C_I	Input capacitance							5	7.5	pF

switching characteristics

V_{DD} (V)	SWITCH INPUT						SWITCH OUTPUT, V_{OS} (V)	
	V_{is} (V)	I_{is} (mA)						
		–55°C	–40°C	25°C	85°C	125°C	MIN	MAX
5	0	0.64	0.61	0.51	0.42	0.36		0.4
5	5	–0.64	–0.61	–0.51	–0.42	–0.36	4.6	
10	0	1.6	1.5	1.3	1.1	0.9		0.5
10	10	–1.6	–1.5	–1.3	–1.1	–0.9	9.5	
15	0	4.2	4	3.4	2.8	2.4		1.5
15	15	–4.2	–4	–3.4	–2.8	–2.4	13.5	

TYPICAL CHARACTERISTICS

TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

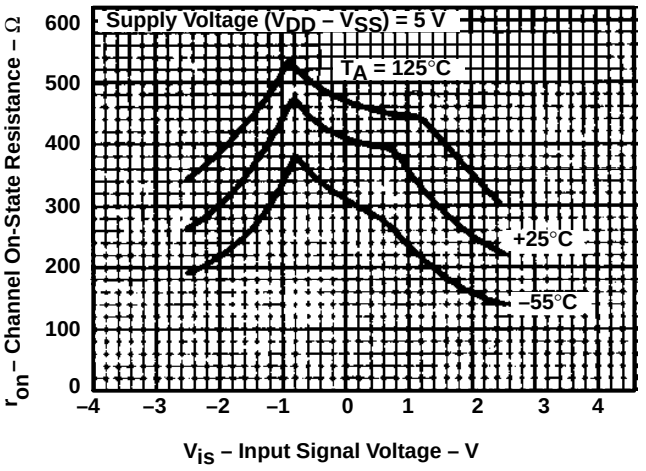


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Figure 2

TYPICAL ON-STATE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

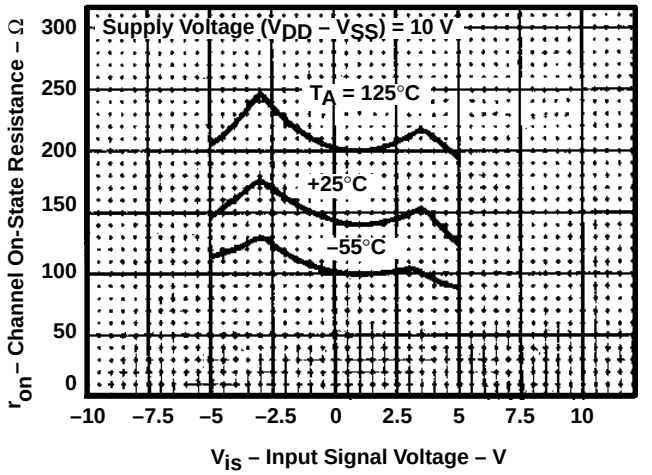

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Figure 3

TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

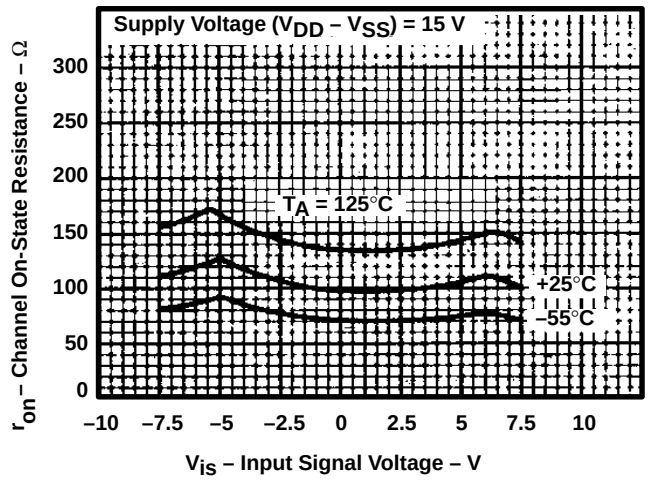

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Figure 4

ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

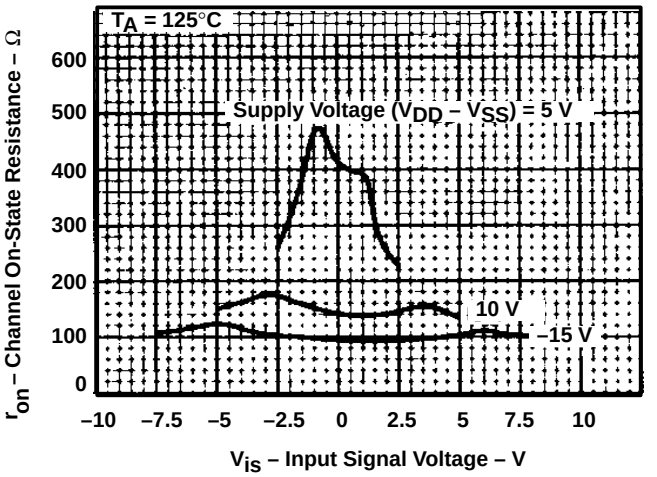

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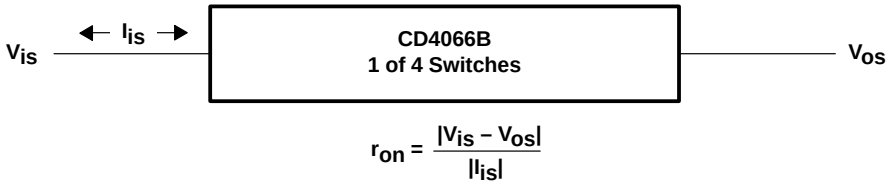
Figure 5

TYPICAL CHARACTERISTICS



92CS - 30966

Figure 6. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification

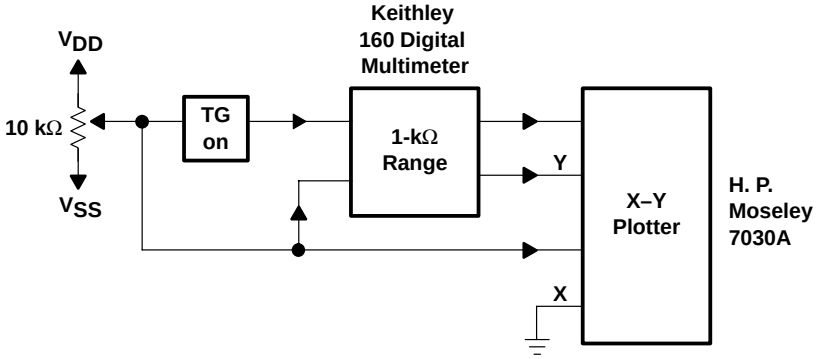


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Figure 7. Channel On-State Resistance Measurement Circuit

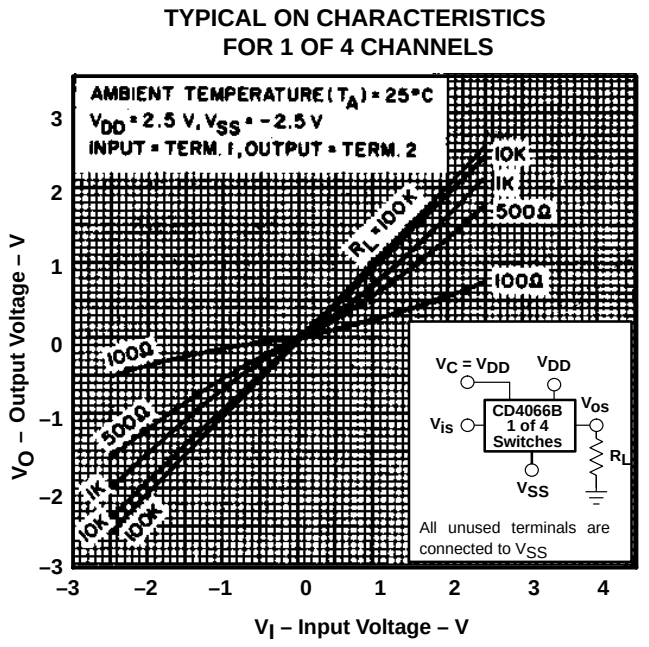

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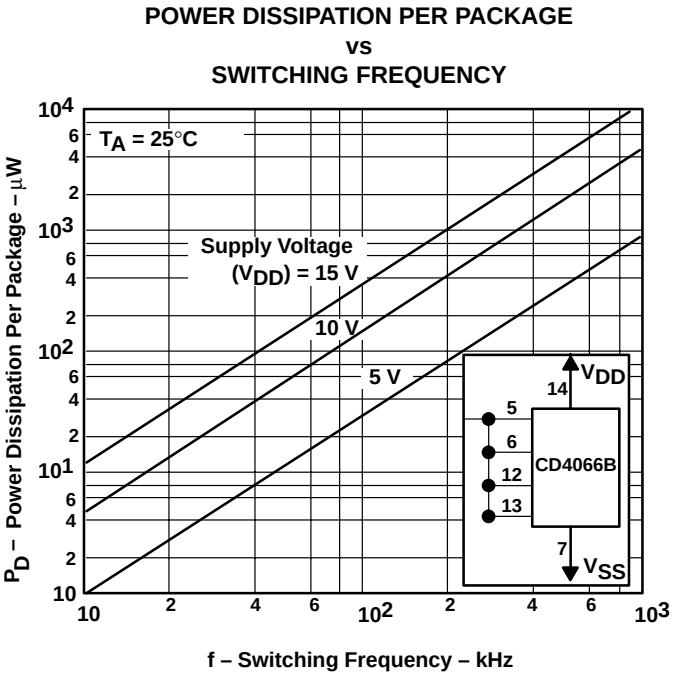
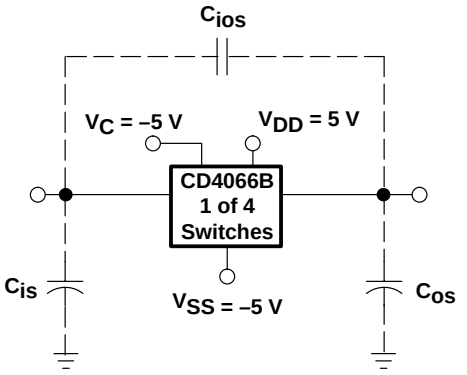
Figure 8



92CS -30920

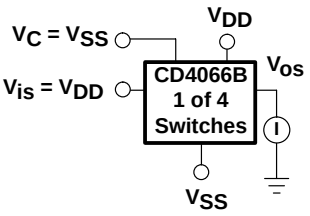
Figure 9

TYPICAL CHARACTERISTICS



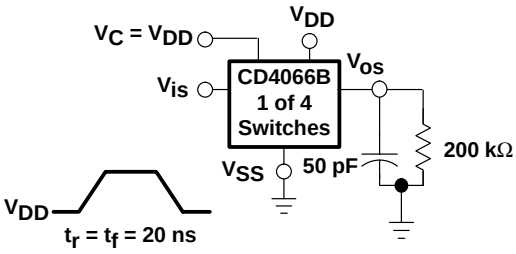
Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

Figure 10. Typical On Characteristics for One of Four Channels



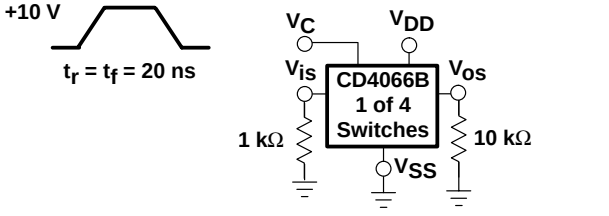
All unused terminals are connected to V_{SS}.

Figure 11. Off-Switch Input or Output Leakage



All unused terminals are connected to V_{SS}.

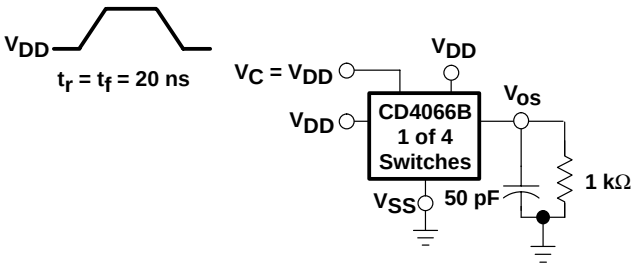
Figure 12. Propagation Delay-Time Signal Input (V_{is}) to Signal Output (V_{os})



All unused terminals are connected to V_{SS}.

Figure 13. Crosstalk-Control Input to Signal Output

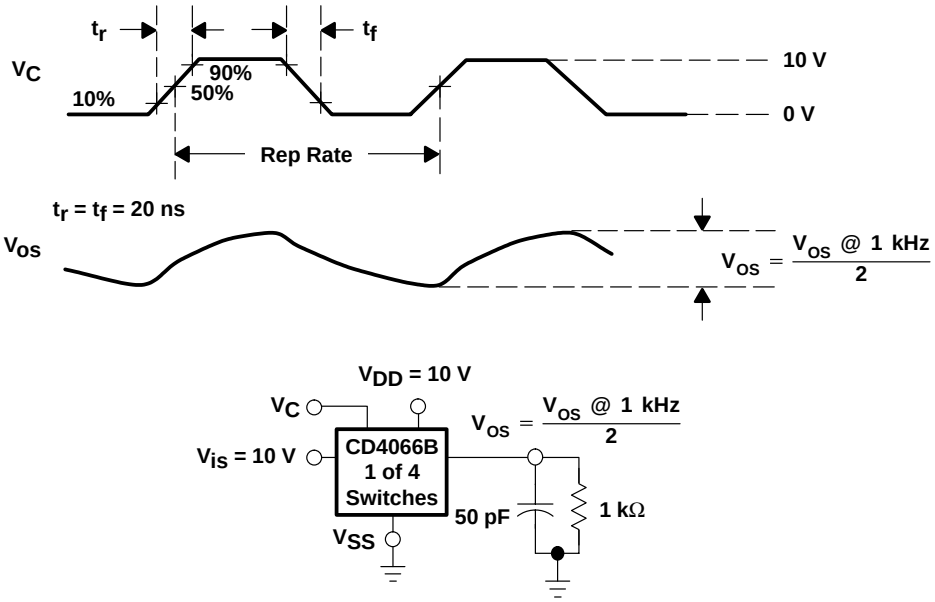
TYPICAL CHARACTERISTICS



NOTES: A. All unused terminals are connected to V_{SS}.
B. Delay is measured at V_{OS} level of +10% from ground (turn-on) or on-state output level (turn-off).

92CS-30925

Figure 14. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output

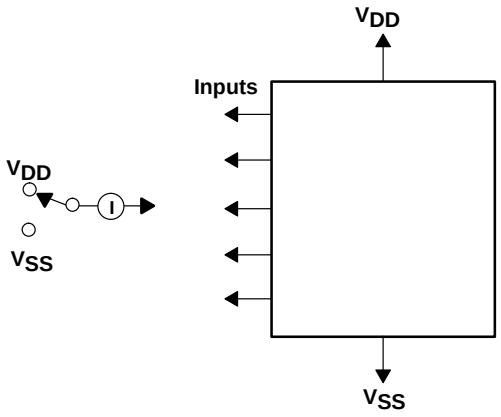


All unused terminals are connected to V_{SS}

92CS-30925

Figure 15. Maximum Allowable Control-Input Repetition Rate

TYPICAL CHARACTERISTICS



Measure inputs sequentially, to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

Figure 16. Input Leakage-Current Test Circuit

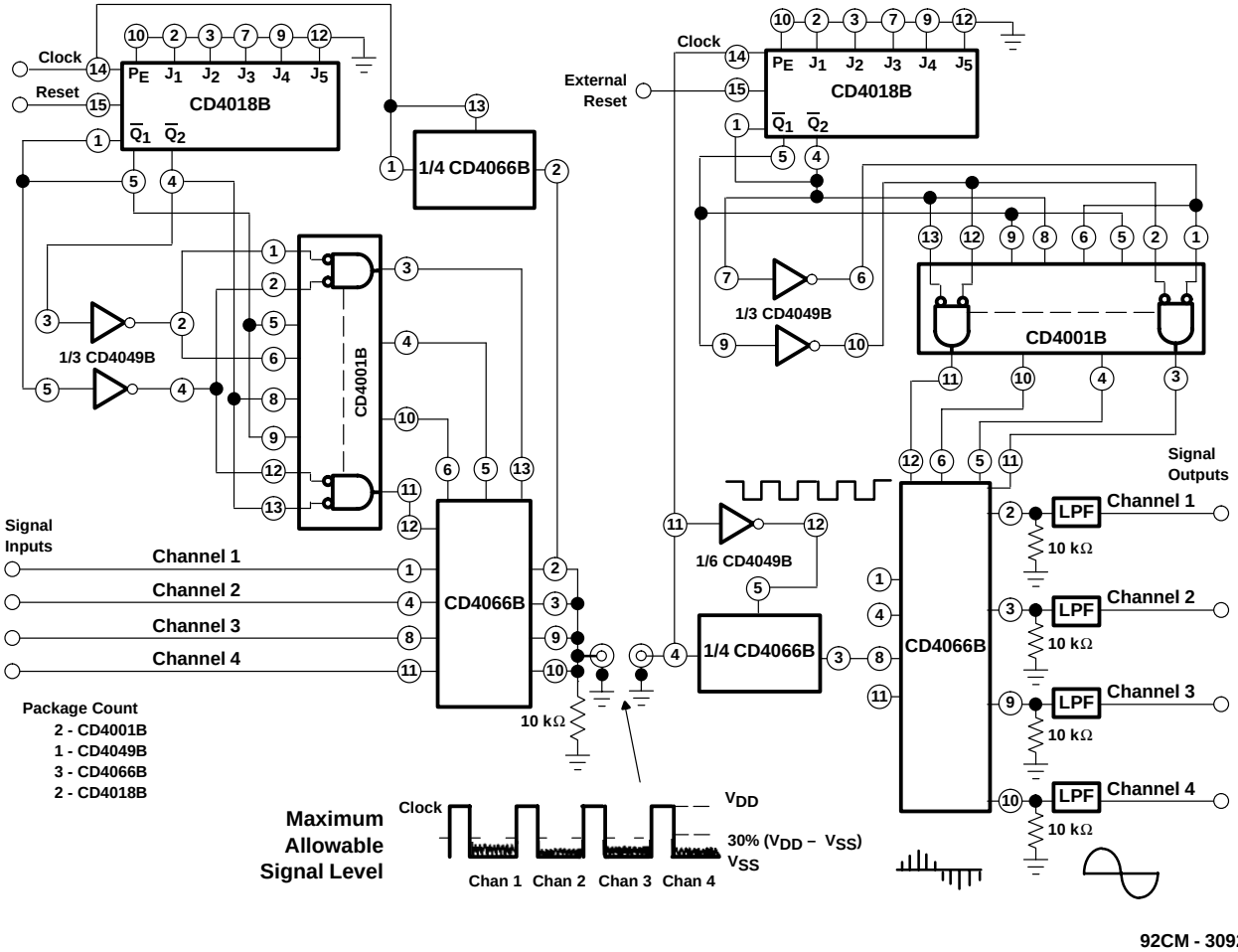
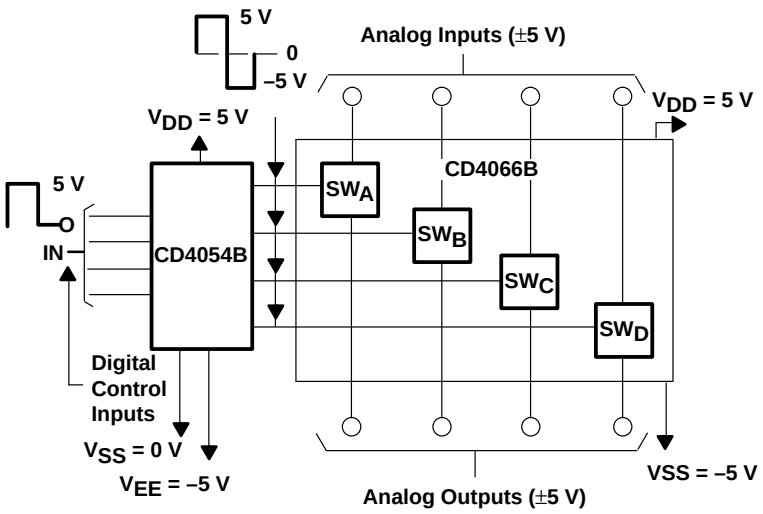


Figure 17. Four-Channel PAM Multiplex System Diagram

TYPICAL CHARACTERISTICS



92CS - 30927

Figure 18. Bidirectional Signal Transmission Via Digital Control Logic

APPLICATION INFORMATION

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.

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