PROGRAMMABLE 27-BIT DISPLAY SERIAL INTERFACE TRANSMITTER

FEATURES

- **FlatLink™3G Serial-Interface Technology**
- **Compatible With FlatLink3G Receivers Such as SN65LVDS306**
- **Input Supports 24-bit RGB Video Mode Interface**
- **24-Bit RGB Data, 3 Control Bits, 1 Parity Bit, and 2 Reserved Bits Transmitted Over One Differential Line**
- **SubLVDS Differential Voltage Levels**
- **Effective Data Throughput up to 405 Mbps**
- **Three Operating Modes to Conserve Power**
  - **Active-Mode QVGA 17.4 mW (Typical)**
  - **Shutdown Mode ≈ 0.5 μA (Typical)**
  - **Standby Mode ≈ 0.5 μA (Typical)**
- **Bus Swap for Increased PCB Layout Flexibility**
- **1.8-V Supply Voltage**
- **ESD Rating > 2 kV (HBM)**
- **Typical Application: Host-Controller to Display-Module Interface**
- **Pixel Clock Range of 4 MHz–15 MHz**
- **Failsafe on all CMOS Inputs**
- **Packaging: 80-Terminal 5-mm × 5-mm μBGA®**

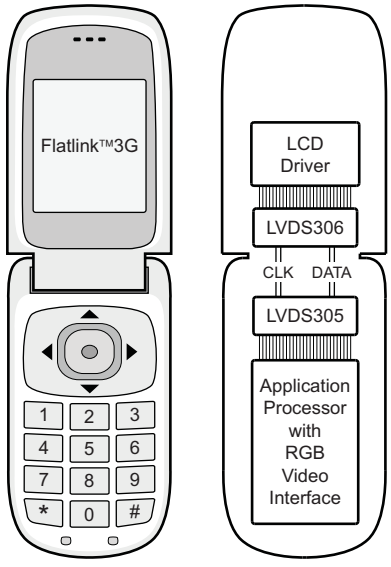
DESCRIPTION

The SN65LVDS305 serializer device converts 27 parallel data inputs to one sub-low-voltage differential signaling (SubLVDS) serial output. It loads a shift register with 24 pixel bits and 3 control bits from the parallel CMOS input interface. In addition to the 27 data bits, the device adds a parity bit and two reserved bits into a 30-bit data word. Each word is latched into the device by the pixel clock (PCLK). The parity bit (odd parity) allows a receiver to detect single bit errors. The serial shift register is uploaded at 30 times the pixel-clock data rate. A copy of the pixel clock is output on a separate differential output.

FPC cabling typically interconnects the SN65LVDS305 with the display. Compared to parallel signaling, the SN65LVDS305 outputs reduce the EMI of the interconnect by over 20 dB.

The SN65LVDS305 supports three power modes (shutdown, standby and active) to conserve power. When transmitting, the PLL locks to the incoming pixel clock, PCLK, and generates an internal high-speed clock at the line rate of the data lines. The parallel data are latched on the rising or falling edge of PCLK, as selected by the external control signal CPOL. The serialized data is presented on the serial output, D, together with a recreated PCLK generated from the internal high-speed clock that is output on CLK. If PCLK stops, the device enters a standby mode to conserve power.

The parallel (CMOS) input bus offers a bus-swap feature. The SWAP terminal configures the input order of the pixel data to be either R[7:0]. G[7:0], B[7:0], VS, HS, DE or B[0:7]. G[0:7], R[0:7], VS, HS, DE. This gives a PCB designer the flexibility to better match the bus to the host controller pinout or to put the transmitter device on the top side or the bottom side of the PCB.

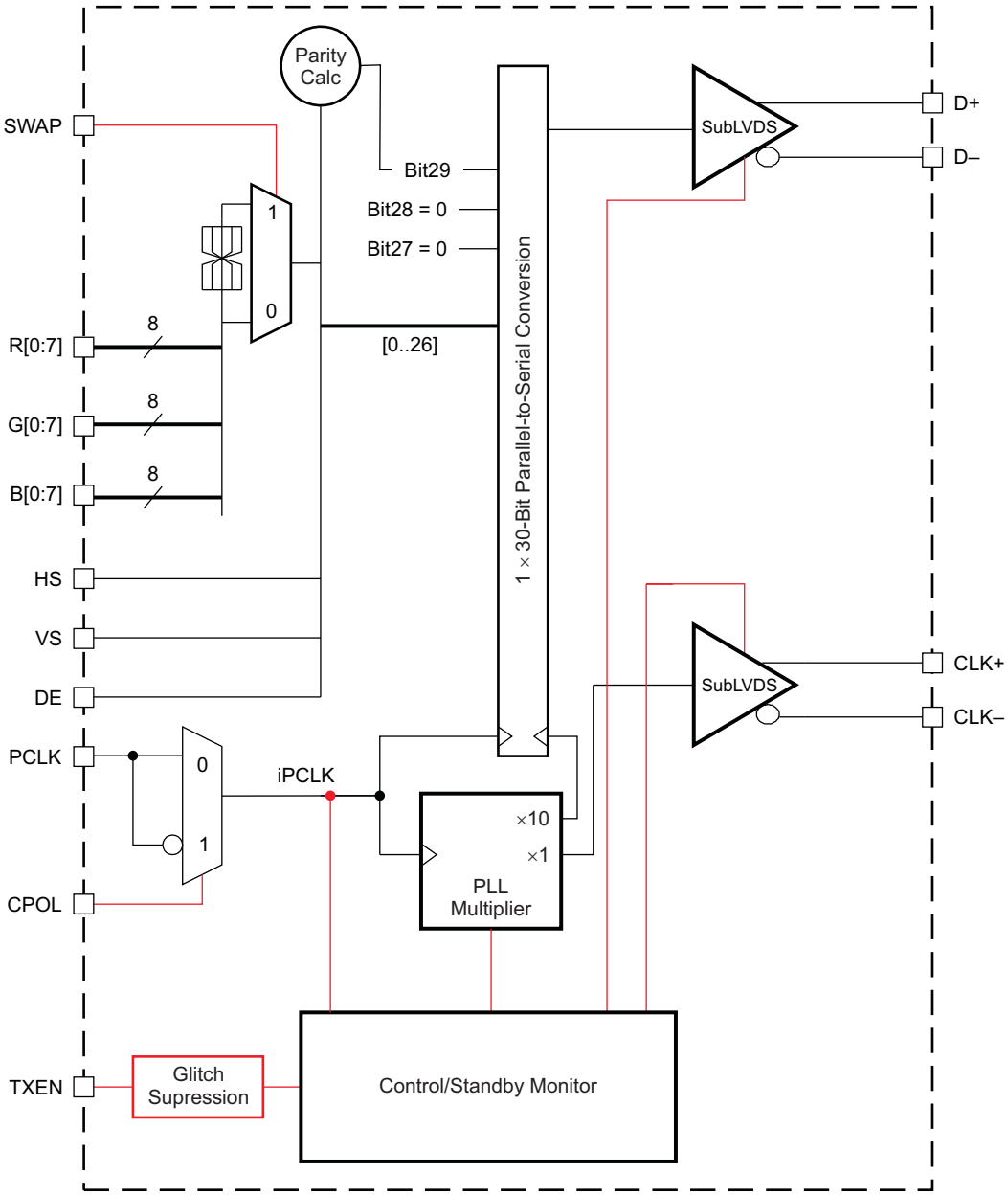


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

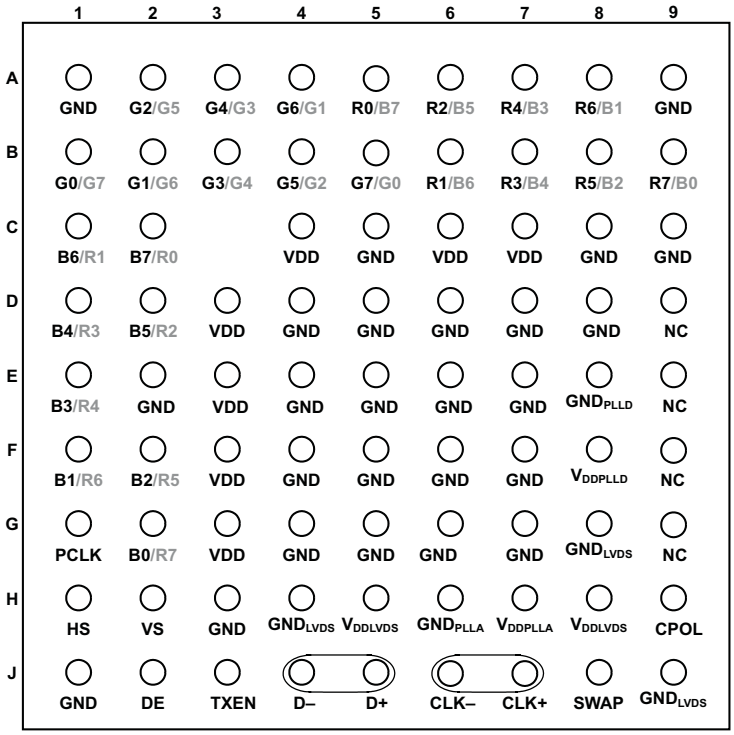
DESCRIPTION (CONTINUED)

The TXEN input can be used to put the SN65LVDS305 in a shutdown mode. The SN65LVDS305 enters an active standby mode if the input clock, PCLK, stops. This minimizes power consumption without the need for controlling an external terminal. The SN65LVDS305 is characterized for operation over ambient air temperatures of –40°C to 85°C. All CMOS inputs offer failsafe to protect the input from damage during power up and to avoid current flow into the device inputs during power up. An input voltage of up to 2.165 V can be applied to all CMOS inputs while V_{DD} is between 0 V and 1.65 V.

Functional Block Diagram



PINOUT – TOP VIEW



RGB Input pin assignment based on SWAP pin setting:

SWAP=0/SWAP=1

PINOUT – TOP VIEW (continued)

SWAP TERMINAL FUNCTIONALITY

The SWAP terminal allows the pcb designer to reverse the RGB bus, thus minimize potential signal crossovers due to signal routing. Figure 1 and Figure 2 show the RGB signal terminal assignment based on the SWAP terminal setting.

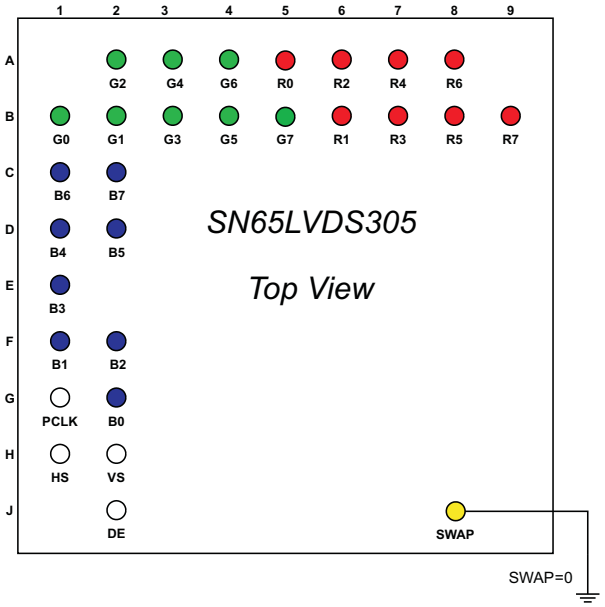


Figure 1. SWAP TERMINAL = 0

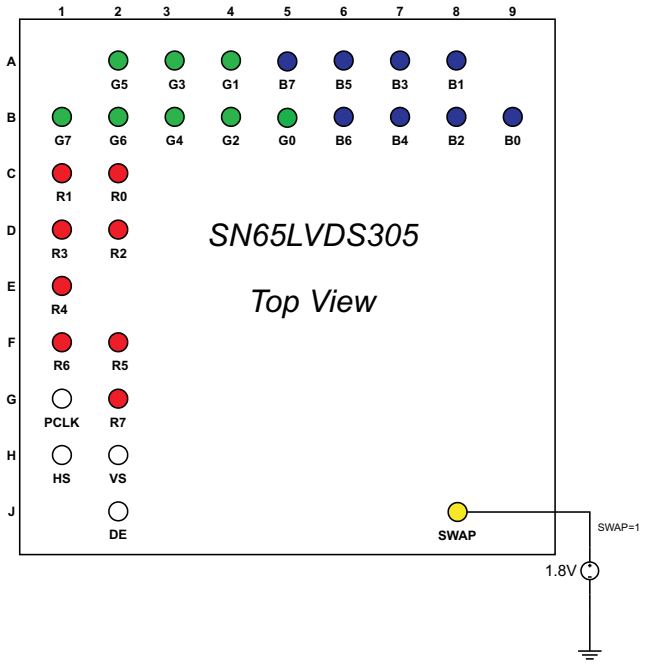


Figure 2. SWAP Terminal = 1

PINOUT – TOP VIEW (continued)

Table 1. NUMERIC TERMINAL LIST

TERMINAL	SWAP	SIGNAL	TERMINAL	SWAP	SIGNAL	TERMINAL	SWAP	SIGNAL
A1	—	GND	**C1**	0	B6	**F1**	0	B1
A2	0	G2		1	R1		1	R6
	1	G5	**C2**	0	B7	**F2**	0	B2
A3	0	G4		1	R0		1	R5
	1	G3	**C3**	UNPOPULATED		**F3**	—	VDD
A4	0	G6	**C4**	—	VDD	**F4**	—	GND
	1	G1	**C5**	—	GND	**F5**	—	GND
A5	0	R0	**C6**	—	VDD	**F6**	—	GND
	1	B7	**C7**	—	VDD	**F7**	—	GND
A6	0	R2	**C8**	—	GND	**F8**	—	V_{DDPLLD}
	1	B5	**C9**	—	GND	**F9**	—	NC
A7	0	R4	**D1**	0	B4	**G1**	—	PCLK
	1	B3		1	R3	**G2**	0	B0
A8	0	R6	**D2**	0	B5		1	R7
	1	B1		1	R2	**G3**	—	V_{DD}
A9	—	GND	**D3**	—	VDD	**G4**	—	GND
B1	0	G0	**D4**	—	GND	**G5**	—	GND
	1	G7	**D5**	—	GND	**G6**	—	GND
B2	0	G1	**D6**	—	GND	**G7**	—	GND
	1	G6	**D7**	—	GND	**G8**	—	GND_{LVDS}
B3	0	G3	**D8**	—	GND	**G9**	—	NC
	1	G4	**D9**	—	NC	**H1**	—	HS
B4	0	G5	**E1**	0	B3	**H2**	—	VS
	1	G2		1	R4	**H3**	—	GND
B5	0	G7	**E2**	—	GND	**H4**	—	GND_{LVDS}
	1	G0	**E3**	—	VDD	**H5**	—	V_{DDLVDS}
B6	0	R1	**E4**	—	GND	**H6**	—	GND_{PLLA}
	1	B6	**E5**	—	GND	**H7**	—	V_{DDPLLA}
B7	0	R3	**E6**	—	GND	**H8**	—	V_{DDLVDS}
	1	B4	**E7**	—	GND	**H9**	—	CPOL
B8	0	R5	**E8**	—	GND_{PLLD}	**J1**	—	GND
	1	B2	**E9**	—	NC	**J2**	—	DE
B9	0	R7				**J3**	—	TXEN
	1	B0				**J4**	—	D–
						J5	—	D+
						J6	—	CLK–
						J7	—	CLK+
						J8	—	SWAP
						J9	—	GND_{LVDS}

Table 2. TERMINAL FUNCTIONS

NAME	I/O	DESCRIPTION
D+, D–	SubLVDS Out	SubLVDS data link (active during normal operation)
CLK+, CLK–		SubLVDS output clock; clock polarity is fixed.
R0–R7	CMOS IN	Red pixel data (8); terminal assignment depends on SWAP terminal setting.
G0–G7		Green pixel data (8); terminal assignment depends on SWAP terminal setting.
B0–B7		Blue pixel data (8); terminal assignment depends on SWAP terminal setting.
HS		Horizontal sync
VS		Vertical sync
DE		Data enable
PCLK		Input pixel clock; rising or falling clock polarity is selected by control input CPOL.
TXEN		Disables the CMOS drivers and turns off the PLL, putting device in shutdown mode 1 – Transmitter enabled 0 – Transmitter disabled (shutdown) Note: The TXEN input incorporates glitch-suppression logic to avoid device malfunction on short input spikes. It is necessary to pull TXEN high for longer than 10 μs to enable the transmitter. It is necessary to pull the TXEN input low for longer than 10 μs to disable the transmitter. At power up, the transmitter is enabled immediately if TXEN = 1 and disabled if TXEN = 0.
CPOL	CMOS In	Input clock polarity selection 0 – rising edge clocking 1 – falling edge clocking
SWAP	CMOS In	Bus swap. Swaps the bus terminals to allow device placement on top or bottom of pcb. See pinout drawing for terminal assignments. 0 – data input from B0...R7 1 – data input from R7...B0
V_{DD}	Power supply(1)	Supply voltage
GND		Supply ground
V_{DDLVDS}		SubLVDS I/O supply voltage
GND_{LVDS}		SubLVDS ground
V_{DDPLLA}		PLL analog supply voltage
GND_{PLLA}		PLL analog GND
V_{DDPLLD}		PLL digital supply voltage
GND_{PLLD}		PLL digital GND

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

FUNCTIONAL DESCRIPTION

The SN65LVDS305 transmits payload data over a single SubLVDS data pair, D. The PLL locks to PCLK and internally multiplies the clock by a factor of 30. The internal high-speed clock is used to serialize (shift out) the data payload on D. Two reserved bits and the parity bit are added to the data frame. Figure 3 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 30 to recreate the pixel clock, and presented on the SubLVDS CLK output. While in this mode, the PLL can lock to a clock that is in the range of 4 MHz through 15 MHz. This is intended for smaller video display formats (e.g. QVGA to HVGA) .

Figure 3. Data and Clock Output

Power-Down Modes

The SN65LVDS305 transmitter has two power-down modes to facilitate efficient power management.

Shutdown Mode

The SN65LVDS305 enters shutdown mode when the TXEN terminal is asserted low. This turns off all transmitter circuitry, including the CMOS input, PLL, serializer, and SubLVDS transmitter output stage. All outputs are high-impedance. Current consumption in shutdown mode is nearly zero.

Standby Mode

The SN65LVDS305 enters the standby mode if TXEN is high and the PCLK input signal frequency is less than 500 kHz. All circuitry except the PCLK input monitor is shut down, and all outputs enter the high-impedance state. The current consumption in standby mode is very low. When the PCLK input signal is completely stopped, the I_{DD} current consumption is less than 10 µA. The PCLK input must not be left floating.

NOTE:

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. To prevent large leakage current, a CMOS gate must be kept at a valid logic level, either V_{IH} or V_{IL}. This can be achieved by applying an external voltage of V_{IH} or V_{IL} to all SN65LVDS305 inputs.

Active Modes

When TXEN is high and the PCLK input clock signal is faster than 3 MHz, the SN65LVDS305 enters the active mode. Current consumption in the active mode depends on operating frequency and the number of data transitions in the data payload.

Acquire Mode (PLL Approaches Lock)

The PLL is enabled and attempts to lock to the input clock. All outputs remain in the high-impedance state. When the PLL monitor detects stable PLL operation, the device switches from the acquire mode to the transmit mode. For proper device operation, the pixel clock frequency must fall within the valid f_{PCLK} range specified under recommended operating conditions. If the pixel clock frequency is larger than 3MHz but smaller than f_{PCLK}(min), the SN65LVDS305 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into transmit mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

Transmit Mode

After the PLL achieves lock, the device enters the normal transmit mode. The CLK terminal outputs a copy of PCLK.

FUNCTIONAL DESCRIPTION (continued)

Parity Bit Generation

The SN65LVDS305 transmitter calculates the parity of the transmit data word and sets the parity bit accordingly. The parity bit covers the 27-bit data payload consisting of 24 bits of pixel data plus VS, HS, and DE. The two reserved bits are not included in the parity generation. Odd-parity bit signaling is used. The transmitter sets the parity bit if the sum of the 27 data bits result in an even number of ones. The parity bit is cleared otherwise. This allows the receiver to verify parity and detect single bit errors.

Status Detect and Operating Modes Flow diagram

The SN65LVDS305 switches between the power saving and active modes in the following way:

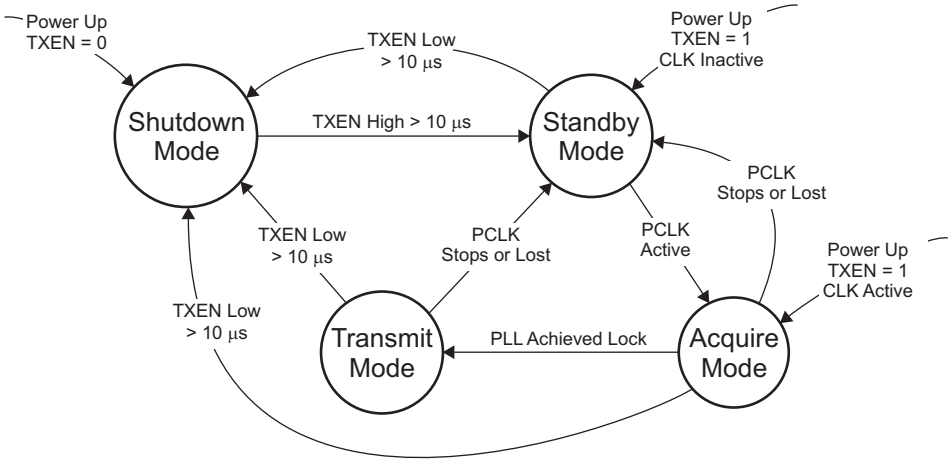


Figure 4. Status Detect and Operating Modes Flow Diagram

Table 3. Status Detect and Operating Modes Descriptions

Mode	Characteristics	Conditions
Shutdown mode	Least amount of power consumption(1) (most circuitry turned off); all outputs are high-impedance.	TXEN is low.(1)(2)
Standby mode	Low power consumption (only clock activity circuit active; PLL is disabled to conserve power); all outputs are high-impedance.	TXEN is high; PCLK input signal is missing or inactive.(2)
Acquire mode	PLL tries to achieve lock; all outputs are high-impedance.	TXEN is high; PCLK input monitor detected input activity.
Transmit mode	Data transfer (normal operation); Transmitter serializes data and transmits data on serial output.	TXEN is high and PLL is locked to incoming clock.

(1) In shutdown mode, all SN65LVDS305 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input terminal remains active.

(2) Leaving inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All inputs must be tied to a valid logic level, V_{IL} or V_{IH}, during shutdown or standby mode.

Table 4. Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → standby	Drive TXEN high to enable transmitter	1. TXEN high > 10 µs 2. Transmitter enters standby mode. a. All outputs are high-impedance. b. Transmitter turns on clock input monitor.
Standby → acquire	Transmitter activity detected	1. PCLK input monitor detects clock input activity. 2. Outputs remain high-impedance. 3. PLL circuit is enabled.
Acquire → transmit	Link is ready to transfer data.	1. PLL is active and approaches lock. 2. PLL achieved lock within 2 ms. 3. Parallel data input latches into shift register . 4. CLK output turns on. 5. Selected data outputs turn on and send out first serial data bit.
Transmit → standby	Request transmitter to enter standby mode by stopping PCLK	1. PCLK Input monitor detects missing PCLK. 2. Transmitter indicates standby, putting all outputs into high-impedance. 3. PLL shuts down. 4. PCLK activity input monitor remains active.
Transmit/standby → shutdown	Turn off transmitter	1. TXEN pulled low for longer than 10 µs 2. Transmitter indicates standby, putting output CLK+ and CLK– into high-impedance state. 3. Transmitter puts all other outputs into high-impedance state. 4. Most IC circuitry is shut down for least power consumption.

ORDERING INFORMATION

PART NUMBER	PACKAGE	SHIPPING METHOD
SN65LVDS305ZQER	ZQE	Reel

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage range, V_{DD}(2), V_{DDPLLA}, V_{DDPLLD}, V_{DDLVDS}		–0.3 to 2.175	V
Voltage range at any input or output terminal	When $V_{DDx} > 0$ V	–0.5 to 2.175	V
	When $V_{DDx} \leq 0$ V	–0.5 to V_{DD} + 2.175	V
Electrostatic discharge	Human-body model(3) (all terminals)	±3	kV
	Charged-device model(4) (all terminals)	±500	V
	Machine model(5) (all terminals)	±200	
Continuous power dissipation		See Dissipation Ratings table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-A.
(4) In accordance with JEDEC Standard 22, Test Method C101.
(5) In accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	T_A < 25°C	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
ZQE	Low-K(2)	592 mW	7.407 mW/°C	148 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-2.

THERMAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS		VALUE	UNIT
P_D Device power dissipation, maximum	V_{DDx} = 1.95 V, T_A = –40°C	PCLK at 4 MHz	22.3	mW
		PCLK = 15 MHz	36.7	

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{DD} V_{DDPLLA} V_{DDPLLD} V_{DDLVDS}	Supply voltages		1.65	1.8	1.95	V
$V_{DDn(PP)}$	Supply voltage noise magnitude 50 MHz (all supplies)	Test setup see Figure 10 f(noise) = 1Hz to 2 GHz			100	mV
f_{PCLK}	Pixel clock frequency	1-channel transmit mode, see Figure 3	4		15	MHz
		Frequency threshold Standby mode to active mode(2), see Figure 14	0.5		3	
t_H x f_{PCLK}	PCLK input duty cycle		0.33		0.67	
T_A	Operating free-air temperature		–40		85	°C
$t_{jit(per)PCLK}$	PCLK RMS period jitter(3)	Measured on PCLK input			5	ps-rms
$t_{jit(TJ)PCLK}$	PCLK total jitter				0.05/f_{PCLK}	s
$t_{jit(CC)PCLK}$	PCLK peak cycle-to-cycle jitter(4)				0.02/f_{PCLK}	s
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, CPOL, TXEN, SWAP						
V_{IH}	High-level input voltage		0.7 V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage				0.3 V_{DD}	V
t_{DS}	Data set up time prior to PCLK transition	f (PCLK) = 10 MHz; see Figure 6	2			ns
t_{DH}	Data hold time after PCLK transition		2			ns

(1) Unused single-ended inputs must be held high or low to prevent them from floating.
(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS305 into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS305. Input frequencies beyond 3 MHz activate the SN65LVDS305.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles over a random sample of 1,000 adjacent cycle pairs.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{DD}	$V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$, $R_{L(PCLK)} = R_{L(D)} =$ 100 Ω, $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, TXEN at V_{DD}, alternating 1010 serial bit pattern	f_{PCLK} = 4 MHz		9	11.4	mA
		f_{PCLK} = 6 MHz		10.6	12.6	
		f_{PCLK} = 15 MHz		16	18.8	
	$V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$, $R_{L(PCLK)} = R_{L(D)} =$ 100 Ω, $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, TXEN at V_{DD}, typical power test pattern (see Table 6)	f_{PCLK} = 4 MHz		8		mA
		f_{PCLK} = 6 MHz		8.9		
		f_{PCLK} = 15 MHz		14		
	Standby mode	$V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}$, $R_{L(PCLK)} = R_{L(D)} = 100$ Ω, $V_{IH} = V_{DD}$, $V_{IL} = 0$ V, all inputs held static high or static low		0.61	10	µA
	Shutdown mode			0.55	10	µA

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

OUTPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
subLVDS output (D+, D–, CLK+, and CLK–)						
$V_{OC(SS)M}$	Steady-state common-mode output voltage	Output load; see Figure 8	0.8	0.9	1.0	V
$V_{OCM(SS)}$	Change in steady-state common-mode output voltage		–10		10	mV
$V_{OCM(PP)}$	Peak-to-peak common mode output voltage				75	mV
$\|V_{OD}\|$	Differential output voltage magnitude $\|V_{Dx+} - V_{Dx-}\|$, $\|V_{CLK+} - V_{CLK-}\|$		100	150	200	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage between logic states		–10		10	mV
$Z_{OD(CLK)}$	Differential small-signal output impedance	TXEN at V_{DD}		210		Ω
I_{OSD}	Differential short-circuit output current	V_{OD} = 0 V, f_{PCLK} = 15 MHz			10	mA
I_{OS}	Short circuit output current(2)	V_O = 0 V or V_{DD}		5		
I_{OZ}	High-impedance state output current	V_O = 0 V or V_{DD}(max), TXEN at GND	–3		3	µA

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.
(2) All SN65LVDS305 outputs tolerate shorts to GND or V_{DD} without permanent device damage.

INPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, CPOL, TXEN, SWAP						
I_{IH}	High-level input current	$V_{IN} = 0.7\ V_{DD}$	–200		200	nA
I_{IL}	Low-level input current	$V_{IN} = 0.3\ V_{DD}$	–200		200	
C_{IN}	Input capacitance			1.5		pF

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_r	20%-to-80% differential output signal rise time	See Figure 7 and Figure 8		250		500	ps
t_f	20%-to-80% differential output signal fall time	See Figure 7 and Figure 8		250		500	ps
f_{BW}	PLL bandwidth (3-dB cutoff frequency)	Tested from PCLK input to CLK output, See Figure 5(2)	f_{PCLK} = 15 MHz			0.076 f_{PCLK}	MHz
$t_{pd(L)}$	Propagation delay time, input to serial output (data latency Figure 9)	TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω		0.8/f_{PCLK}	1/f_{PCLK}	1.2/f_{PCLK}	s
$t_H \times f_{CLK0}$	Output CLK duty cycle			0.45	0.5	0.55	
t_{GS}	TXEN glitch suppression pulse width(3)	V_{IH}=V_{DD}, V_{IL}=GND, TXEN toggles between V_{IL} and V_{IH}, see Figure 12 and Figure 13		3.8		10	µs
t_{pwrup}	Enable time from power down (↑TXEN)	Time from TXEN pulled high to CLK and D outputs enabled and transmit valid data; see Figure 13			0.24	2	ms
t_{pwrdn}	Disable time from active mode (↓TXEN)	TXEN is pulled low during transmit mode; time measurement until output is disabled and PLL is shut down; see Figure 13			0.5	11	µs
t_{wakup}	Enable time from standby (↕PCLK)	TXEN at V_{DD}; device in standby; time measurement from PCLK starts switching to CLK and D outputs enabled and transmit valid data; see Figure 13			0.23	2	ms
t_{sleep}	Disable time from active mode (PCLK stopping)	TXEN at V_{DD}; device is transmitting; time measurement from PCLK input signal stops until CLK + D outputs are disabled and PLL is disabled; see Figure 13			0.4	100	µs

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.
(2) The maximum limit is based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on automatic test equipment (ATE).
(3) The TXEN input incorporates glitch-suppression circuitry to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.

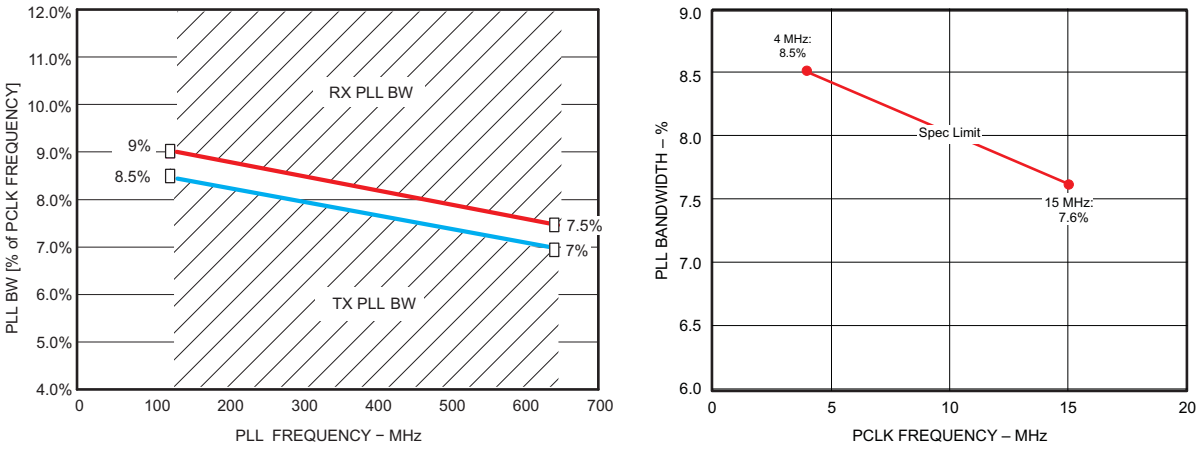


Figure 5. SN65LVDS305 PLL Bandwidth (Also Showing the SN65LVDS306 PLL Bandwidth)

TIMING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PPOSX}	Output pulse position, serial data to ↑CLK; see (1)(2)and Figure 11	x = 0..29, f_{PCLK} = 15 MHz; TXEN at V_{DD}, V_{IH} = V_{DD}, V_{IL} = GND, R_L = 100 Ω, test pattern as in Table 8(3)	$\frac{x}{30 \cdot f_{PCLK}} - 330\ ps$		$\frac{x}{30 \cdot f_{PCLK}} + 330\ ps$	ps
		x = 0..29, f_{PCLK} = 4 MHz to 15 MHz (4)	$\frac{x - 0.1845}{30 \cdot f_{PCLK}}$		$\frac{x + 0.1845}{30 \cdot f_{PCLK}}$	

(1) This number also includes the high-frequency random and deterministic PLL clock jitter that is not traceable by the SN65LVDS306 receiver PLL; tPPosx represents the total timing uncertainty of the transmitter necessary to calculate the jitter budget when combined with the SN65LVDS306 receiver.
(2) The pulse position min/max variation is given with a bit error rate target of 10^{-12}; the measurement estimates the random jitter contribution to the total jitter by multiplying the random RMS jitter by the factor 14; measurements of the total jitter are taken with > 10^{-12} samples.
(3) The minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on automatic test equipment (ATE).
(4) These minimum and maximum limits are simulated only.

PARAMETER MEASUREMENT INFORMATION

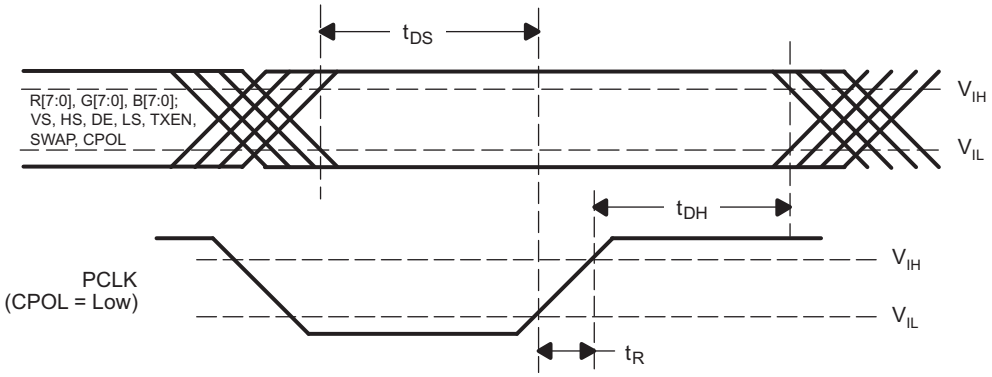


Figure 6. Setup/Hold Time

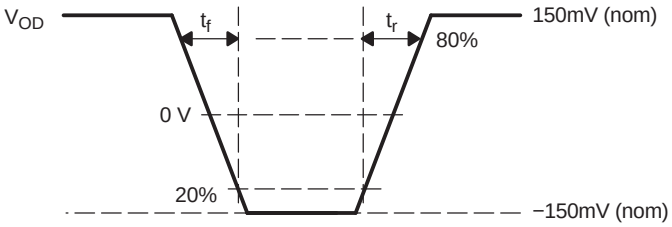
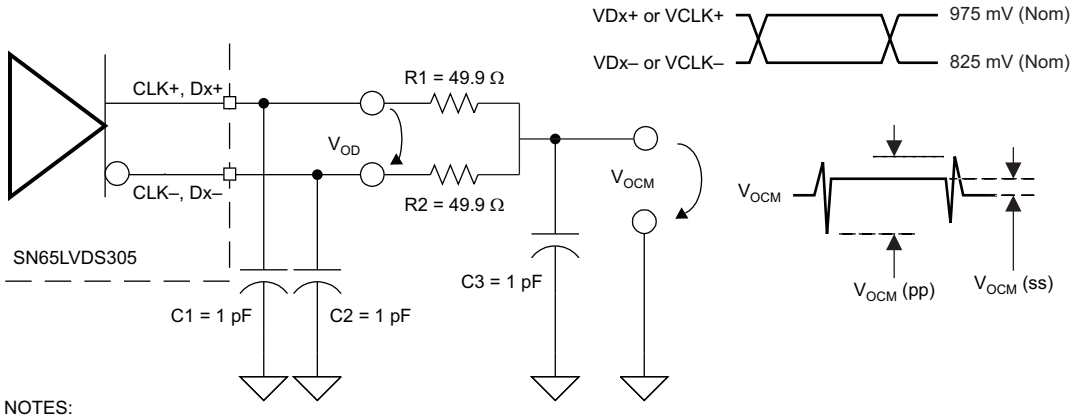


Figure 7. Rise and Fall Time Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



NOTES:
A. 15-MHz output test pattern on all differential outputs (CLK and D):
this is achieved by: 1. f_{PCLK} = 15 MHz
2. Inputs R[7:0] connected to V_{DD}, all other data inputs set to GND.
B. C1, C2, and C3 include instrumentation and fixture capacitance, tolerance ±20%; C, R1, and R2 tolerance ±1%
C. The measurement of V_{OCM} (pp) and V_{OC}(ss) are taken with test equipment bandwidth >1 GHz.

Figure 8. Driver Output Voltage Test Circuit and Definitions

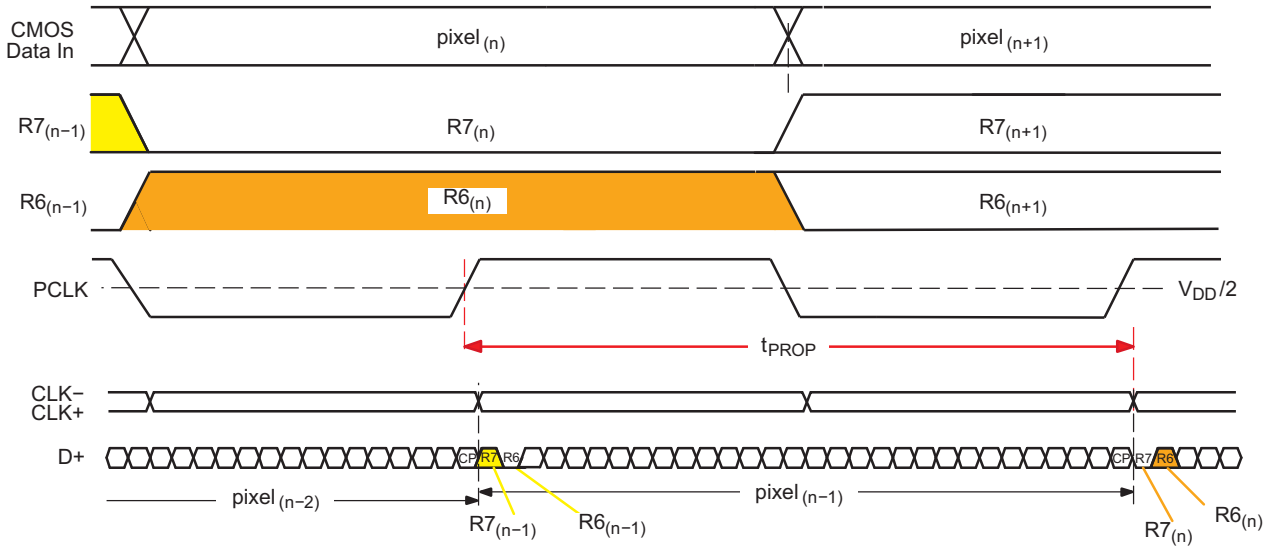


Figure 9. $t_{pd(L)}$ Propagation Delay Input to Output (CPOL = 0)

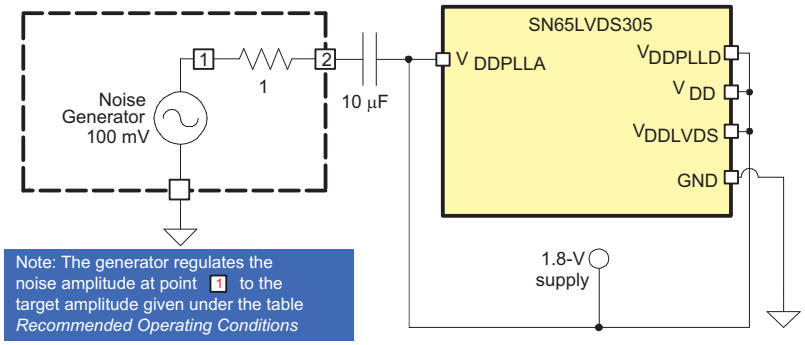


Figure 10. Power Supply Noise Test Setup

PARAMETER MEASUREMENT INFORMATION (continued)

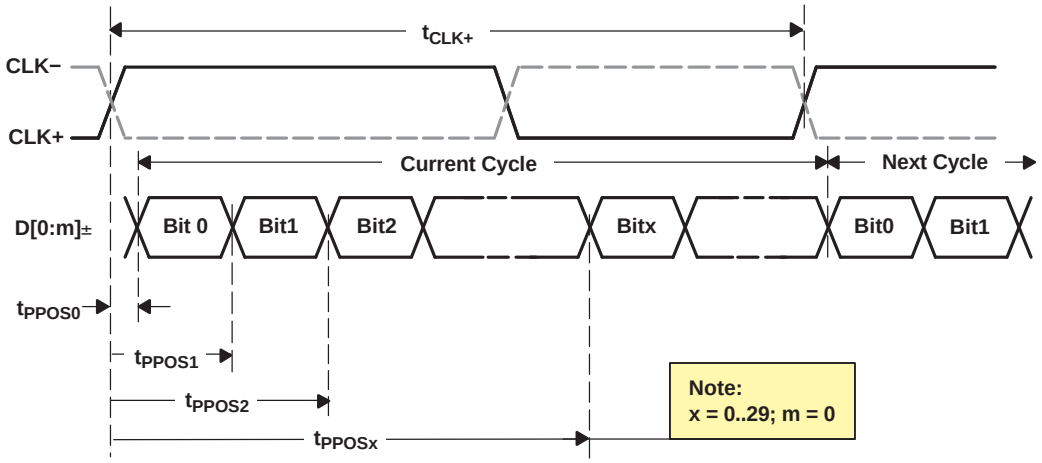


Figure 11. $t_{SK(0)}$ SubLVDS Output Pulse Position Measurement

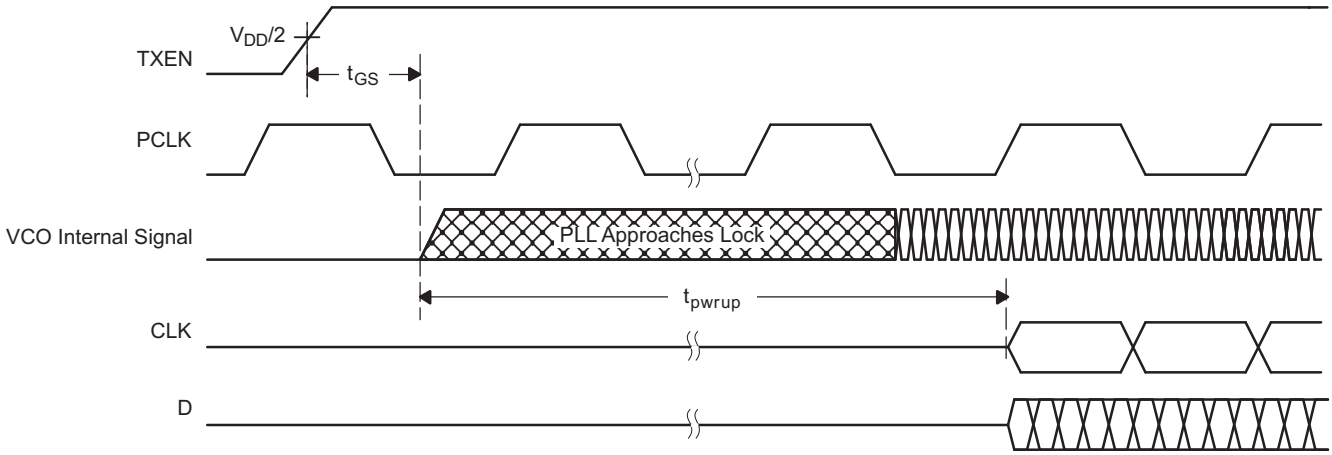


Figure 12. Transmitter Behavior While Approaching Sync

PARAMETER MEASUREMENT INFORMATION (continued)

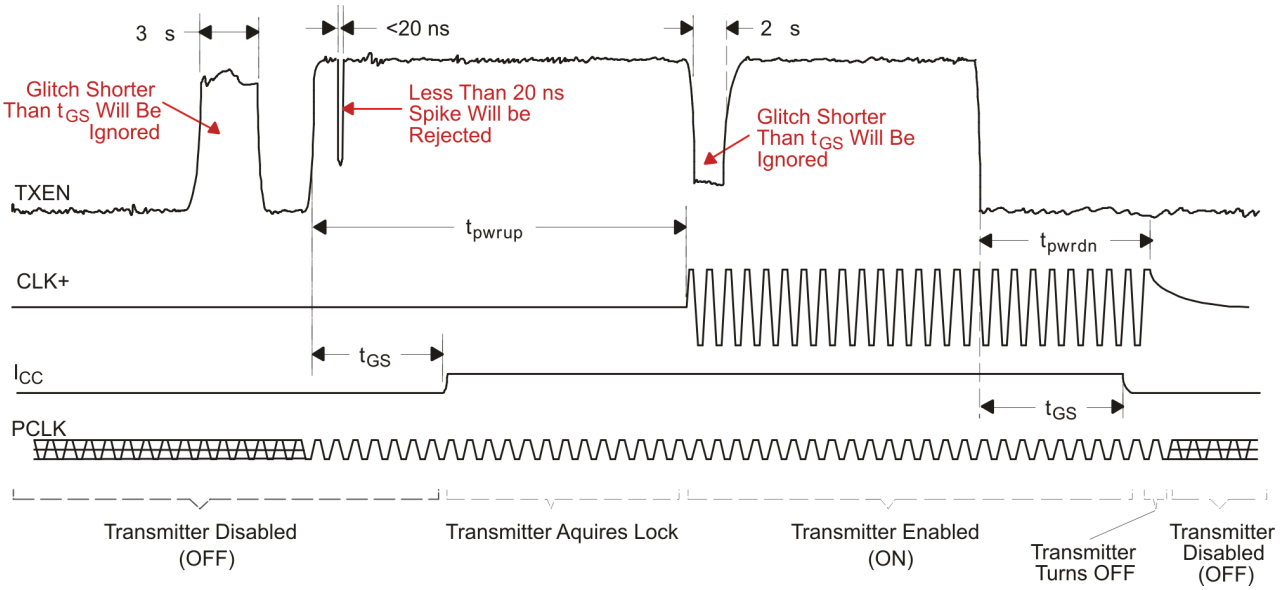


Figure 13. Transmitter Enable Glitch Suppression Time

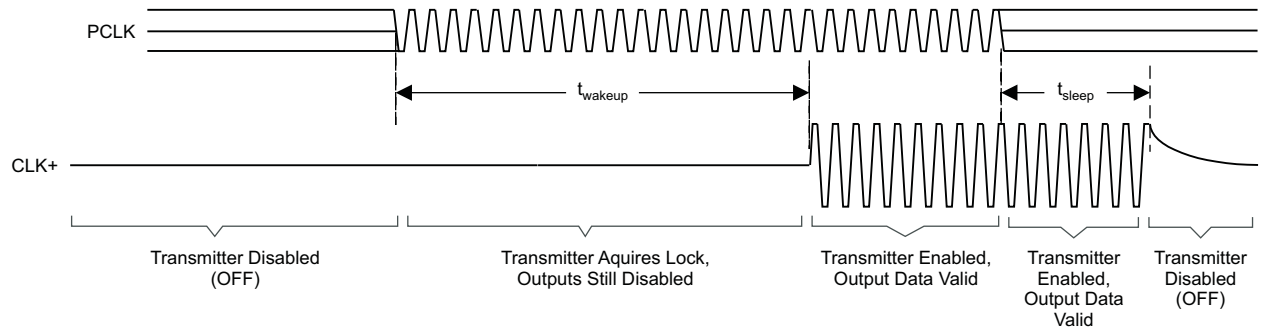


Figure 14. Standby Detection

Power Consumption Tests

Table 5 shows an example test pattern word.

Table 5. Example Test Pattern Word

Word	R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x7C3E1E7

7				C				3				E				1				E				7			
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	0	VS	HS	DE
0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1

Typical IC Power-Consumption Test Pattern

The typical power consumption test pattern consists of sixteen 30-bit transmit words. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 6. Typical IC Power-Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000007
2	0xFFF0007
3	0x01FFF47
4	0xF0E07F7
5	0x7C3E1E7
6	0xE707C37
7	0xE1CE6C7
8	0xF1B9237
9	0x91BB347
10	0xD4CCC67
11	0xAD53377
12	0xACB2207
13	0xAAB2697
14	0x5556957
15	0xAAAAAB3
16	0xAAAAAA5

Maximum Power-Consumption Test Pattern

The maximum (or worst-case) power consumption of the SN65LVDS305 is tested using the two different test patterns shown in table. The test patterns consist of sixteen 30-bit transmit words. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 7. Worst-Case Power-Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0xAAAAAA5
2	0x5555555

Output Skew Pulse Position and Jitter Performance

The following test patterns are used to measure the output skew pulse position and the jitter performance of the SN65LVDS305. The jitter test patterns stress the interconnect for worst-case ISI. Each pattern is self-repeating for the duration of the test.

Table 8. Transmit Jitter Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE
1	0x0000001
2	0x0000031
3	0x00000F1
4	0x00003F1
5	0x0000FF1
6	0x0003FF1
7	0x000FFF1
8	0x0F0F0F1
9	0x0C30C31
10	0x0842111
11	0x1C71C71
12	0x18C6311
13	0x1111111
14	0x3333331
15	0x2452413
16	0x22A2A25
17	0x5555553
18	0xDB6DB65
19	0xCCCCCC1
20	0xEEEEEE1
21	0xE739CE1
22	0xE38E381
23	0xF7BDEE1
24	0xF3CF3C1
25	0xF0F0F01
26	0xFFF0001
27	0xFFFC001
28	0xFFFF001
29	0xFFFFC01
30	0xFFFFF01
31	0xFFFFFC1
32	0xFFFFFF1

TYPICAL CHARACTERISTICS

POWERDOWN, STANDBY SUPPLY CURRENT vs TEMPERATURE

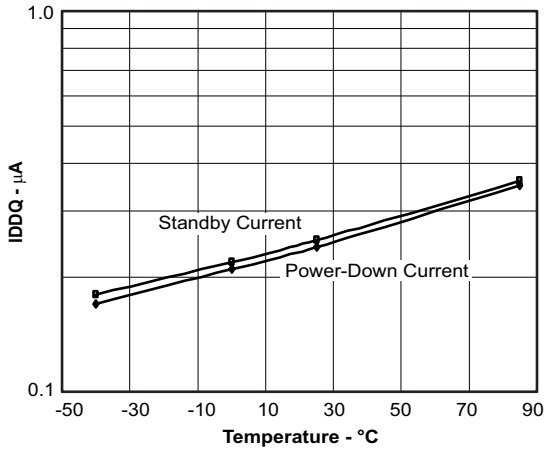


Figure 15.

SUPPLY CURRENT I_{DD} vs TEMPERATURE

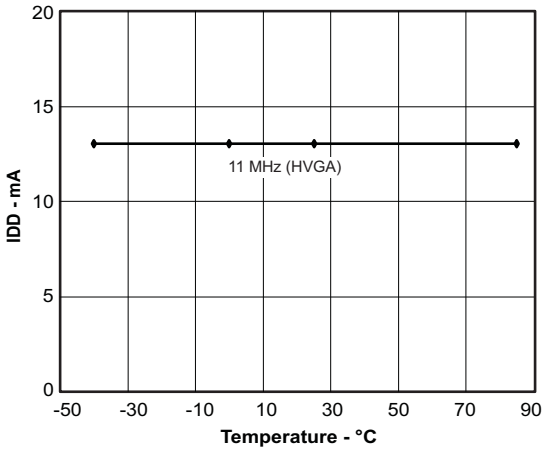


Figure 16.

SUPPLY CURRENT vs PCLK FREQUENCY

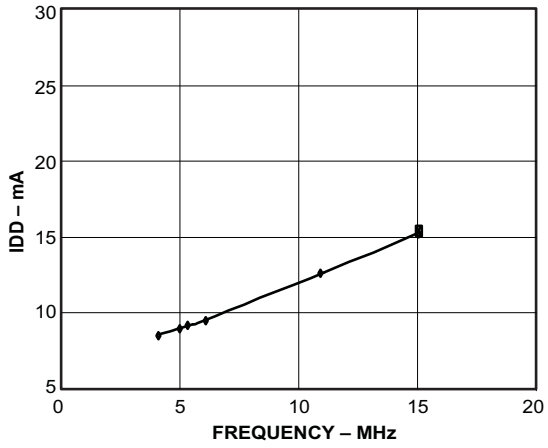


Figure 17.

DIFFERENTIAL OUTPUT SWING vs PCLK FREQUENCY

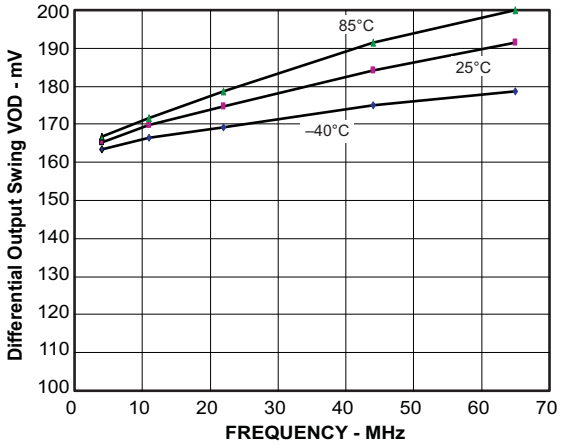


Figure 18.

PLL BANDWIDTH

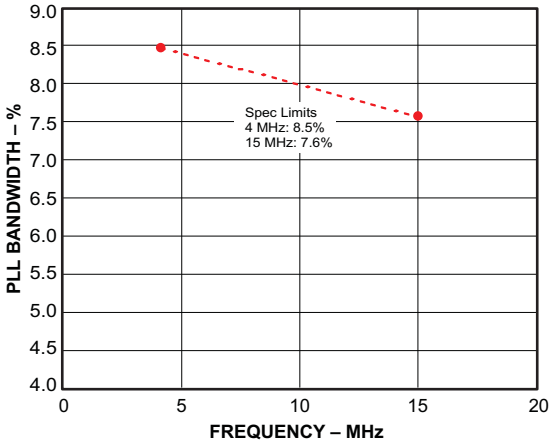


Figure 19.

CYCLE-TO-CYCLE OUTPUT JITTER vs PCLK FREQUENCY

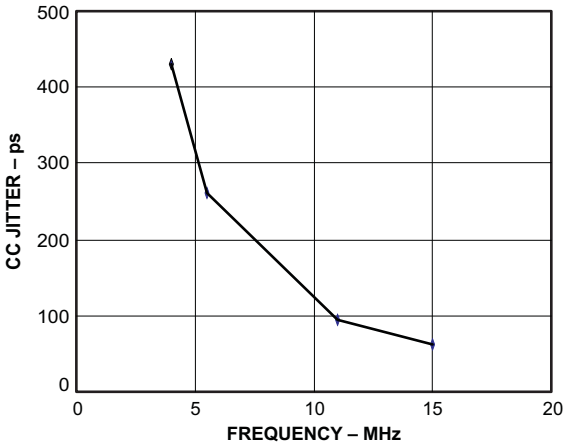


Figure 20.

TYPICAL CHARACTERISTICS (continued)

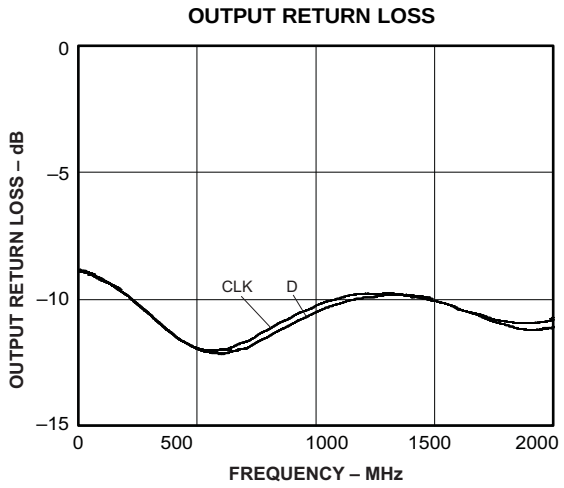


Figure 21.

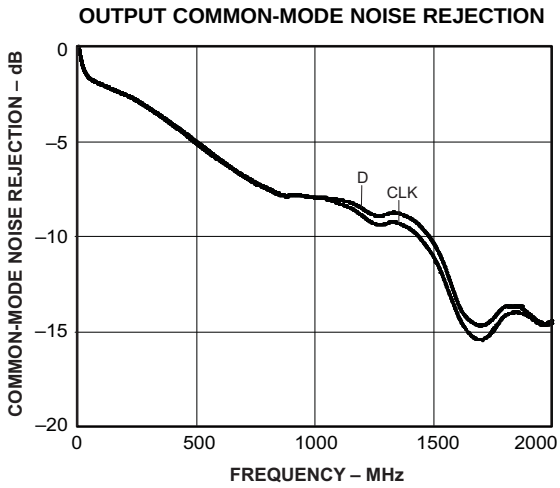


Figure 22.

APPLICATION INFORMATION

Preventing Increased Leakage Currents in Control Inputs

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. Do not leave any CMOS Input unconnected or floating. Every input must be connected to a valid logic level, V_{IH} or V_{OL}, while power is supplied to V_{DD}. This also minimizes the power consumption of standby and power-down modes.

Power Supply Design Recommendation

For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

Decoupling Recommendation

The SN65LVDS305 was designed to operate reliably in a constricted environment with other digital switching ICs. In cell phone designs, the SN65LVDS305 often shares a power supply with the application processor. The SN65LVDS305 can operate with power-supply noise as specified in *Recommend Operating Conditions*. To minimize the power-supply noise floor, provide good decoupling near the SN65LVDS305 power terminals. The use of four ceramic capacitors (2×0.01 µF and 2×0.1 µF) provides good performance. At the very least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65LVDS305. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and IC power input terminals must be minimized. Placing the capacitor underneath the SN65LVDS305 on the bottom of the pcb is often a good choice.

Typical Application Frequencies

The SN65LVDS305 supports pixel clock frequencies from 4 MHz to 15 MHz. Table 9 provides a few typical display resolution examples and shows the number of data lanes necessary to connect the SN65LVDS305 with the display. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate. Furthermore, the examples in the table assumes a display frame refresh rate of 60 Hz. The actual refresh rate may differ depending on the application-processor clock implementation.

Table 9. Typical Application Data Rates and Serial Lane Usage

Display Screen Resolution	Visible Pixel Count	Blanking Overhead	Display Refresh Rate	Pixel Clock Frequency [MHz]	Serial Data Rate
176 × 220 (QCIF+)	38,720	20%	90 Hz	4.2 MHz	125 Mbps
240 × 320 (QVGA)	76,800		60 Hz	5.5 MHz	166 Mbps
640 × 200	128,000			9.2 MHz	276 Mbps
352 × 416 (CIF+)	146,432			10.5 MHz	316 Mbps
352 × 440	154,880			11.2 MHz	335 Mbps
320 × 480 (HVGA)	153,600			11.1 MHz	332 Mbps
800 × 250	200,000			14.4 MHz	432 Mbps
640 × 320	204,800			14.7 MHz	442 Mbps

Calculation Example: HVGA Display

This example calculation shows a typical half-VGA display with these parameters:

Display resolution:	480 × 320
Frame refresh rate:	58.4 Hz
Vertical visible pixels:	320 lines
Vertical front porch:	10 lines
Vertical sync:	5 lines
Vertical back porch:	3 lines
Horizontal visible pixels:	480 columns
Horizontal front porch:	20 columns
Horizontal sync:	5 columns
Horizontal back porch:	3 columns

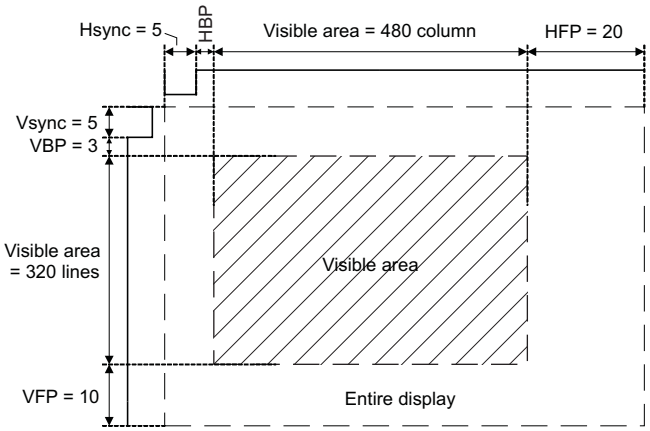


Figure 23. HVGA Display Parameters

Calculation of the total number of pixels and blanking overhead:

Visible area pixel count:	480 × 320 = 153,600 pixels
Total frame pixel count:	(480 + 20 + 5 + 3) × (320 + 10 + 5 + 3) = 171,704 pixels
Blanking overhead:	(171,704 – 153,600) ÷ 153,600 ≈ 11.8%

The application requires following serial-link parameters:

Pixel clk frequency:	171,704 × 58.4 Hz = 10 MHz
Serial data rate:	10 MHz × 30 bits = 300 Mbps

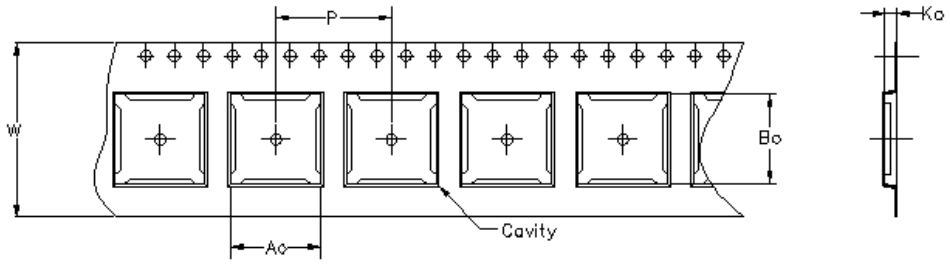
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDS305ZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

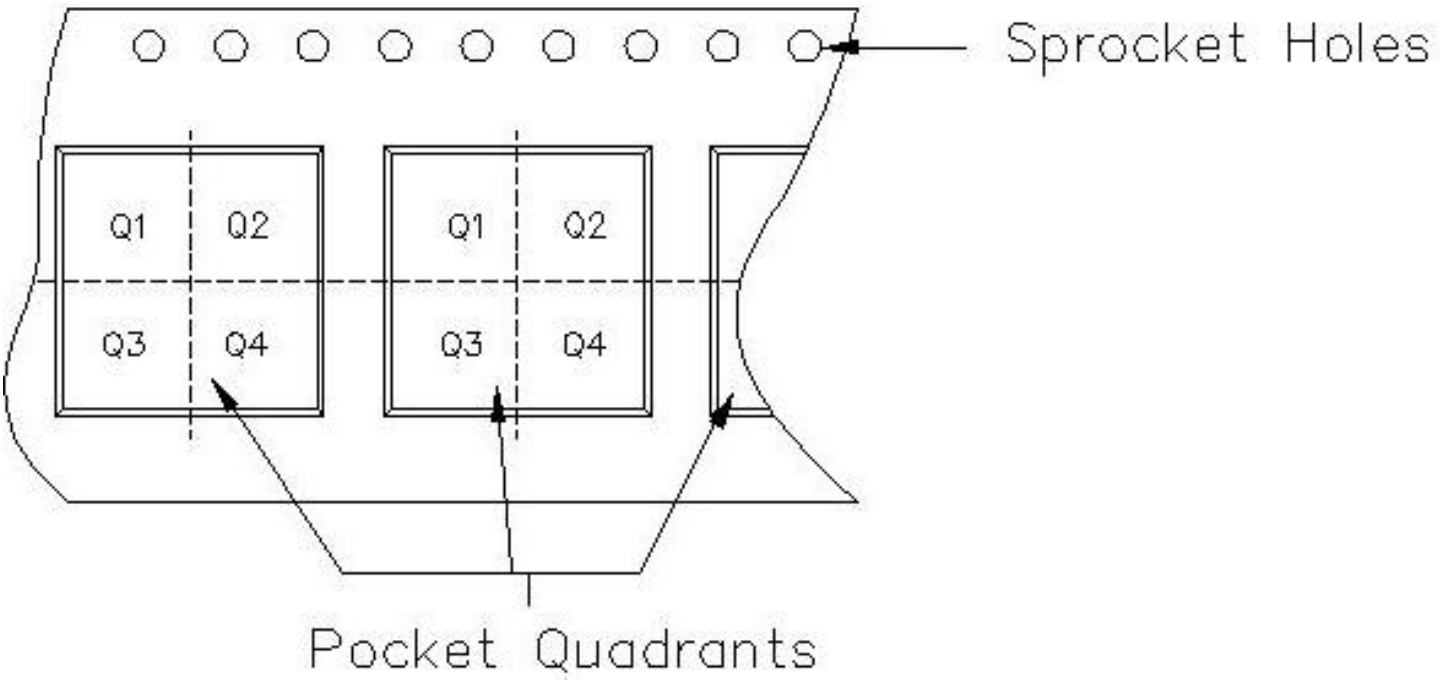
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



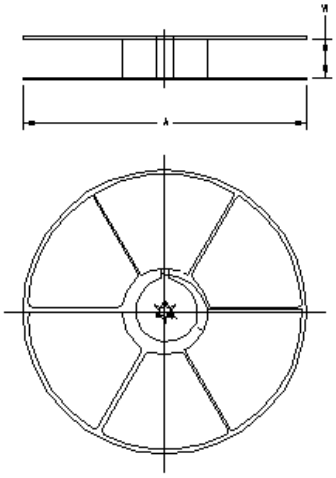
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



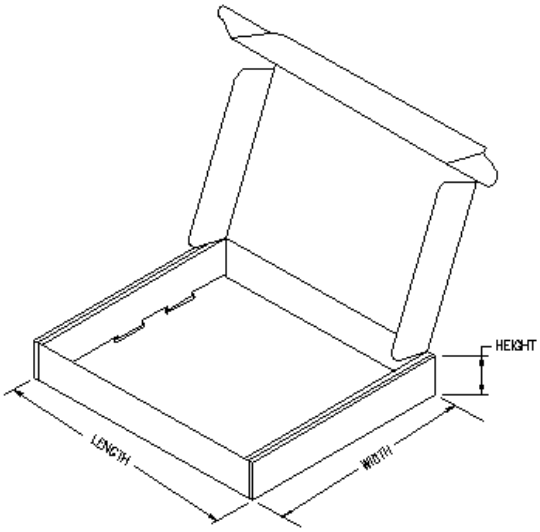
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS305ZQER	ZQE	80	TAI	330	12	5.3	5.3	1.5	8	12	NONE

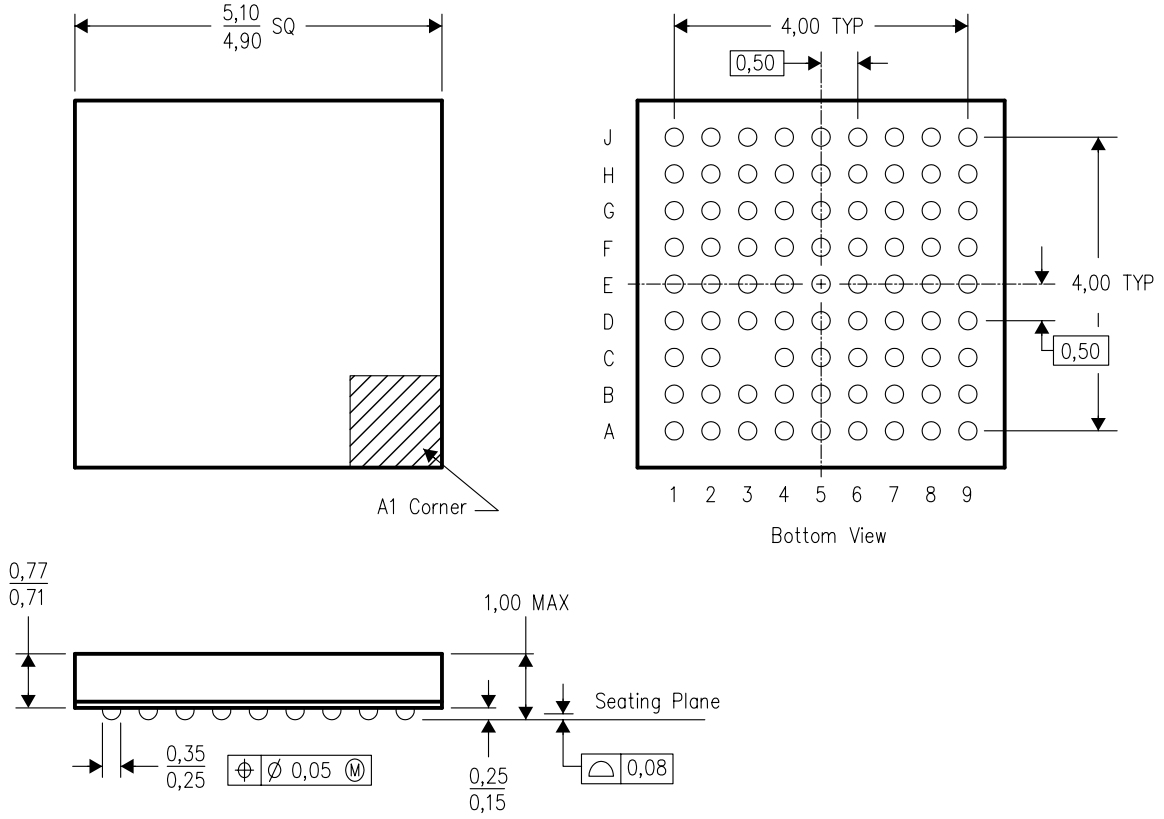


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65LVDS305ZQER	ZQE	80	TAI	342.9	336.6	20.64



ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334–4/D 10/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

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Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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